Integrated circuits
Part 8 May 1982

Analogue circuits

signetics

Analog Data Manual 1982

Signetics

PREFACE

The Analog Division, one of ten Signetics divisions, is a major supplier of a broad line of Analog integrated circuits ranging from proprietary high performance original designs to many of the more popular industry standard devices and custom designs.

The 1982 Analog Data Manual provides complete technical data on Signetics Analog Division's full line of standard linear, consumer and data conversion integrated circuit products.

Employing Signetics high quality processing and screening standards, the Analog Division is dedicated to providing high quality analog products to our worldwide customers. Our full product line addresses the needs of the EDP, Automotive, Military, Industrial, Consumer and Communication markets.

Our products include a line of wide performance operational and video amplifiers, timers, comparators, A/D and D/A converters, sample/holds, radio and audio circuits, computer and display interface circuits, phase-locked loops, power controllers and transistor arrays.

A few of the more popular original Signetics analog product designs in this data manual include the NE555 timer, NE5534 low noise op amp, NE592 video amplifier, 5018 and 5020 D/A converters, the 5036 and 5037 A/D converters, and the Dolby circuits, the NE648, NE649 and NE650.

Helpful selection and cross reference guides are included to help the designer search for the correct devices. In addition, a packaging section and hi-rel screening for MIL-STD 38510 devices are included. Contact the Signetics sales office, representative or distributor nearest you for further assistance.

Although every attempt has been made to insure the accuracy of the information in this manual, Signetics assumes no liability for inadvertent errors.

Your suggestions for improvement in further editions are welcome.

Signetics Analog Marketing

PRODUCT DELETIONS/ADDITIONS

DELETIONS

NE5007/5008/SE5008[1]	8-Bit High Speed Multiplying D/A Converter
NE/SE5009[1]	8-Bit High Speed Multiplying D/A Converter
NE5522	Universal Analog Controller
NE/SE5553/5554	Dual Polarity Regulator
SD210/211/212/213/214/215	D-MOS FET Switch N-Channel Enhancement
SD300/303/304	D-MOS FET Dual Gate N-Channel Enhancement
SD305/306	D-MOS FET Dual Gate N-Channel Enhancement
SD5000/5001/5002	D-MOS FET Quad Analog Switch Arrays and Multiplexers
75S107	High Speed Dual Line Receiver
75S108	High Speed Dual Line Receiver
75S207	High Speed Dual Sense Amplifier for MOS Memories
75S208	High Speed Dual Sense Amplifier for MOS Memories

ADDITIONS

CA3183	High Voltage Transistor Array	13-3
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NOTE
1. See DAC-08 Series

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ORDERING INFORMATION

ORDERING INFORMATION

Signetics' Analog integrated circuit products may be ordered by contacting either the local Signetics sales office, Signetics representatives and/or Signetics authorized distributors. A complete listing is located in the back of this manual.

Minimum Factory Order:

Commercial Product:
$1000 per order
$250 per line item per order

Military Product:
$250 per line item per order

Table 1 provides part number information concerning for both Signetics originated products and industry standard products.

Table 2 is a cross reference of both the old and new package suffixes for all presently existing types, while Table 3 and 4 provide appropriate explanations on the various prefixes employed in the part number descriptions.

As noted in Table 3, Signetics defines device operating temperature range by the appropriate prefix. It should be noted however, that devices with a SE prefix (-55° C to +125° C) indicates only its operating temperature range and *not* its military qualification status. The military qualification status of any analog product can be determined by either looking in the Military Section in this manual and/or contacting your local sales office.

Table 1 PART NUMBER DESCRIPTION

PART NUMBER	CROSS REF PART NO.	PRODUCT FAMILY	PRODUCT DESCRIPTION
NE5534N		ANA	Low Noise OP-AMP
μA741C	LM741CJ	ANA	General Purpose OP-AMP

→ Description of Product Function

→ Product Family

ECL Emitter Coupled Logic
DTL Diode Transistor Logic
ANA Analog Products
MOS Metal Oxide Silicon
BIM Bipolar Memory Products
MIL Military Products
TTL Transistor Logic
ML2 Military Products

→ Package Type—See Table 1

→ Device Number and Temperature Range Suffix

→ Device Family and Temperature Range Prefix for Industry Standard and Signetics Originated Products—See Table 2.

Table 2 PACKAGE DESCRIPTIONS

SUFFIX		PACKAGE DESCRIPTION2
Old	New	
A,AA	N	14-lead plastic DIL
A	N-14	14-lead plastic DIL (Selected Analog products only)
B,BA	N	16-lead plastic DIL
-	D	Microminiature package (SO)
F	F	14, 16, 18, 22 and 24-lead ceramic (Cerdip) DIL
I,IK	I	14, 16, 18, 22, 28 and 4-lead ceramic DIL
K	H	10-lead TO-100
L	H	10-lead high-profile TO-100 can
NA,NX	N	24-lead plastic DIL
Q,R	Q	10, 14, 16 and 24-lead ceramic flat
T,TA	H	8-lead TO-99
U	U	SIL Plastic power
V	N	8-lead plastic DIL
W,WJ	W	10, 14, 16 and 24-lead ceramic (Cerpac) flat
XA	N	18-lead plastic DIL
XC	N	20-lead plastic DIL
XC	N	22-lead plastic DIL
XL,XF	N	28-lead plastic DIL

Table 3 DEVICE TEMPERATURE

PREFIX	DEVICE TEMPERATURE RANGE
N-	0° to +70°C
S-	-55° to +125°C
NE-	0° to +70°C
SE-	-55° to +125°C
SA	-40° to +85°C
SU	-25° to +85°C

Table 4 FAMILY PREFIX

PREFIX	DEVICE FAMILY
CA	Linear Industry Standard
DS	Linear Industry Standard
JB	Mil Rel—Jan Qualified—Old Designator
JM	Mil Rel—Jan Qualified—New Designator
LH	Linear Industry Standard
LM	Linear Industry Standard
M	Mil Rel—Jan Processed
MC	Linear Industry Standard
SD	Linear DMOS
μA	Linear Industry Standard
ULN	Linear Industry Standard

PRODUCT STATUS DEFINITIONS

DEFINITION OF TERMS

Data Sheet Identification	Product Status	Definition
Preview	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Advance Information	Sampling or Pre-Production	This data sheet contains advance information and specifications are subject to change without notice.
Preliminary	First Production	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification Noted	Full Production	This data sheet contains final specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Section 1
Indices

ALPHA/NUMERIC INDEX

SIGNETICS ANALOG SELECTOR GUIDE

OPERATIONAL AMPLIFIERS

DEVICE	COM-PLEXITY	TEMP. RANGE	MAX. INPUT VOLTAGE		MAX. INPUT CURRENT		MIN. A VOL (V/mV)	TYP. BW Av = 1 (MHz)	TYP. SLEW RATE (V/μs)	DIFF. INP. VOLT (V)	TYP. COMMON MODE REJ. VOLT.		TYP. PSRR (dB)	SUPPLY VOLT. TYP.		OUTPUT CURR. (mA)	MAX. SUPPLY CURR. (mA)	MIN. OUTPUT VOLT. SWING (V)	INT. COMPEN-SATION	INPUT NOISE VOLT. (N√Hz)
			Offset (mV)	Drift (μV/°C)	Offset (nA)	Bias (nA)					Ratio (dB)	Range (V)		Min. (V)	Max. (V)					
NE536	Sing.	Ind.	30●	30●	5pA■	0.1▲	25	1.0	6.0	±30	80	±11	80	±6	±20	5.0	8.0▲	±12	yes	
SU536	Sing.	Ext.	30	20●	5pA■	3.0	50	1.0	6.0	±30	80	±11	86	±6	±18	5.0	5.5▲	±12	yes	
NE530	Sing.	Ind.	6.0	6●	80	200	25	3.0	35	±30	90	±13	70	±15	±18	25▲	3.0	±12	yes	
SE530	Sing.	Ind.	3.0	15	20	100	25	3.0	35	±30	90	±13	70	±15	±18	25▲	3.0	±12	yes	
SE538	Sing.	Mil.	3.0	15	20	100	25	6.0	60	±30	90	±13	70	±15	±22	25▲	3.6	±12	yes	
NE538	Sing.	Ind.	6.0	6●	80	200	25	6.0	60	±30	90	±13	70	±15	±18	25▲	2.2●	±12	yes	
NE5534/A	Sing.	Ext.	4.0▲		300▲	1500▲	30▲	10.0	13	±5	100	±13	100	±3	±22	38■	6.5▲	±12	yes	4.5
SE5534/A	Sing.	Mil.	3.0		500	1500	25	10.0	13	±5	100	±13	100	±3	±22	38■	9.0	±12	yes	4.5
μA740C	Sing.	Ind.	30●		0.06●	10.0	500●	1.0	6.0	±30	80	±12	80	±5	±22	5.0	8.0▲	±12	yes	
μA741	Sing.	Mil.	6.0		500	1500	25	1.0	0.5	±30	90	±13	100	±3	±22	5.0	2.5	±12	yes	
μA741C	Sing.	Ind.	7.5		300	800	15	1.0	0.5	±30	90	±13	100	±3	±18	5.0	2.8▲	±12	yes	
μA748	Sing.	Mil.	6.0		500	1500	25	1.0	0.5	±30	0	±13	90	±3	±22	5.0	2.8	±12	no	
μA748C	Sing.	Ind.	7.5		300	800	25	1.0	0.5	±30	90	±13	90	±3	±18	5.0	2.8	±12	no	
LM158	Dual	Mil.	7.0	7●	100	300	25	1.0		32	70	$V_S - 1.5$	100	3	30	40	2.0	$V_S - 2$	yes	
LM258	Dual	Ext.	9.0	7●	150	500	15	1.0		32	65	$V_S - 1.5$	100	3	30	40	2.0	$V_S - 2$	yes	
LM358	Dual	Ind.	9.0	7●	150	500	15	1.0		32	65	$V_S - 1.5$	100	3	30	40	2.0	$V_S - 2$	yes	
MC1458	Dual	Ind.	7.5		300	800	15	1.0	0.8	±30	90	±13	90	±3	±18	5.0	5.6▲	±12	yes	
MC1588	Dual	Mil.	6.0		500	1500	25	1.0	0.5	±30	90	±13	90	±3	±22	5.0	5.0▲	±12	yes	
SA1458	Dual	Ext.	7.5		500	1500	15	1.0	0.8	±30	90	±13	90	±3	±18	5.0	5.0▲	±12	yes	
NE532	Dual	Ind.	7.5	7●	150	500	15	1.0		32	70	$V_S - 1.5$	100	3	30	40	1.2	$V_S - 2$	yes	
SA532	Dual	Ext.	7.5	7.5●	150	500	15	1.0		32	70	$V_S - 1.5$	100	3	30	40	1.2	$V_S - 2$	yes	
SE532	Dual	Mil.	7.0	7●	100	300	25	1.0		32	70	$V_S - 1.5$	100	3	30	40	1.2	$V_S - 2$	yes	
μA747	Dual	Mil.	6.0		500	1500	25	1.0	.05	±30	90	±13	90	±3	±22	5.0	3.3	±12	yes	
μA747C	Dual	Ind.	7.5		300	800	15	1.0	0.5	±30	90	±13	90	±3	±18	5.0	3.3	±12	yes	
SE5535	Dual	Mil.	3.0	15	20	100	25	1.0	15	±30	90	±13	70	±3	±22	5.0	3.3	±12	yes	
NE5535	Dual	Ind.	6.0	6●	80	200	25	1.0	15	±30	90	±13	70	±3	±18	5.0	2.0●	±12	yes	
LM124	Quad	Mil.	7.0	7●	100	300	25	1.0		32	85	$V_S - 1.5$	100	3	30	40	2.0	$V_S - 2$	yes	
LM224	Quad	Ext.	9.0	7●	150	500	15	1.0		32	85	$V_S - 1.5$	100	3	30	40	2.0	$V_S - 2$	yes	
LM324	Quad	Ind.	9.0	7●	150	500	15	1.0		32	85	$V_S - 1.5$	100	3	30	40	2.0	$V_S - 2$	yes	
SA534	Quad	Ext.	9.0	7●	150	500	15	1.0		32	85	$V_S - 1.5$	100	3	30	40	2.0	$V_S - 2$	yes	
LM2902	Quad	Ext.	15.0	7●	200	1000	15	1.0		26	85	$V_S - 1.5$	100	3	26	40	2.0	$V_S - 2$	yes	
SE5538	Dual	Mil.	3.0	15	20	100	25	6.0	60	±30	90	±13	70	±15	±22	25▲	3.6	±12	yes	
NE5538	Dual	Ind.	6.0	6●	80	200	25	6.0	60	±30	90	±13	70	±15	±18	25▲	2.2●	±12	yes	
SE5530	Dual	Mil.	3.0	15	20	100	25	3.0	35	±30	90■		70	±3	±22		3.6	±13	yes	
NE5530	Dual	Ind.	6.0	6●	80	200	25	3.0	35	±30	90■		70	±3	±18		2.2	±13	yes	
NE5532/A	Dual	Ind.	5.0		200	1000	10	10	9	±5	100		80	±5	±22		16	±15	yes	6
NE5533/A	Dual	Ind.	5.0		400	2000	15	10	13	±5	100		80	±5	±22		8	±15	yes	4.5
NE5512	Dual	Ind.	1.5		8	8	200		1				100		±16		5.5	±8		30
NE5514	Quad	Ind.	1.5		8	8	25		1		100		100		±16		12	±8		30
NE4558	Dual	Ind.	2.0		200	500			0.5		100				±18			±10		
MC3403	Quad	Ind.	10		75	500			0.6		90		30					±18		

NOTES
1. Military: −55°C to +125°C
Extended: −25°C to +85°C
Industrial: 0°C to +70°C
2. Specifications guaranteed over full temperature range unless otherwise indicated by the following marks:
● Typical over full temperature range ▲ Guaranteed at 25°C ■ Typical at 25°C

SIGNETICS ANALOG SELECTOR GUIDE

COMPARATORS

DEVICE	COMPLEXITY	TEMP. RANGE*	MAX. INP. OFFSET VOLT. (mV)	MAX. INP. CURRENT		SUPPLY VOLTAGE (V)	RESPONSE TIME (TYP.) (ns)	COMMON MODE VOLTAGE RANGE (V)	OUTPUT VOLT.		OUTPUT STRUCTURE	VOLT. GAIN (TYP.) (V/mV)	TTL FANOUT	MAX. DIFF. INPUT VOLT. (V)	PACKAGES
				Bias μA)	Offset μA)				V_{OL} Max. (V)	V_{OH}Min. (V)					
LM111[1]	Single	M	4.00	0.15	0.02	± 15	200	± 14	0.4		O.C.	200	5	± 30	F,T
LM211	Single	E	4.00	0.15	0.02	to	200	± 14		O.C.	200	5	± 30	F,N,T	
LM311	Single	I	10.0	0.30	0.07	+ 5 and GND	200	± 14	0.4		O.C.	200	5	± 30	F,N,T
NE527[2]	Single	I	10.0	4.00	1.00	± 5 to ± 15	16	± 6	0.5	2.7	TTL		5	± 5	F,K,N
SE527	Single	M	6.00	4.00	1.00	and GND	16	± 6	0.5	2.5	TTL		5	± 5	F,K
NE529[2]	Single	I	10.0	50.0	15.0	± 5 to ± 15	12	± 6	0.5	2.7	TTL		5	± 5	F,K,N
SE529	Single	M	6.00	36.0	9.00	and GND	12	± 6	0.5	2.5	TTL		5	± 5	F,K
LM119[1]	Dual	M	7.00	1.00	0.10	± 15	80	± 13	0.6		O.C.	40	2	± 5	K,F
LM219	Dual	E	7.00	1.00	0.10	to	80	± 13	0.6		O.C.	40	2	± 5	K,F
LM319	Dual	I	10.0	1.20	0.30	± 5 and GND	80	± 13	0.6		O.C.	40	2	± 5	F,K,N
LM193[3]	Dual	M	9.00	0.30	0.10	± 1 to ± 18	1300	0 to V_S−2	0.7		O.C.	200	2	36	T
LM293	Dual	E	9.00	0.40	0.15	or	1300	0 to V_S−2	0.7		O.C.	200	2	36	N,T
LM393	Dual	I	9.00	0.40	0.15	+2 to +36 GND	1300	0 to V_S−2	0.7		O.C.	200	2	36	N,T
LM2903	Dual	E	15.0	0.50	0.20		1300	0 to V_S−2	0.7		O.C.	100	2	36	N,T
NE521[4]	Dual	I	10.0	40.0	12.0	+ 5, − 5 GND	7	± 3	0.5	2.7	TTL		12	± 6	F,N
NE522	Dual	I	10.0	40.0	12.0	+ 5, − 5, GND	9	± 3	0.5		O.C.		12	± 6	F,N
LM139[3]	Quad	M	9.00	0.30	0.10		1300	0 to V_S−2	0.7		O.C.	200	2	36	F,N
LM239	Quad	E	9.00	0.40	0.15	± 1 to ± 18 or	1300	0 to V_S−2	0.7		O.C.	200	2	36	F,N
LM339	Quad	I	9.00	0.40	0.15	+ 2 to + 36	1300	0 to V_S−2	0.7		O.C.	200	2	36	F,N
LM2901	Quad	E	15.0	0.50	0.20		1300	0 to V_S−2	0.7		O.C.	100	2	36	N
MC3302[3]	Quad	E	40.0	1.00	0.20	+2 to +28 GND	2000	0 to V_S−2	0.4		O.C.	30	2	28	N

NOTES

1. With strobe; will work from single supply
2. Complementary output gates with individual strobes.
3. Will operate from single or dual supplies.
4. Ultra high speed

*Temperature Range
E = Extended
I = Industrial
M = Military

D/A CONVERTERS

PRODUCT	# BITS	ACC. %	OUTPUT			INT. REF.	INT. LATCH	PACKAGE		TEMPERATURE RANGE		RELIABILITY	
			V	I	T			N	F	Com'l.	Mil.	SURE II	SUPR II
MC1408-6	8	.78		X				X	X	X		X	
MC1408-7	8	.39		X				X	X	X		X	X
MC1408-8	8	.19		X				X	X	X		X	X
MC1508-8	8	.19		X					X		X	X	X
DAC-08C	8	.39		X	X			X	X	X		X	X
DAC-08E	8	.19		X	X			X	X	X		X	X
DAC-08H	8	.1		X	X			X	X	X		X	X
DAC-08	8	.19		X	X				X		X	X	X
DAC-08A	8	.1		X	X				X		X	X	X
NE5018	8	.19	X			X	X	X	X	X		X	X
NE5019	8	.1	X			X	X	X	X	X		X	X
SE5018	8	.19	X			X	X		X		X	X	X
SE5019	8	.1	X			X	X		X		X	X	X
NE5118	8	.19		X		X	X	X	X	X		X	
NE5119	8	.1		X		X	X	X	X	X		X	
SE5118	8	.19		X		X	X		X		X	X	
SE5119	8	.1		X		X	X		X		X	X	
NE5020	10	.1	X			X	X	X	X	X		X	

ANALOG CROSS REFERENCE GUIDE

ANALOG CROSS REFERENCE

Manufacturer	T.I.	AMD	FAIRCHILD	INTEL	MOTOROLA	NATIONAL	SIGNETICS
TEMPERATURE RANGE CROSS REFERENCE							
Commercial	72, 74, 75	C	C	—	14, 34, 86	3, 86, 88	NE
Military	52, 54, 55	M	M	M	15, 35, 96	1, 96, 78	SE
PACKAGE CROSS REFERENCE							
Hermetic DIP	J	D	D	C, D	L	D	F-FE
Molded DIP	N	P	P	P	P_2	N	N
Mini-Molded DIP	P	T	T	—	P_1	N	N
Metal Can	L	H	H	—	G, R	H	H
Small Outline (SO)	—	—	—	—	D	—	D

PART NUMBER CROSS REFERENCES

TYPE TO BE REPLACED	SIGNETICS REPLACEMENT	TYPE TO BE REPLACED	SIGNETICS REPLACEMENT	TYPE TO BE REPLACED	SIGNETICS REPLACEMENT
AD741CN	μA741CN	CA741CE	μA741CN	LM239N	LM239N
AD559JD	MC1408-8F	CA741CF	μA741CFE	LM258JG	LM258FE
AD559K	MC1408-8F	CA741F	μA741FE	LM258P	LM258N
AD559KD	MC1408-8F	CA747CF	μA747CF	LM293P	LM293N
AD559S	MC1508-8F	CA747F	μA747F	LM301AJG	LM301AFE
AD559SD	MC1508-8F	CA748CE	μA748CN	LM311D	LM311F
AM555DC	NE555F	CA748CF	μA748CF	LM311J	LM311F
AM555DM	SE555F	CA748F	μA748F	LM311J-14	LM311F
AM555HC	NE555H	CA1458E	MC1458N	LM311JG	LM311FE
AM555HM	SE555H	CA1458F	MC1458FE	LM311N	LM311N
AM555TC	NE555N	CA3081E	CA3081N	LM311P	LM311N
AM723DC	μA723CF	CA3082E	CA3082N	LM319D	LM319F
AM723DM	μA723F	CA3183E	CA3183N	LM319J	LM319F
AM741DC	μA741CFE	DAC-08A	DAC-08A/SE5009	LM319N	LM319N
AM741DM	μA741FE	DAC-08	DAC-08/SE5008	LM324J	LM324F
AM747DC	μA747CF	DAC-08H	DAC-08H/NE5009	LM324N	LM324N
AM747DM	μA747F	DAC-08E	DAC-08E/NE5008	LM339J	LM339F
AM748DC	μA748CF	DAC-08C	DAC-08C/NE5007	LM339N	LM339N
AM748DM	μA748F	DS1488J	MC1488F	LM358H	LM358H
AMLM211D	LM211F	DS1489AJ	MC1489AF	LM358JG	LM358FE
AMLM311D	LM311F	DS1489J	MC1489F	LM358L	LM358H
CA111F	LM111F	LM111D	LM111F	LM358N	LM358N
CA124F	LM124F	LM111J	LM111F	LM358P	LM358N
CA139AF	LM139AF	LM119D	LM119F	LM361D	NE529F
CA139F	LM139F	LM119J	LM119F	LM361H	NE529H
CA211F	LM211F	LM124D	LM124F	LM361J	NE529F
CA224F	LM224F	LM124J	LM124F	LM361N	NE529N
CA239AF	LM239F	LM139D	LM139F	LM381N	LM381N
CA239F	LM239F	LM139J	LM139F	LM382N	LM382N
CA301AF	LM301AFE	LM158JG	LM158FE	LM387N	LM387N
CA311F	LM311F	LM161D	SE529F	LM393N	LM393N
CA324E	LM324N	LM161H	SE529H	LM393P	LM393N
CA324F	LM324F	LM161J	SE529F	LM555CH	NE555H
CA339E	LM339N	1LM211D	LM211F	LM555CN	NE555N
CA339F	LM339F	LM211J	LM211F	LM555H	SE555H
CA555CE	NE555N	LM219D	LM219F	LM556CD	NE556F
CA555CF	NE555F	LM219J	LM219F	LM556CJ	NE556F
CA555CT	NE555H	LM224D	LM224F	LM556CN	NE556N
CA555F	SE555F	LM224J	LM224F	LM556D	SE556F
CA555T	SE555H	LM224N	LM224N	LM556J	SE556F
CA723CE	μA723CN	LM239D	LM239F	LM565CH	NE565H
CA723E	μA723N	LM239J	LM239F	LM565CN	NE565N

ANALOG CROSS REFERENCE GUIDE

PART NUMBER CROSS REFERENCES (Continued)

TYPE TO BE REPLACED	SIGNETICS REPLACEMENT	TYPE TO BE REPLACED	SIGNETICS REPLACEMENT	TYPE TO BE REPLACED	SIGNETICS REPLACEMENT
LM565H	SE565H	MC1458SP1	NE5535N	MLM324P	LM324N
LM566CN	NE566N	MC1458U	MC1458FE	MLM339AL	LM339AF
LM567H	SE567H	MC1488L	MC1488F	MLM339AP	LM339AN
LM567CN	NE567N	MC1489AL	MC1489AF	MLM339L	LM339F
LM567H	SE567H	MC1489L	MC1489F	MLM339P	LM339N
LM723CD	μA723CF	MC1496G	MC1496H	MLM358G	LM358H
LM723CJ	μA723CF	MC1496L	MC1496F	MLM358P1	LM358N
LM723CN	μA723CN	MC1496P	MC1496N	MLM358U	LM358FE
LM723D	μA723F	MC1508L8	MC1508-8F	MLM565CP	NE565N
LM723J	μA723F	MC1555G	SE555H	MLM2901P	LM2901N
LM723N	μA723N	MC1555U	SE555FE	MLM2902P	SA534N
LM733CD	μA733CF	MC1556U	MC1556FE	μA124DM	LM124F
LM733CJ	μA733CF	MC1558JG	MC1558FE	μA224DM	LM224F
LM733CN	μA733CN	MC1558SL	SE5535F	μA301ANC	LM301AN
LM733D	μA733F	MC1558U	MC1558FE	μA311TC	LM311N
LM733T	μA733F	MC1596G	MC1596H	μA324DC	LM324F
LM741CJ	μA741CFE	MC1596L	MC1596F	μA324PC	LM324N
LM741CN	μA741CN	MC1723CL	μA723CF	μA339ADC	LM339AF
LM747CD	μA747CF	MC1723CP	μA723CN	μA339DC	LM339F
LM747CJ	μA747CF	MC1723L	μA723F	μA339PC	LM339N
LM747D	μA747F	MC1733CL	μA733CF	μA555HC	NE555H
LM747J	μA747F	MC1733CP	μA733CN	μA555HM	SE555H
LM748CJ	μA748CF	MC1733L	μA733F	μA555TC	NE555N
LM748CN	μA748CN	MC1741CP1	μA741CN	μA556DC	NE556F
LM748J	μA748F	MC1741CU	μA741CFE	μA556DM	SE556F
LM1458J	MC1458FE	MC1741SCP1	NE535N	μA556PC	NE556N
LM1458N	MC1458N	MC1741SCU	NE535FE	μA723CJ	μA723CF
LM1496J	MC1496F	MC1741SU	SE535FE	μA723CN	μA723CN
LM1496N	MC1496N	MC1741U	SE535FE	μA723DC	μA723CF
LM1558J	MC1558FE	MC1747CL	μA747CF	μA723DM	μA723F
LM1596H	MC1596H	MC1747CP2	μA747CN	μA723MJ	μA723F
LM1596J	MC1596F	MC1747L	μA747F	μA723PC	μA723CN
LM2901J	LM2901F	MC1748CP1	μA748CN	μA733CJ	μA733CF
LM2901N	LM2901N	MC3302L	MC3302F	μA733CN	μA733CN
LM2902J	SA534F	MC3302P	MC3302N	μA733DC	μA733CF
LM2902N	SA534N	MC3456L	NE556F	μA733DM	μA733F
LM2903N	LM2903N	MC3456P	NE556N	μA733MJ	μA733F
LM2903P	LM2903N	MC3556L	SE556F	μA740HC	μA740CH
MC1408L6	MC1408-6F	MLM111L	LM111F	μA741CJG	μA741CFE
MC1408L7	MC1408-7F	MLM111U	LM111FE	μA741CP	μA741CN
MC1408L8	MC1408-8F	MLM124L	LM124F	μA741MJG	μA741FE
MC1408P6	MC1408-6N	MLM139AL	LM139AF	μA741TC	μA741CN
MC1408P7	MC1408-7N	MLM139L	LM139F	μA747CJ	μA747CF
MC1408P8	MC1408-8N	MLM158U	LM158FE	μA747CN	μA747CN
MC1411P	ULN2001N	MLM211L	LM211F	μA747DC	μA747CF
MC1416P	ULN2004N	MLM211U	LM211FE	μA747DM	μA747F
MC1455G	NE555H	MLM224L	LM224F	μA747MJ	μA747F
MC1455P1	NE555N	MLM224P	LM224N	μA747PC	μA747CN
MC1455U	NE555FE	MLM239AL	LM239AF	μA748CJ	μA748CF
MC1456CP1	MC1456N	MLM239AP	LM239AN	μA748CP	μA748CN
MC1456CU	MC1456FE	MLM239L	LM239F	μA748DC	μA748CF
MC1456P1	MC1456N	MLM239P	LM239N	μA748DM	μA748F
MC1456U	MC1456FE	MLM258P1	LM258N	μA748MJ	μA748F
MC1458CL	MC1458F	MLM258U	LM258FE	μA748TC	μA748CN
MC1458CP1	MC1458N	MLM301AP1	LM301AN	μA796HC	MC1496H
MC1458CU	MC1458FE	MLM301AU	LM301AFE	μA0802DC-1	MC1408-8F
MC1458JG	MC1458FE	MLM311L	LM311F	μA0802DC-2	MC1408-7F
MC1458P	MC1458N	MLM311P1	LM311N	μA0802DC-3	MC1408-6F
MC1458P1	MC1458N	MLM311U	LM311FE	μA0802DM-1	MC1508-8F
MC1458SL	NE5535F	MLM324L	LM324F	μA0802PC-1	MC1408-8N

PART NUMBER CROSS REFERENCES (Continued)

TYPE TO BE REPLACED	SIGNETICS REPLACEMENT	TYPE TO BE REPLACED	SIGNETICS REPLACEMENT	TYPE TO BE REPLACED	SIGNETICS REPLACEMENT
µA0802PC-2	MC1408-7N	SN72311J	LM311F	733CJ	µA733CN
µA0802PC-3	MC1408-6N	SN72311P	LM311N	747BL	µA747F
µA1458TC	MC1458N	SN72555L	NE555H	747CJ	µA747CN
µA2901PC	LM2901N	SN72555P	NE555N	747CL	µA747CF
µA2902PC	SA534N	SN72558P	MC1458N	748BL	µA748F
NE555JG	NE555FE	SN72723N	µA723CN	748CL	µA748CF
NE555L	NE555H	SN72733J	µA733CF	1458CP	MC1458N
NE555P	NE555N	SN72733N	µA733CN	1458P	MC1458N
NE592G	NE592H	SN72741P	µA741CN	2740CE	µA740CH
NE592L	NE592F	SN72747J	µA747CF	9665DC	ULN2001F
RC723D	µA723CF	SN72747N	µA747CN	0665PC	ULN2001N
RC733D	µA733CF	SN72748J	µA748CF	µA3089N	CA3089N
RC741DN	µA741CN	SN72748P	µA748CN	µA3089	CA3089N
RC747D	µA747CF	SN72771N	MC1456N	µA760HM	NE527H
RC1458DN	MC1458N	SN75188J	MC1488F	µA760DC	NE527N
RC1488DC	MC1488F	SN75188N	MC1488N	µA7898TC	NE532N
RC1489ADC	MC1489AF	SN75189AT	MC1489AF	µA740HM	NE536H
RC1489DC	MC1489F	SN75189AN	MC1489AN	µA556PC	NE556N
SE555JG	SE555FE	SN75189J	MC1489F	µA0801	DAC-08N
SE555L	SE555H	SN75189N	MC1489N	µA0801A	DAC-08AN
SE592G	SE592H	TBB0748B	µA748CN	µA758PC	µA758N
SE592L	SE592F	TBB1458B	MC1458N	µA739PC	LM387N
SFC2301ADC	LM301AN	TDB0555	NE555H	µA739PC	LM382N
SFC2741DC	µA741CN	TDB0555B	NE555N	µA796PC	MC1496N
SFC2741EC	µA741CN	TDB0556A	NE556N	µA760HC	NE529N
SFC2741EM	µA741N	TDB0723A	µA723CN	SN7512L	µA733CH
SFC2748DC	µA748CN	TDC0555	SE555H	SN7512N	µA733N
SN52555L	SE555H	ULN2001A	ULN2001N	SN76689N	CA3089N
SN52723J	µA723F	ULN2003A	ULN2003N	ULN2210A	µA758N
SN52733J	µA733F	ULN2004A	ULN2004N	ULN2244	µA758N
SN52747J	µA747F	556CJ	NE556CN	µA740HC	µA740CH
SN52748J	µA748F	723CT	µA723CN		
SN72301AP	LM301AN	723CL	µA723CF		

Section 2
Quality, Reliability and Assurance

QUALITY, RELIABILITY AND ASSURANCE

QUALITY AND RELIABILITY

Quality and reliability are two important measures of a product's merit. Quality is a measure of an integrated circuit's conformance to agreed-upon criteria at a given time, while Reliability is a measure of the circuit's ability to continue to conform over a period of time. The Signetics SUPR II Program has been designed to upgrade the basic product quality through the use of more rigorous screening criteria at the critical process steps. These additional screens constitute the Level A portion of the Program. A burn-in option is available for those users requiring enhanced reliability performance, and this option is designated as Level B.

Quality

The quality of an integrated circuit is appraised by the user based on the ability of the circuit to meet the specified electrical criteria and external visual appearance. The SUPR II Program focuses on supplying to the user a product that has a high probability of meeting the user's needs through the sampling plans defined in MIL-STD-105D and the quality levels (AQL's) stated in Table II. Many of the inspection methods at critical process steps are now based on MIL-STD-883 criteria in order to build, rather than test, quality into the product.

Reliability

System performance over a period of time is the user's measure of an integrated circuit's reliability. The SUPR II Program improves system reliability by building quality into the product via additional manufacturing inspections and the offering of a burn-in screen. In addition to the SUPR II Program, Signetics performs periodic reliability testing via the SUREIII/883A Program to assure continuing uniformity and long-term reliability of all product lines. This data base is available upon request as is the ten-year reliability summary, Signetics Product Reliability Report, R-363.

How Do Integrated Circuit Failures Occur?

Results from the Signetics Failure Analysis Lab over a three-year period on product returned from board checkout, system checkout, field usage and accelerated life testing are graphically presented in Figure 1. Under typical system operating conditions, random manufacturing defects, as outlined in Table 1, are the primary cause of true device failure. Also shown in Table 1 are the process controls that have been added via the SUPR II Program to minimize these defects prior to shipment to the customer. The device failure models are categorized as:

Half of the devices analyzed were found to be electrically good. They are attributed to being "false pulls" that occur during normal troubleshooting at the board and system levels.

Devices damaged by electrical over-stress account for 25% of the failures. Typical causes for electrical over-stress are incorrect board insertion, board shorts between device pins, power supply transients, and poor handling techniques.

The remaining 25% were verified to be true failures which occurred as a result of an in-process manufacturing defect or test escape.

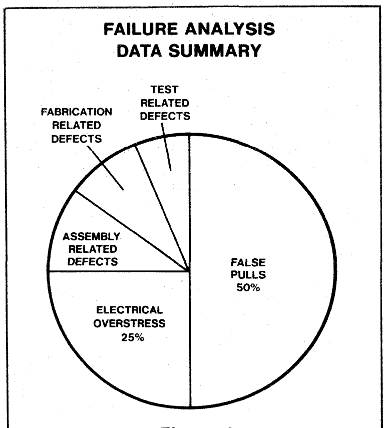

FAILURE ANALYSIS DATA SUMMARY

Figure 1

SIGNETICS SUPR II LEVEL A

Improved Quality Benefits

From the user's point of view, improved integrated circuit quality from the supplier means a lower cost of ownership. This cost saving can be effected through the reduction or elimination of involved incoming inspection testing, reduced PC board rework, simplified system checkout, reduced in-line inventories, and less complicated part tracking by Purchasing Management.

The SUPR II Program is Corporate in scope and covers Logic (Standard TTL, Schottky TTL, Low Power Schottky TTL, ECL, 8T Interface), Analog (Industrial, Consumer, Interface), Bipolar Memories (RAM's, ROM's, PROM's), and MOS Memories (RAM's, ROM's, Shift Registers), All package options are also available.

The SUPR II flow is detailed in Figure 5, including the test methods and Quality acceptance levels (Table 2 provides the electrical/mechanical finished product AQL's). Highlights of the flow are visual inspections, thermal shock preconditioning, hermeticity, and burn-in, all based on MIL-STD-883 criteria.

A good example of the savings which can be achieved by purchasing tighter inspection levels is given in Figure 2. Here we are comparing the various levels of inspection (AQL's) available for device functionality and its impact on the number of PC boards which must be reworked during system manufacturing. Using the standard commercial AQL in functionality of 1.0%, at 120 integrated circuit packages per board, typically more than 90% of boards will require rework. At 0.15% AQL, rework is reduced to 25%, and at 0.1%, typically only 12% rework is required.

SIGNETICS SUPR II LEVEL B

Infant Mortality Failures

Failure rates are most severe during the first few months of operating life. This is known as the "infant mortality" phase. A system

FAILURE MECHANISMS	CAUSES	SUPR II CONTROL
Die Fabrication Related	Metalization Oxide Defects Mechanical Scratches Contamination	SEM Monitor Visual Stabilization Bake Burn-In
Assembly Related	Bonding, Wire, Package and Seal Defects	Preseal Visual Thermal Shock Stabilization Bake Hermeticity Hot-Rail Testing
Test Related	Test Escapes	Tightened AQL Guarantees High Temperature Testing

Table 1

QUALITY, RELIABILITY AND ASSURANCE

AQL LEVELS ON FUNCTIONALITY VERSUS BOARD REWORK RATES

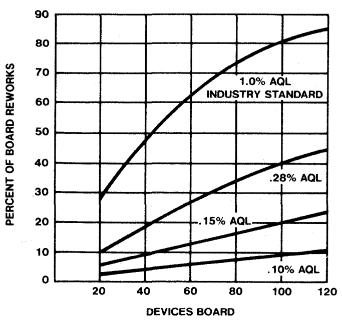


Figure 2

RELATIVE FAILURE RATE VERSUS TIME

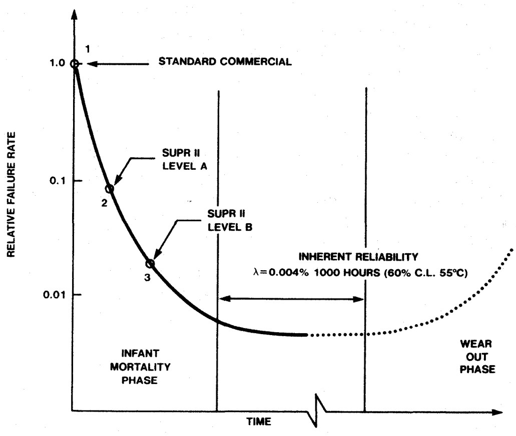


Figure 3

manufacturer has various options to solve problems arising from infant failures. He can ship his system to the end customer and repair field failures as they occur. He can operate the system in-house for this period and repair failures. Or he can purchase devices which have already been preconditioned to eliminate the early failures. Each customer must choose the most cost-effective method for his particular business. A considerable number of the reliabilty defects which cause early failures are eliminated by the manufacturing control and preconditioning steps of SUPR II Level A processing. More persistent defects can be removed by the use of "burn-in" techniques. The "burn-in" processing of SUPR II Level B effectively allows the system manufacturer to ship his equipment at Point 3 on the failure rate curve in Figure 3.

Burn-In Conditions

MIL-STD-883A, Method 1015 describes a number of different conditions for integrated circuit burn-in. For SUPR II Level B, Signetics has selected Condition F. This is the accelerated burn-in method derived from MIL-STD-883A, utilizing a high temperature reversed bias condition. This bias scheme is preferred for infant mortality screening, while operating conditions are generally utilized for internal reliability programs oriented toward generating MTBF data for the system designer.

Integrated Burn-In Flow

Signetics SUPR II Level B burn-in is performed to provide reliability assurance equivalent to a 168-hour/125°C screen. This process has been integrated into the standard manufacturing flow to provide the customer with the most cost effective screen and significantly reduced delivery times.

		ANALOG AQL GUARANTEES	
		Standard	SUPR IIA/B
HOT OPENS	100°C	0.015	0.015
DC PARAMETRIC/FUNCTIONAL	25°C	0.25	0.10
DC PARAMETRIC/FUNCTIONAL	MIN./MAX. RATED TEMP. (Combined)	0.40	0.25
AC PARAMETRIC	25°C	0.40	0.40
MECHANICAL	MAJOR/MINOR (Combined)	0.40	0.40
SEAL TESTS (CERAMIC/METAL CANS ONLY)	FINE LEAK 5×8^{-8}cc/s GROSS LEAK (Combined)	0.40	0.40

NOTE

1. To insure AQL levels tighter than 0.65% on D.C. parameters usually requires continual correlation of test equipment between customer and vendor to avoid test interpretation problems. If the objective is to reduce system rework costs, functional operation of a device (does it switch or toggle in the system) is often more critical than the absolute value of a parameter. For this reason SUPR II focuses on tightened AQLs on functionality.

Table 2 SUPR II AQL GUARANTEE

QUALITY, RELIABILITY AND ASSURANCE

BURN-IN FLOW

ASSEMBLY

The flow from SEM control through package seal is common to Levels A and B.

⇩

TEST

The pre-burn-in electrical screen is designed to remove assembly rejects and increase equipment efficiency.

⇩

BURN-IN

The 24-hour/155°C accelerated burn-in is well controlled to provide maximum screening effectiveness without damaging good devices.

⇩

TEST

The post-burn-in electrical is a 100% production DC/function electrical test.

Figure 4

Marking Format

Product processed to the SUPR II manufacturing flow can be identified by an SA for Level A, and an SB for the Level B burn-in option.

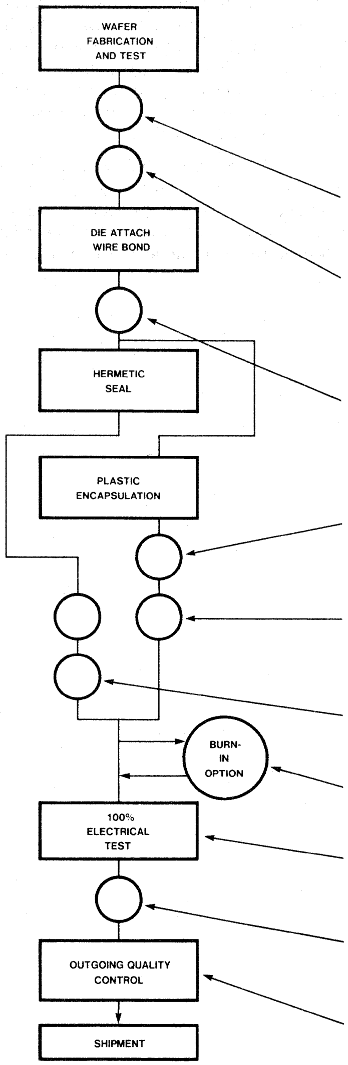
NE5534N XXXX **SA**	NE5534N XXXX **SB**
SUPR II LEVEL A	SUPR II LEVEL B

NOTE

Marking for Level A in process of being implemented.

Figure 5 shows the generalized process flow for all Signetics integrated circuits purchased to the SUPR II program. Each product group (Analog, Bipolar Memory, Logic, and MOS) may follow slightly different procedures dictated by the specific device characteristics.

SUPR II PROCESS FLOW



SCANNING ELECTRON MICROSCOPE CONTROL (SEM)
Wafers are sampled daily by the Quality Control Laboratory from each fabrication area and subjected to SEM analysis. This process control reveals manufacturing defects such as contact and oxide step coverage in the metalization process which may result in early failures.

DIE SORT VISUAL ACCEPTANCE
Criteria based on MIL-STD-883, Method 2010, Condition B, are employed to detect defects caused during fabrication, wafer testing, or the mechanical scribe and break operation. Critical defects such as scratches, smears, and glassivated bonding pads are inspected to a 1% AQL. Lot acceptance for noncritical defects is to a 4% AQL.

PRE-SEAL VISUAL ACCEPTANCE
Criteria based on MIL-STD-883, Method 2010, Condition B, are employed to detect any damage incurred at the die attach and wire bonding stations. Critical defects such as scratches, contamination and smeared ball bonds are inspected to a 0.65% AQL. Lot acceptance is to 2.5% AQL.

STABILIZATION BAKE PRECONDITIONING
Plastic molded devices are baked to stress wire and die bonds and help eliminate marginal devices. It also ensures an optimum plastic seal to enhance moisture resistance.

THERMAL SHOCK PRECONDITIONING
MIL-STD-883, Method 1011, Condition A. Devices are cycled from cold to hot temperatures imposing a very severe stress which weakens loose bonds and package seals without degrading good devices. A loosened bond is later detected during high temperature "HOT-RAIL" testing. This preconditioning is especially effective in eliminating intermittent or "HOT-OPENS" problems in plastic devices.

SEAL TESTS
Package seal integrity is ensured by 100% gross leak testing per MIL-STD-883, Method 1014, Condition C and fine leak sampling per Condition A or B.

BURN-IN (LEVEL B OPTION)
Devices are burned in for the equivalent of 168 hours at 125°C in accordance with MIL-STD-883A, Method 1015, Condition F.

100% PRODUCTION ELECTRICAL TESTING
Every device is tested for functional and DC parameters at 25°C, room ambient.

HOT RAIL, HIGH TEMPERATURE TESTING
All plastic devices are subjected to testing at 100°C. In plastic devices this eliminates "HOT-OPENS" and shorts resulting from temperature sensitive intermittent bonds. In addition, logic circuits are tested 100% to a functional pattern that simulates usage in a system environment.

QA GUARANTEES
A final QA inspection step guarantees the mechanical and electrical AQL's of Table II. Every shipment is sealed and identified by QA personnel.

Figure 5

QUALITY, RELIABILITY AND ASSURANCE

SURE III/883B RELIABILITY PROGRAM

Definition

Signetics is recognized as a manufacturer of reliable integrated circuts. Signetics realized long ago the need for a comprehensive reliability program to provide timely data representative of the entire Signetics product line. Thus the establishment of a Systematic and Uniform Reliability Evaluation program, known as SURE, which provides this data in a manner unique to the industry. Furthermore, this program is provided at no cost to customers.

The SURE Program is a Signetics in-house Qualification Test Program which has been in existence since 1963. The SURE Program is designed to monitor the continuing uniformity of all Signetics products and to demonstrate via periodic qualifications that Signetics products meet or exceed the stringent long-term reliability requirements of their intended applications.

The SURE Program is reviewed and modified annually to incorporate appropriate changes in military microelectronic test programs, products and demonstrated product capabilities, and market requirements. The 1978 SUREIII/883B Reliability Program contains minor changes to the 1975 SURE II/883A Program, most significant of which is the inclusion of recent changes in military microelectronic test programs (i.e., inclusion of MIL-SD-883B, Method 5005.4 and MIL-M-38510D). The SURE III/883B Program continues to incorporate additional environmental tests to fulfill the need for special reliability assurance of plastic products.

Section 3
Operational Amplifiers

INDEX

Section 3 — Operational Amplifiers

OPERATIONAL AMPLIFIERS—SYMBOLS AND DEFINITIONS

T_A

Ambient temperature range. Range of the surrounding environment of the operating device.

T_J

Junction Temperature. The maximum temperature of the device. 150°C is standard for silicon devices.

T_{STG}

Storage temperature range. Temperature range that the device can be stored in a non-operating condition.

T_{SOLD}

Soldering Temperature. The temperature which can be applied to the lead frame of the device for short periods of time (normally specified for a duration of 10 sec).

Absolute Maximum Rating

Operating safe zones exceeding these limits could cause permanent damage to the device and are not meant to imply that devices can operate at these limits.

Power Dissipation

The power that the device can safely handle at 25°C. The dissipation must be derated as indicated for the individual package type.

Package Type Designation

See full package designations in Appendix.

V_{CC} ($-V_{CC}$)

Supply Voltage. The range of power supply voltage over which the device will operate safely.

Bandwidth

The frequency at which the gain is down 3dB from its dc value. It's measured in sample (track) mode with a small-signal sine wave that doesn't exceed the slew rate limit.

Average Input Offset Current Temperature Coefficient (TCI_{OS})

The change in input offset current divided by the change to ambient temperature producing it.

Average Input Offset Voltage Temperature Coefficient (TCV_{OS})

The change in input offset voltage divided by the change in ambient temperature producing it.

Common Mode Input Resistance

The resistance looking into both inputs, with inputs tied together.

Common Mode Rejection Ratio (CMRR)

The ratio of the change of input offset voltage to the input common mode voltage change producing it.

Full Power Bandwidth

The maximum frequency at which the full sinewave output might be obtained.

Input Bias Current (I_B)

The average of the two input currents at zero output voltage. In some cases, the input current is measured for either input independently.

Input Capacitance

The capacitance looking into either input terminal with the other grounded.

Input Current

The current into an input terminal.

Input Noise Voltage

The square root of the mean square narrow-band noise voltage referred to the input.

Input Offset Current

The difference in the currents into the two input terminals with the output at zero volts.

Input Offset Voltage

That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

Input Resistance

The resistance looking into either input terminal with the other grounded.

Input Voltage Range

The range of voltages on the input terminals for which the amplifier operates within specifications. In some cases, the input offset specifications apply over the input voltage range.

Large-Signal Voltage Gain

The ratio of the maximum output voltage swing to the change in input voltage required to drive the output to this voltage.

Output Resistance

The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

Output Short-Circuit Current

The maximum output current available from the amplifier with the output shorted to ground or to either supply.

Output Voltage Swing

The peak output swing, referred to zero, that can be obtained.

Power Consumption

The dc power required to operate the amplifier with the output at zero and with the output at zero and with no load current.

Power Supply Rejection Ratio

The ratio of the change in input offset voltage to the change in supply voltages producing it.

Rise Time

The time required for an output voltage step to change from 10% to 90% of its final value.

Slew Rate

The maximum rate of change of output voltage under large signal condition.

Supply Current

The current required from the power supply to operate the amplifier with no load and the output at zero.

Temperature Stability of Voltage Gain

The maximum variation of the voltage gain over the specified temperature range.

NOTE

Refer to Section 3 of the 1979 Analog Applications Manual for an in depth explanation of Operational Amplifiers and their applications

OPERATIONAL AMPLIFIERS—SYMBOLS AND DEFINITIONS

MC1458 DUAL OPERATIONAL AMPLIFIER

COMPETITION	INDUSTRY VALUE	KEY PARAMETER	SIGNETICS AVAILABLE VALUE	SIGNETICS ORIGINATED DEVICES	QR&A		COMMENTS
					SURE II	SUPR II	
MOTOROLA FAIRCHILD RAYTHEON N.S.C. T.I.	.8	Slew Rate	10 to 60 V/μ sec	NE/SE 5530	Yes		
				5538	Yes		
				NE 5532	Yes		
				5532A	Yes		
				5533	Yes		
				5533A	Yes		
	14	Full power out	30 to 300 kHz	NE/SE 5530	Yes		
				5538	Yes		
				NE 5532	Yes		
				5532A	Yes		
				5533			
				5533A			
	45	Noise	4, 5 nv/$\sqrt{Hz}$	NE 5532			
				5532A			
				5533	Yes		
				5533A	Yes		
	6	Offset voltage	4 mv	NE 5532			
				5532A			
				5533	Yes		
				5533A	Yes		
	500	Bias current	60 to 150 na	NE/SE 5530	Yes		
				5538	Yes		
	1	Gain bandwidth	1.5 ↓ 15 MHz	NE/SE 5530	Yes		
				5538	Yes		
				NE 5533	Yes		
				5533A	Yes		
				5532			
				5532A			
	2,000	Maximum loading	600 OHM	NE 5533			
				5533A	Yes		
				5532	Yes		
				5532A			

OPERATIONAL AMPLIFIERS—SYMBOLS AND DEFINITIONS

μa741 SINGLE OPERATIONAL AMPLIFIER

COMPETITION	INDUSTRY VALUE	KEY PARAMETER	SIGNETICS AVAILABLE VALUE	SIGNETICS ORIGINATED DEVICES	QR&A		COMMENTS
					SURE II	SUPR II	
MOTOROLA FAIRCHILD RAYTHEON N.S.C. T.I.	0.5	Slew rate	10 to 600 V/μ sec	NE/SE 530	Yes		
				538	Yes		
				5534	Yes	Yes	
				5534A	Yes	Yes	*Not pin for pin replacement.
				NE 5539*			
	10	Full power out	300 to 350,000 kHz	NE/SE 530	Yes		
				538	Yes		
				5534	Yes	Yes	
				5534A	Yes	Yes	*Not pin for pin replacement.
				NE 5539*			
	45	Noise	4, 5 nv/√Hz	NE/SE 5534	Yes	Yes	
				5534A	Yes	Yes	
	5	Offset voltage	4 mv	NE/SE 5534	Yes	Yes	
				5534A	Yes	Yes	
	500	Bias current	60 to 150 na	NE/SE 530	Yes		
				538	Yes		
	1	Gain bandwidth	1.5 ↓ 1200 MHz	NE/SE 530	Yes		
				538	Yes		
				5534	Yes	Yes	
				5534A	Yes	Yes	*Not pin for pin replacement.
				NE 5539*			
	2,000	Maximum loading	600 OHM	NE/SE 5534	Yes	Yes	
				5534A	Yes	Yes	

HIGH PERFORMANCE JFET INPUT OP AMPS

LF355/356

DESCRIPTION

The LF355 and LF356 operational amplifiers employ well matched, high voltage JFET input structures on the same monolithic chip as bipolar devices. These amplifiers feature low input bias and offset currents, low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time and low noise.

COMMON FEATURES

(TYPICAL)

- **Low input bias current 50pA**
- **Low input offset current 10pA**
- **High input impedance $10^{12}\Omega$**
- **Low input offset voltage 3mV**
- **Low V_{OS} temperature drift 5μV/°C**
- **Low input noise current 0.01pA/$\sqrt{Hz}$**

APPLICATIONS

- **Precision high speed integrators**
- **Fast A/D, D/A converters**
- **High impedance buffers**
- **Wideband, low noise, low drift amplifier**

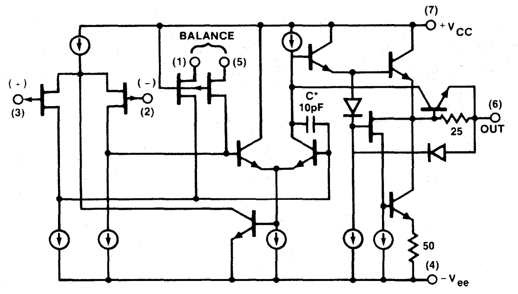
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	±18	V
Power dissipation	500	mW
Operating temperature range	0 to +70	°C
T_j (Max)	100	°C
Input voltage range[1]	±20	V
Output short circuit duration	Continuous	
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 10 sec.)	300	°C

NOTE

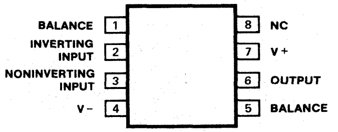
1. Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

EQUIVALENT SCHEMATIC



PIN CONFIGURATION

N PACKAGE

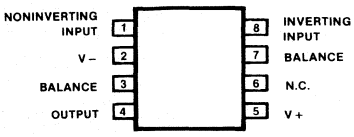


TOP VIEW

ORDER NUMBERS

LF355N LF356N

D PACKAGE

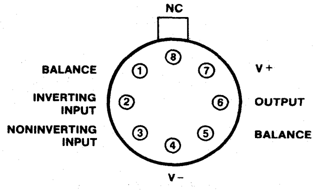


TOP VIEW

ORDER NUMBER

LF356D

H PACKAGE*



TOP VIEW

ORDER NUMBERS

LF355H LF356H

*Metal cans (H) not recommended for new designs

HIGH PERFORMANCE JFET INPUT OP AMPS

LF355/356

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	LF355/356			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S = 50\Omega$		3	10 13	mV mV
$\Delta V_{OS}/\Delta T$	Avg. TC of input offset voltage	$R_S = 50\Omega$		5		$\mu V/°C$
$\Delta TC/\Delta V_{OS}$	Change in average TC[2] with V_{OS} adjust	$R_S = 50\Omega$		0.5		$\mu V/°C$ per mV
I_{OS}	Input offset current[1,3]	$T_J = 25°C$ $T_J \le T_{high}$		3	50 2	pA nA
I_B	Input bias current[1,3]	$T_J = 25°C$ $T_J \le T_{high}$		30	200 8	pA nA
R_{IN}	Input resistance	$T_J = 25°C$		10^{12}		Ω
A_{VOL}	Large signal voltage gain	$V_S = \pm 15V$ $V_O = \pm 10V$, $R_L = 2k\Omega$ Over temp.	25 15	200		V/mV V/mV
V_O	Output voltage swing	$V_S = \pm 15V$, $R_L = 10k\Omega$ $V_S = \pm 15V$, $R_L = 2k\Omega$	±12 ±10	±13 ±12		V V
V_{CM}	Input common mode Voltage range	$V_S = \pm 15V$	±10	+15.1 -12		V V V
CMRR	Common-mode rejection ratio		80	100		dB
PSRR	Supply volt. rej. ratio[4]		80	100		dB

NOTES

1. These specifications apply for $V_S = \pm 15V$ and $0° C \le T_A \le +70°C$. V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.
2. The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5$\mu V/°C$ typically) for each mV of adjustment from its original unadjusted value. Common mode rejection and open loop voltage gain are also unaffected by offset adjustment.
3. The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_j = T_A + \theta_{jA}$ Pd where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
4. Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

PARAMETER	LF355			LF356			UNIT
	Min	Typ	Max	Min	Typ	Max	
Supply current		2	4		5	10	mA

HIGH PERFORMANCE JFET INPUT OP AMPS

LF355/356

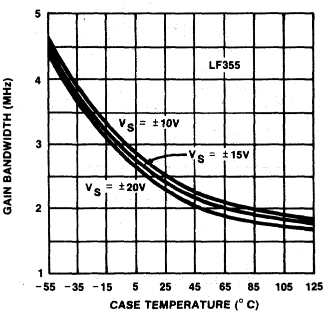
AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.[1]

PARAMETER		TEST CONDITIONS	LF355			LF356			UNIT
			Min	Typ	Max	Min	Typ	Max	
SR	Slew rate	$A_V = 1$		5			12		V/µs
GBW	Gain bandwidth product			2.5			5		MHz
t_s	Settling time[1] to 0.01%			4			1.5		µs
e_n	Equiv. input noise volt.	$R_S = 100\Omega$							
		f = 100Hz		25			15		nV/√Hz
		f = 1000Hz		20			12		nV/√Hz
i_n	Equiv. input noise current	f = 100Hz		0.01			0.01		pA/√Hz
		f = 1000Hz		0.01			0.01		pA/√Hz
C_{IN}	Input capacitance			3			3		pF

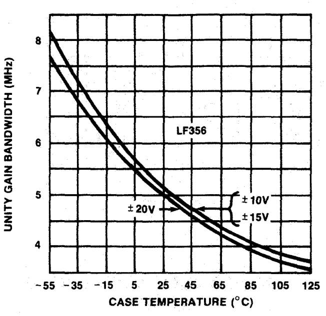
NOTE

1. Settling time is defined here, for a unity gain inverter connection using 2kΩ resistors for the LF355/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter.

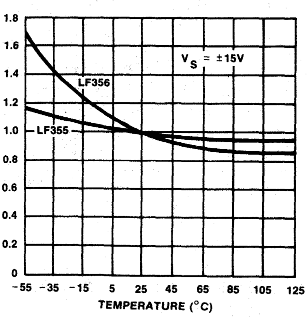
TYPICAL AC PERFORMANCE CHARACTERISTICS



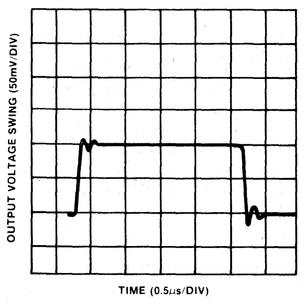
GAIN BANDWIDTH



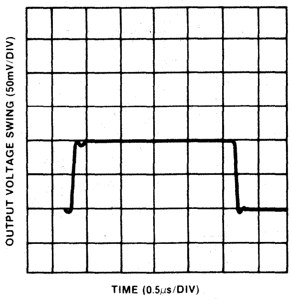
UNITY GAIN BANDWIDTH



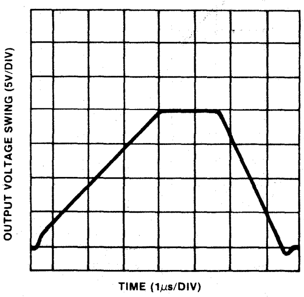
NORMALIZED SLEW RATE



LF355 SMALL SIGNAL PULSE RESPONSE, $A_V = +1$



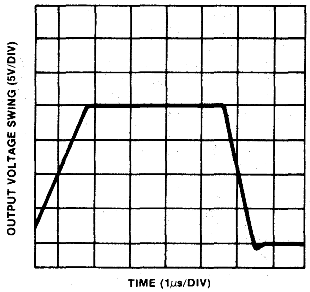
LF356 SMALL SIGNAL PULSE RESPONSE, $A_V = +1$



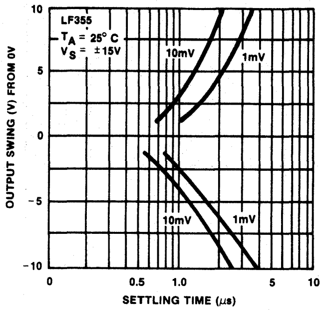
LF355 LARGE SIGNAL PULSE RESPONSE, $A_V = +1$

TYPICAL AC PERFORMANCE CHARACTERISTICS (Cont'd)

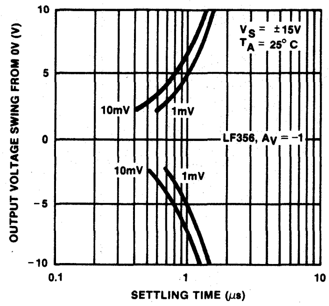
LF356 LARGE SIGNAL PULSE RESPONSE, $A_V = +1$



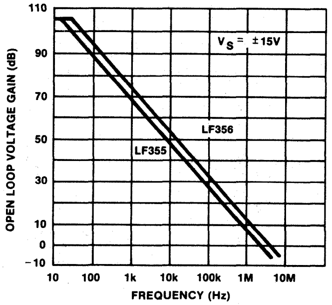
INVERTER SETTLING TIME



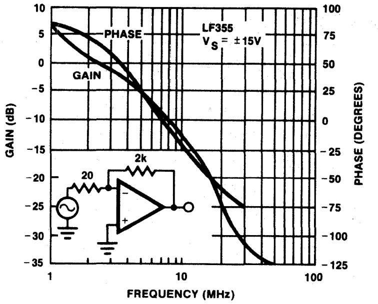
INVERTER SETTLING TIME



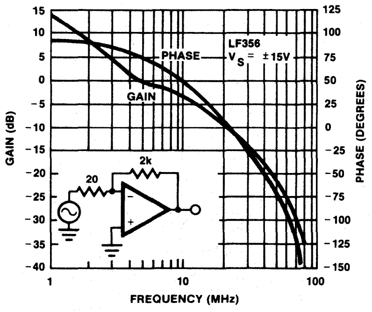
OPEN LOOP FREQUENCY RESPONSE



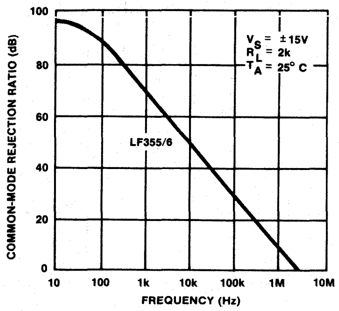
BODE PLOT



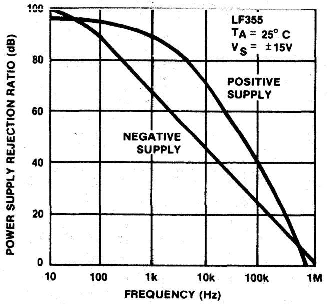
BODE PLOT



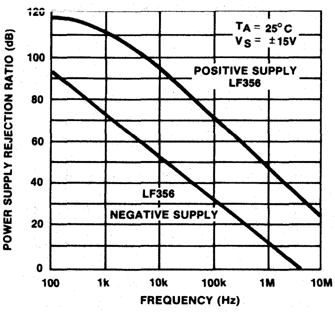
COMMON-MODE REJECTION RATIO



POWER SUPPLY REJECTION RATIO



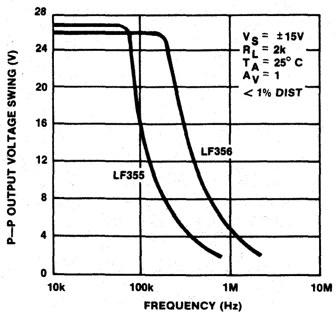
POWER SUPPLY REJECTION RATIO



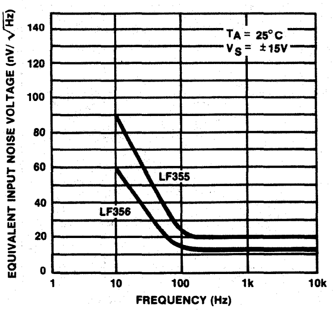
HIGH PERFORMANCE JFET INPUT OP AMPS LF355/356

TYPICAL AC PERFORMANCE CHARACTERISTICS (Cont'd)

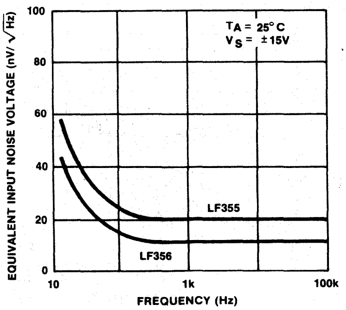
UNDISTORTED OUTPUT VOLTAGE SWING



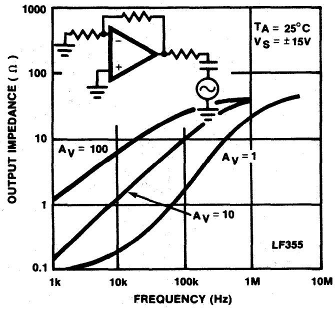
EQUIVALENT INPUT NOISE VOLTAGE



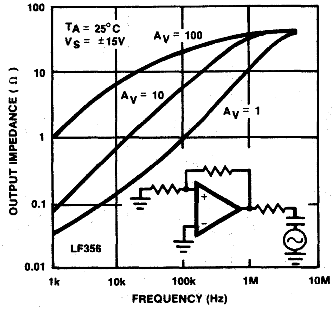
EQUIVALENT INPUT NOISE VOLTAGE (EXPANDED SCALE)



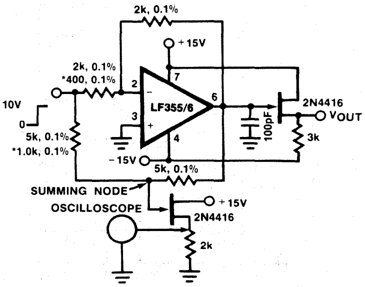
OUTPUT IMPEDANCE



OUTPUT IMPEDANCE



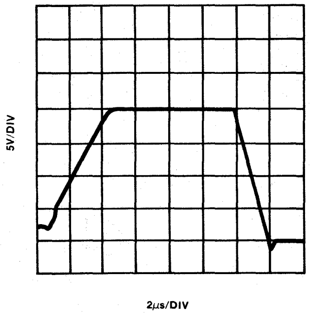
SETTLING TIME TEST CIRCUIT



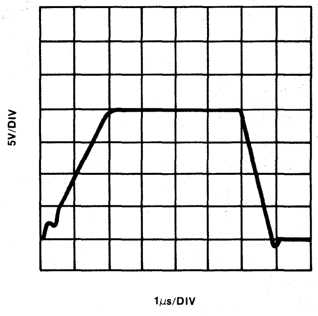
- Settling time is tested with the LF355/6 connected as unity gain inverter,
- FET used to isolate the probe capacitance
- Output = 10V step

LARGE SIGNAL INVERTER OUTPUT, V_{OUT} (FROM SETTLING TIME CIRCUIT)

LF355

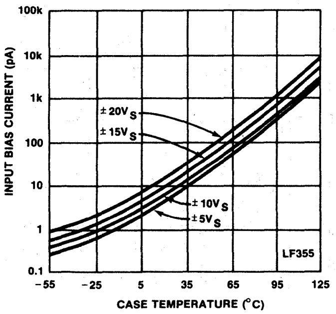


LF356

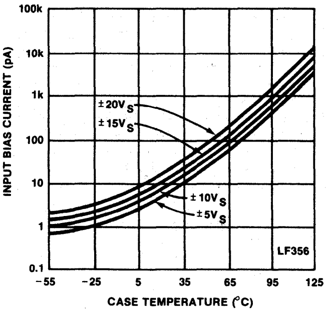


TYPICAL DC PERFORMANCE CHARACTERISTICS

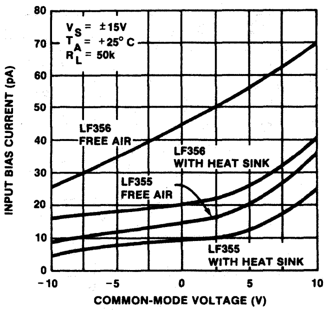
INPUT BIAS CURRENT



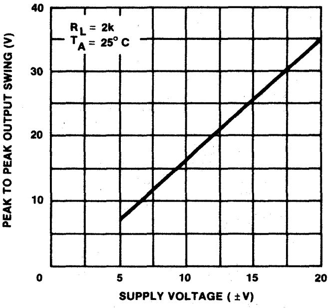
INPUT BIAS CURRENT



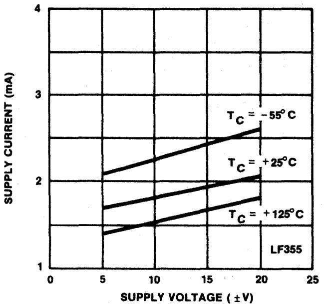
INPUT BIAS CURRENT



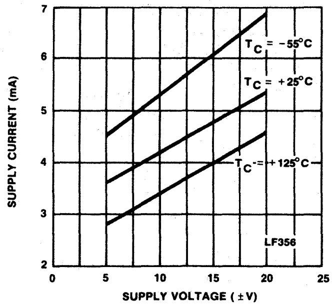
VOLTAGE SWING



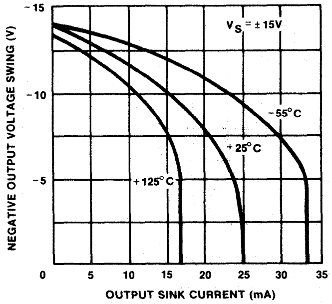
SUPPLY CURRENT



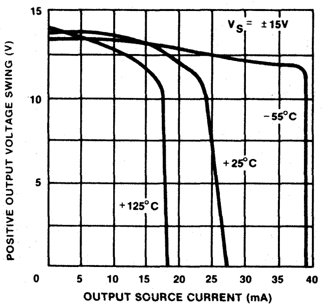
SUPPLY CURRENT



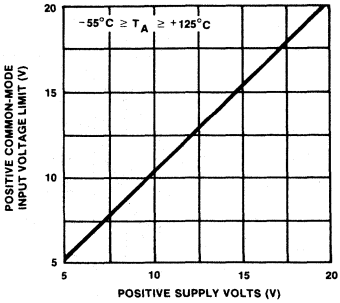
NEGATIVE CURRENT LIMIT



POSITIVE CURRENT LIMIT

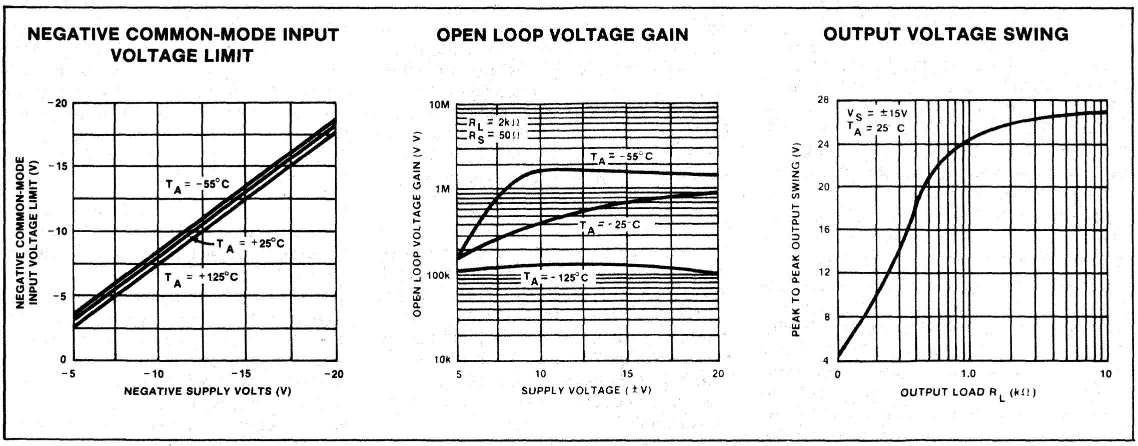


POSITIVE COMMON-MODE INPUT VOLTAGE LIMIT



HIGH PERFORMANCE JFET INPUT OP AMPS LF355/356

TYPICAL DC PERFORMANCE CHARACTERISTICS (Cont'd)



NEGATIVE COMMON-MODE INPUT VOLTAGE LIMIT

OPEN LOOP VOLTAGE GAIN

OUTPUT VOLTAGE SWING

L16

HIGH PERFORMANCE JFET INPUT OP AMPS

LF355/356

APPLICATIONS

The LF355 and LF356 are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

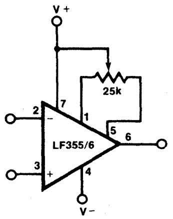
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

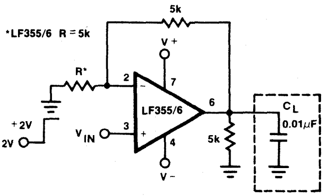
TYPICAL CIRCUIT CONNECTIONS

V_{OS} ADJUSTMENT



- V_{OS} is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V+
- For potentiometers with temperature coefficient of 100ppm/°C or less the additional drift with adjust is ≃ 0.5μV/°C/mV of adjustment
- Typical overall drift: 5μV/°C ± (0.5μV/°C/mV of adj.)

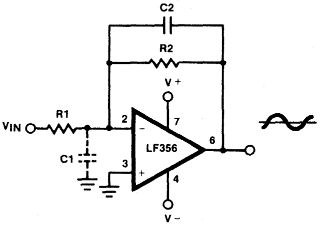
DRIVING CAPACITIVE LOADS



Due to a unique output stage design these amplifiers have the ability to drive large capacitive loads and still maintain stability. C_L max ≤ 0.01μF.
Overshoot ≤ 20%
Setting time (t_S) ≥ 5μs

TYPICAL APPLICATIONS

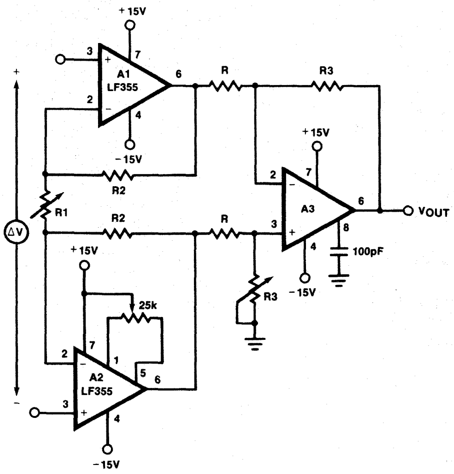
WIDE BW LOW NOISE, LOW DRIFT AMPLIFIER



- Power BW: $f_{MAX} = \frac{S_r}{2\pi/p} \cong 240kHz$
- Parasitic input capacitance C1 ≅ (3pF for LF355 and LF356, plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that: R2C2 ≅ R1C1.

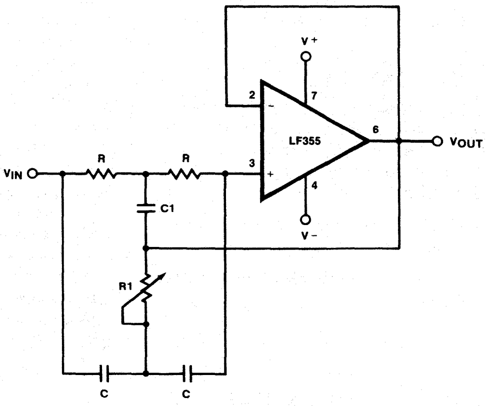
TYPICAL APPLICATIONS (Cont'd)

HIGH IMPEDANCE, LOW DRIFT INSTRUMENTATION AMPLIFIER



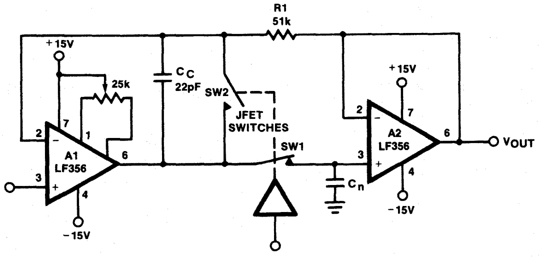
- $V_{OUT} = \frac{R3}{R}\left[\frac{2R2}{R1} + 1\right]\Delta V$, V- +2V ≤ V_{IN} Common-Mode ≤ V+
- System V_{OS} adjusted via A2 V_{OS} adjust
- Trim R3 to boost up CMRR to 120dB.

HIGH Q NOTCH FILTER



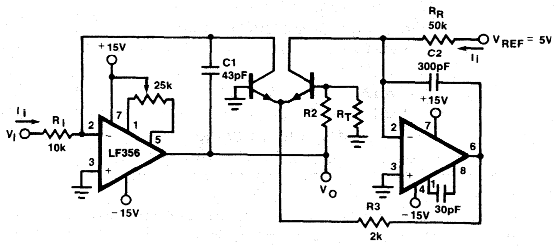
- 2R1 = R = 10MΩ
  2C = C1 = 300pF
- Capacitors should be matched to obtain high Q
- f_{NOTCH} = 120Hz, notch = 55dB, Q > 180
- Use LF355 for
  Δ Low I_B
  Δ Low supply current

HIGH ACCURACY SAMPLE AND HOLD



- By closing the loop through A2 the V_{OUT} accuracy will be determined uniquely by A1. No V_{OS} adjust required for A2.
- T_A can be estimated by same considerations as previously but, because of the added on propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold.
- R1, C_C: additional compensation
- Use LF356 for
  Δ Fast settling time
  Δ Low V_{OS}

FAST LOGARITHMIC CONVERTER



$$|V_{OUT}| = \left[1 + \frac{R2}{R}\right]\frac{kT}{q} \ln V_I\left[\frac{R_r}{V_{REF}\, R_i}\right] = \log V_I \frac{1}{R_i\, I_R}$$

R2 = 15.71, R_1 = 1k, 0.3%°C (for temperature compensation)

- Dynamic range: 100μA ≤ I_i ≤ 1mA (5 decades, $|V_O|$ = 1V/decades)
- Transient response: 3μs for Δ, = decades
- C1, C2, R2, R3: added dynamic compensation
- V_{OS} adjust the LF356 to minimize quiescent error
- R_T: Tel Labs type Q81 + 0.3%/°C.

GENERAL PURPOSE SINGLE SUPPLY OP AMP LM124/224/324/SA534

DESCRIPTION

The LM124/SA534 series consists of four independent, high gain, internally frequency compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages.

UNIQUE FEATURES

In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

The unity gain cross frequency is temperature compensated.

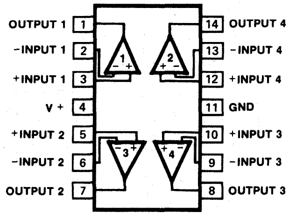
The input bias current is also temperature compensated.

FEATURES

- **Internally frequency compensated for unity gain**
- **Large dc voltage gain—(100dB)**
- **Wide bandwidth (unity gain)—1MHz (temperature compensated)**
- **Wide power supply range**
  Single supply—(3Vdc to 30Vdc) or dual supplies—(±1.5Vdc to ±15Vdc)
- **Very low supply current drain—essentially independent of supply voltage (1mW/op amp at +5Vdc)**
- **Low input biasing current—(45nAdc temperature compensated)**
- **Low input offset voltage—(2mVdc) and offset current—(5nAdc)**
- **Differential input voltage range equal to the power supply voltage**
- **Large output voltage—(0Vdc to V+—1.5Vdc swing)**
- **LM124 Mil std 883A,B,C available**

PIN CONFIGURATION

D,F,N PACKAGE



TOP VIEW

ORDER NUMBERS

LM124N	LM224N	LM324N
LM124F	LM224F	LM324F
SA534N	SA534F	LM324D

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V+	Supply voltage	32 or ±16	Vdc
	Differential input voltage	32	Vdc
	Input voltage	-0.3 to +32	Vdc
	Power dissipation[1]		
	N package	570	mW
	F package	900	mW
	Output short-circuit to GND		
	1 amplifier[2]	Continuous	
	V+ < 15Vdc and T_A = 25°C		
	Input current (V_{IN} < -0.3V)[3]	50	mA
	Operating temperature range		
	LM324	0 to +70	°C
	LM224	-25 to +85	°C
	SA534	-40 to +85	°C
	LM124	-55 to +125	°C
	Storage temperature range	-65 to +150	°C
	Lead temperature (soldering, 10sec)	300	°C

NOTES

1. For operating at high temperatures, all devices must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. LM 124/224 can be derated based on a +150°C maximum junction temperature.
2. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of +15Vdc continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.
3. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading change exists on the input lines.

GENERAL PURPOSE SINGLE SUPPLY OP AMP

LM124/224/324/SA534

DC ELECTRICAL CHARACTERISTICS

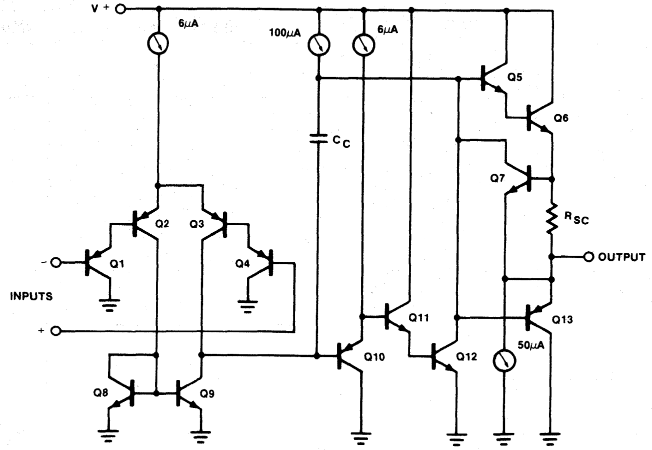
$V+ = 5V$, $T_A = 25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	LM124/LM224			LM324/SA534			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage[1]	$R_S = 0\Omega$		±2	±5		±2	±7	mV
		$R_S = 0\Omega$, over temp.			±7			±9	mV
V_{OS}	Drift	$R_S = 0\Omega$		7			7		μV/°C
I_{BIAS}	Input current[2]	$I_{IN}(+)$ or $I_{IN}(-)$		45	150		45	250	nA
		$I_{IN}(+)$ or $I_{IN}(-)$, over temp.		40	300		40	500	nA
I_{OS}	Offset current	$I_{IN}(+) - I_{IN}(-)$		±3	±30		±5	±50	nA
		$I_{IN}(+) - I_{IN}(-)$, over temp.			±100			±150	nA
I_{OS}	Drift			10			10		pA/°C
V_{CM}	Common mode voltage range[3]	$V+ = 30V$	0		$V+-1.5$	0		$V+-1.5$	V
		$V+ = 30V$, over temp.	0		$V+-2$	0		$V+-2$	V
C_{MRR}	Common mode rejection ratio		70	85		65	70		dB
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$, $V+ = +30V$, over temp.	26			26			V
V_{OH}		$R_L \leq 10k\Omega$, over temp.	27	28		27	28		V
V_{OL}		$R_L \leq 10k\Omega$, $V+ = 5V$, over temp.		5	20		5	20	mV
I_{CC}	Supply current	$R_L = \infty$, $V_{CC} = 30V$, over temp.		1.5	3		1.5	3	mA
		$R_L = \infty$, on all op amps, over temp.		0.7	1.2		0.7	1.2	
A_{VOL}	Large signal voltage gain	$V+ = +15V$ (for large V_O swing), $R_L \geq 2k\Omega$	50	100		25	100		V/mV
		$V+ = +15V$ (for large V_O swing), $R_L \geq 2k\Omega$, over temp.	25			15			V/mV
	Amplifier-to-amplifier coupling[5]	f = 1kHz to 20kHz, input referred		−120			−120		dB
PSRR		$R_S \leq 0\Omega$	65	100		65	100		dB
	Output current								
	Source	$V_{IN}+ = +1Vdc$, $V_{IN}- = 0Vdc$, $V+ = 15Vdc$	20	40		20	40		mA
		$V_{IN}+ = +1Vdc$, $V_{IN}+ = 0Vdc$, $V+ = 15Vdc$, over temp.	10	20		10	20		mA
	Sink	$V_{IN}- = +1Vdc$, $V_{IN}+ = 0Vdc$, $V+ = 15Vdc$	10	20		10	20		mA
		$V_{IN}- = +1Vdc$, $V_{IN}+ = 0Vdc$, $V+ = 15Vdc$, over temp.	5	8		5	8		mA
		$V_{IN}+ = 0Vdc$, $V_{IN}- = +1Vdc$, $V_O = 200mV$	12	50		12	50		μA
I_{SC}	Short circuit current[4]			40	60		40	60	mA
	Differential input voltage[6]				V+			V+	V

NOTES

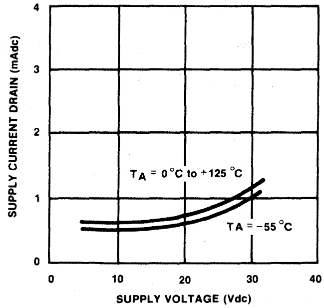
1. $V_O \cong 1.4Vdc$, $R_S = 0\Omega$ with V+ from 5V to 30V and over full input common mode range (0Vdc+ to V+ −1.5V).
2. The direction of the input current is out of the IC due to the pnp input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ −1.5, but either or both inputs can go to +32V without damage.
4. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of +15Vdc continous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
5. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ −1.5V, but either or both inputs can go to +32Vdc without damage.

EQUIVALENT SCHEMATIC

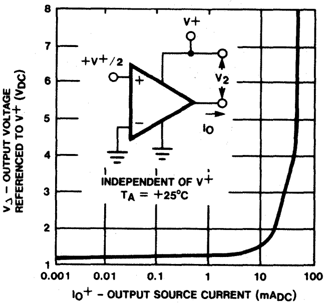


TYPICAL PERFORMANCE CHARACTERISTICS

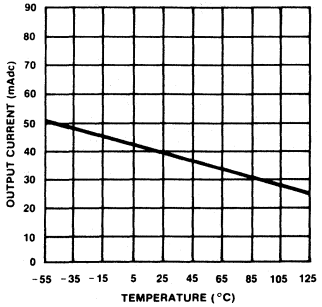
SUPPLY CURRENT



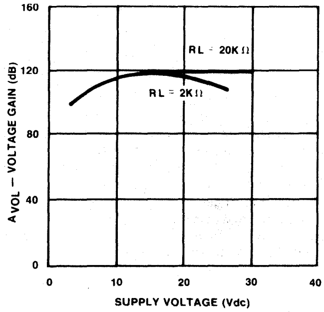
OUTPUT CHARACTERISTICS CURRENT SOURCING



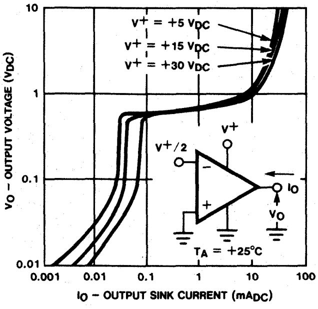
CURRENT LIMITING



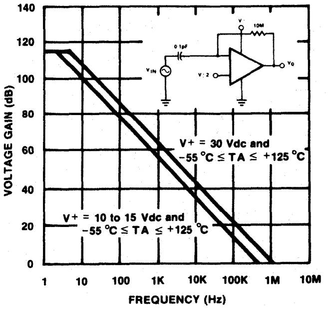
VOLTAGE GAIN



OUTPUT CHARACTERISTICS CURRENT SINKING



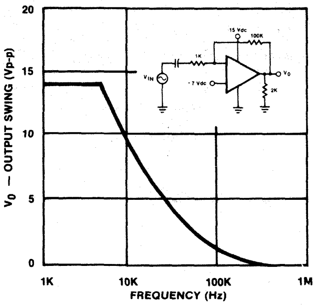
OPEN LOOP FREQUENCY RESPONSE



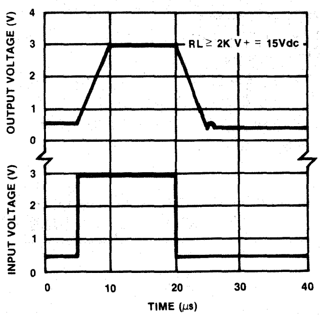
GENERAL PURPOSE SINGLE SUPPLY OP AMP LM124/224/324/SA534

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

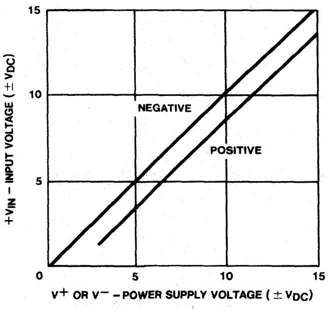
LARGE SIGNAL FREQUENCY RESPONSE



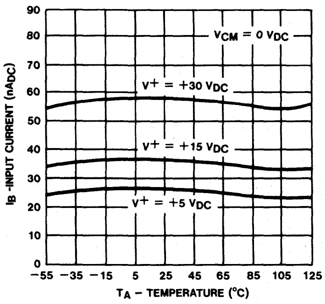
VOLTAGE FOLLOWER PULSE RESPONSE



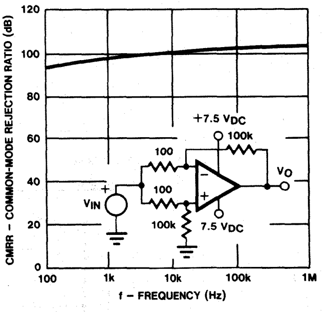
INPUT VOLTAGE RANGE



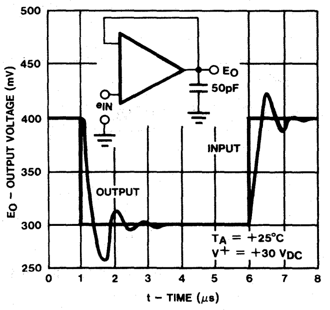
INPUT CURRENT



COMMON MODE REJECTION RATIO



VOLTAGE FOLLOWER PULSE RESPONSE (SMALL SIGNAL)



ANALOG DIVISION MARCH 1982

HIGH PERFORMANCE AMPLIFIER LM301A

DESCRIPTION

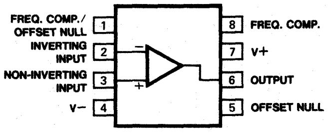
The LM301A is a high performance operational amplifier featuring high gain, short circuit protection, simplified compensation and excellent temperature stability.

FEATURES

- **Short circuit protection**
- **Offset voltage null capability**
- **Large common-mode and differential voltage ranges**
- **Low power consumption**
- **No latch up**
- **LM101, LM101A, LH2101, LH2101A Mil std 883A,B,C available**
- **LM101A, LH2101A MIL-STD-38510 (JAN) available**

PIN CONFIGURATIONS

D,N,FE PACKAGE



TOP VIEW

ORDER NUMBERS

LM301AN
LM301AFE
LM301AD

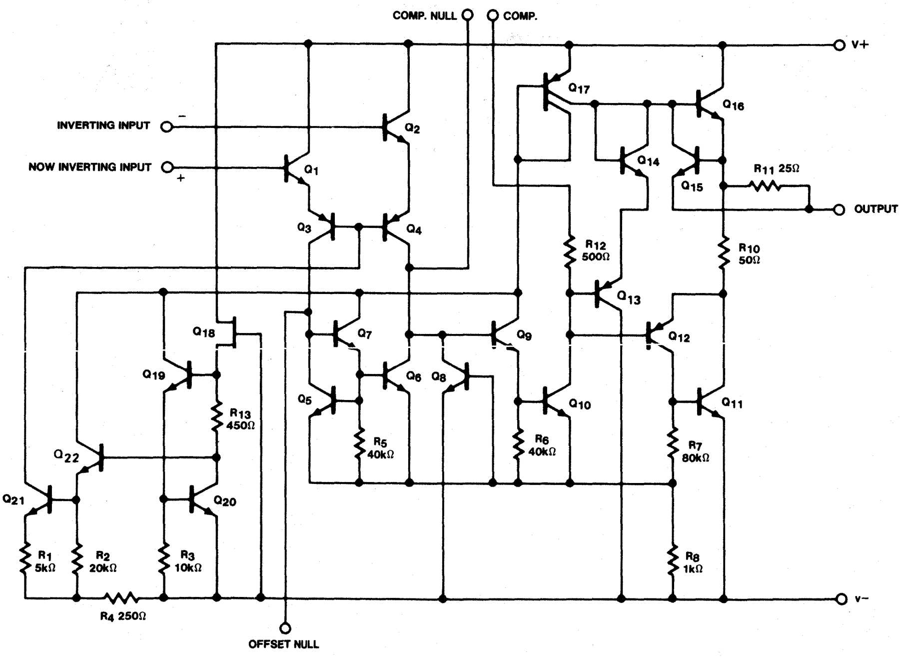
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply Voltage		
LM301A	±18	V
Power dissipation	500	mW
Differential input voltage	±30	V
Input voltage[1]	±15	V
Output short circuit duration	Indefinite	
Operating temperature range		
LM301A	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 60sec)	300	°C

NOTES

1. For supply voltages less then ±15V, the absolute maximum input voltage is equal to the supply voltage.

EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS $0^\circ C \le T_A < 70^\circ C$, ±5V, $\le V_S \le$ ±15V and $C_1 = 30pF$

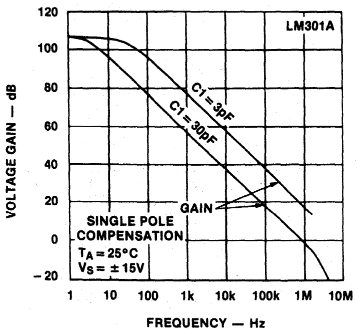
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Input Offset Voltage	$T_A = 25^\circ C$, $R_S < 50K\Omega$		2.0	7.5	mV
I_{OS}	Input Offset Current	$T_A = 25^\circ C$		3	50	nA
I_{BIAS}	Input Bias Current	$T_A = 25^\circ C$		70	250	nA
I_{OS}	Input Resistance	$T_A = 25^\circ C$	0.5	2		MΩ
I_{CC}	Supply Current	$T_A = 25^\circ C$, $V_S = \pm 15V$		1.8	3.0	mA
A_{VOL}	Large Signal Voltage Gain	$T_A = 25^\circ C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$; $R_L > 2k\Omega$	25	160		V/mV
V_{OS}	Input Offset Voltage	$R_S < 50k\Omega$			10	mV
V_{OS}	Average Temperature Coefficient of Input Drift Offset Voltage			6.0	30	μV/°C
I_{OS}	Input Offset Current				70	nA
I_{OS}	Average Temperature Coefficient of Input Offset Current	$25^\circ C < T_A < 70^\circ C$ $0^\circ C < T_A < 25^\circ C$		0.01 0.02	0.3 0.6	nA/°C nA/°C
I_{BIAS}	Input Bias Current				300	nA
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L > 2k\Omega$	15			V/mV
V_{OUT}	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k\Omega$ $R_L = 2k\Omega$	±12 ±10	±14 ±13		V V
V_{IN}	Input Voltage Range	$V_S = \pm 15V$	±12			V
C_{MRR}	Common Mode Rejection Ratio	$R_S < 50k\Omega$	70	90		dB
P_{SRR}	Supply Voltage Rejection Ratio	$R_S < 50k\Omega$	70	96		dB

*NOTE

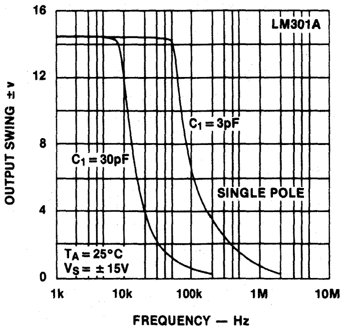
Unless otherwise specified, all specifications for LM301A are ±5V ≤ V_S ≤ ±15V.

TYPICAL PERFORMANCE CHARACTERISTICS

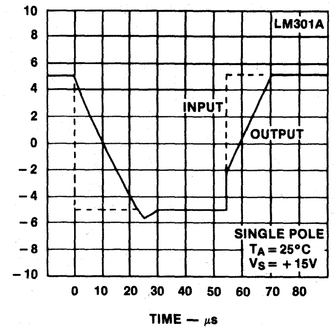
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE

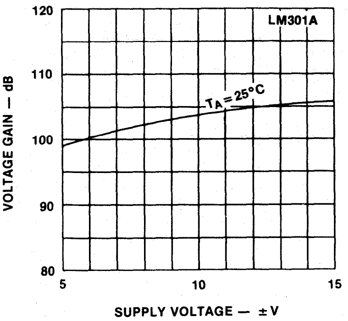


VOLTAGE FOLLOWER PULSE RESPONSE

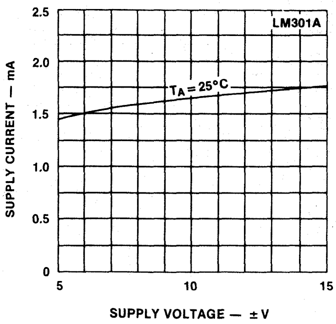


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

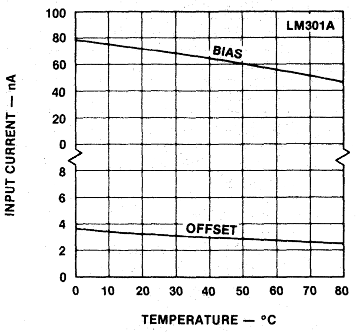
VOLTAGE GAIN



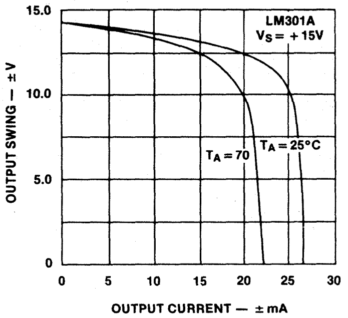
SUPPLY CURRENT



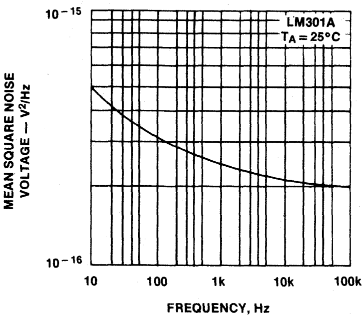
INPUT CURRENT



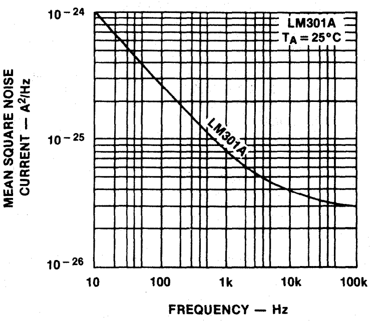
CURRENT LIMITING



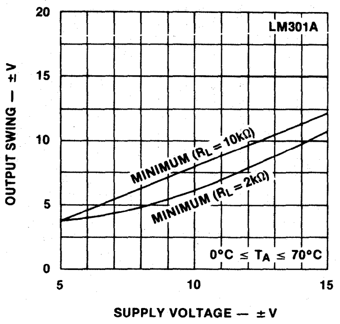
INPUT NOISE VOLTAGE



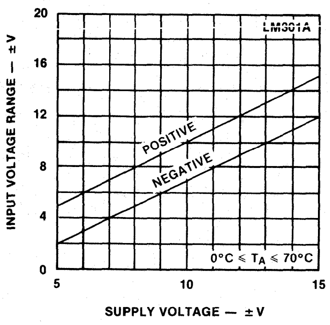
INPUT NOISE CURRENT



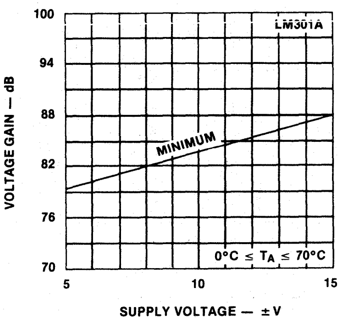
OUTPUT SWING



INPUT VOLTAGE RANGE



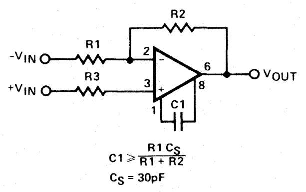
VOLTAGE GAIN



HIGH PERFORMANCE AMPLIFIER LM301A

COMPENSATION CIRCUITS

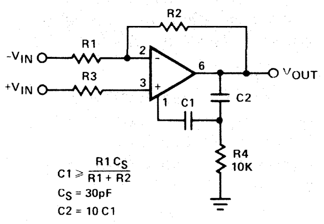
SINGLE POLE COMPENSATION



$C1 \geq \frac{R1\,C_S}{R1 + R2}$

$C_S = 30pF$

TWO POLE COMPENSATION

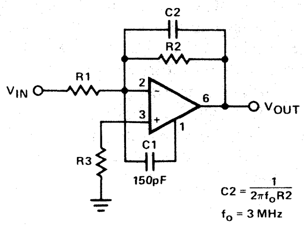


$C1 \geq \frac{R1\,C_S}{R1 + R2}$

$C_S = 30pF$

$C2 = 10\,C1$

FEED FORWARD COMPENSATION

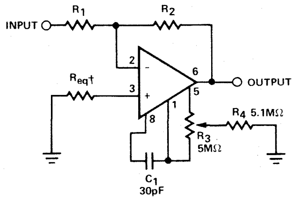


$C2 = \frac{1}{2\pi f_o R2}$

$f_o = 3\,MHz$

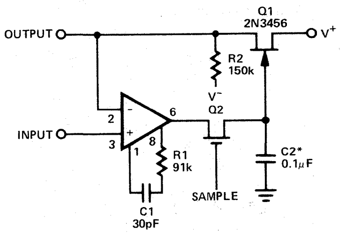
TYPICAL APPLICATIONS

INVERTING AMPLIFIER WITH BALANCING CIRCUIT



†May be zero or equal to parallel combination of R_1 and R_2 for minimum offset.

LOW DRIFT SAMPLE AND HOLD



*Polycarbonate Dielectric Capacitor

OPERATIONAL TRANSCONDUCTANCE AMPLIFIERS LM13600/13600A

DESCRIPTION

The LM13600 series consists of two current controlled transconductance amplifiers each with differential inputs and a push pull output. The two amplifiers share common supplies but otherwise operate independently. Linearizing diodes are provided at the inputs to reduce distortion and allow higher input levels. The result is a 10 dB signal-to-noise improvement referenced to 0.5 percent THD. Controlled impedance buffers are provided which are specifically designed to complement the dynamic range of the amplifiers.

FEATURES

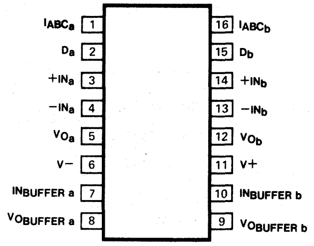
- **gm adjustable over 6 decades**
- **Excellent gm linearity**
- **Excellent matching between amplifiers**
- **Linearizing diodes**
- **Controlled impedance buffers**
- **High output signal to noise ratio**
- **Wide supply range ±2V to ±22V.**

APPLICATIONS

- **Current controlled amplifiers**
- **Current controlled impedances**
- **Current controlled filters**
- **Current controlled oscillators**
- **Multiplexers**
- **Timers**
- **Sample and hold circuits**

PIN DESCRIPTION

D,N PACKAGE



TOP VIEW

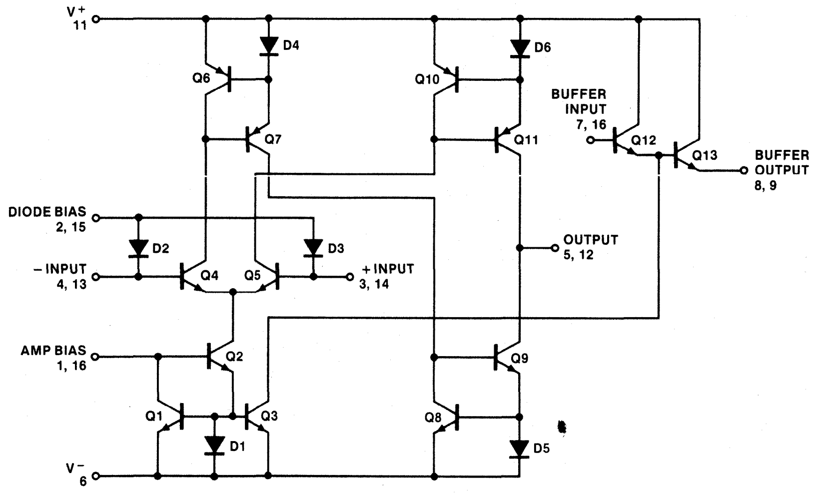
ORDER NUMBERS
LM13600N LM13600D
LM13600AN

NOTE
See Signetics NE5517 for typical circuit applications information.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage[1]		
LM13600	36 V_{DC} or ±18	V
LM13600A	44 V_{DC} or ±22	V
Power dissipation[2] $T_A = 25°C$		
LM13600N, LM13600AN	570	mW
Differential input voltage	±5	V
Diode bias current (I_D)	2	mA
Amplifier bias current (I_{ABC})	2	mA
Output short circuit duration	Indefinite	
Buffer output current[3]	20	mA
Operating temperature range		
LM13600N, LM13600AN	0°C to +70	°C
DC input voltage	$+V_S$ to $-V_S$	
Storage temperature range	−65°C to +150	°C
Lead temperature (Soldering, 10 Seconds)	300	°C

BLOCK DIAGRAM



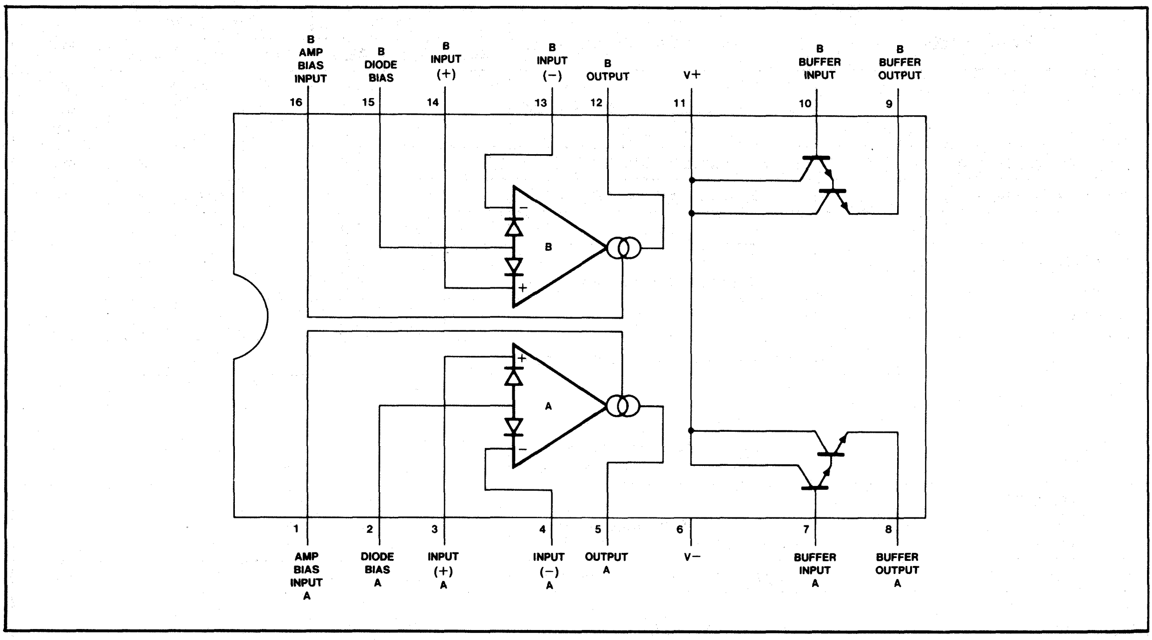
ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	LM13600			LM13600A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage (V_{OS})			0.4	5		0.4	2	mV
	Over specified temperature range						5	mV
	I_{ABC} 5μA		0.3	5		0.3	2	mV
V_{OS} including diodes	Diode Bias Current (I_D) = 500 μA		0.5	5		0.5	2	mV
Input offset change	5 μA ≤ I_{ABC} ≤ 500 μA		0.1			0.1	3	mV
Input offset current			0.1	0.6		0.1	0.6	μA
Input bias current			0.4	5		0.4	5	μA
	Over specified temperature range		1	8		1	7	μA
Forward Transconductance (gm)		6700	9600	13000	7700	9600	12000	μmho
	Over specified temperature range	5400			4000			μmho
gm tracking			0.3			0.3		dB
Peak output current	RL = 0, I_{ABC} = 5μA		5		3	5	7	μA
	RL = 0, I_{ABC} = 500 μA	350	500	650	350	500	650	μA
	RL = 0, Over specified temp range	300			300			μA
Peak output voltage								
positive	RL = ∞, 5 μA ≤ I_{ABC} ≤ 500 μA	+12	+14.2		+12	+14.2		V
negative	RL = ∞, 5 μA ≤ I_{ABC} ≤ 500 μA	−12	−14.4		−12	−14.4		V
Supply current	I_{ABC} = 500 μA, Both channels		2.6			2.6		mA
V_{OS} sensitivity								
positive	$\Delta V_{OS}/\Delta V+$		20	150		20	150	μV/V
negative	$\Delta V_{OS}/\Delta V-$		20	150		20	150	μV/V
CMRR		80	110		80	110		dB
Common mode range		±12	±13.5		±12	±13.5		V
Crosstalk	Referred to input[5] 20 Hz < f < 20 KHz		100			100		dB
Diff. input current	I_{ABC} = 0, Input = ±4V		0.02	100		0.02	10	nA
Leakage current	I_{ABC} = 0 (Refer to test circuit)		0.2	100		0.2	5	nA
Input resistance		10	26		10	26		KΩ
Open loop bandwith			2			2		MHz
Slew rate	Unity gain compensated		50			50		V/μSec
Buff. input current	5		0.4	5		0.4	5	μA
Peak buffer output voltage	5	10			10			V

NOTES
1. For selections to a supply voltage above ±22V, contact factory.
2. For operating at high temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 175° C/W which applies for the device soldered in a printed circuit board, operating in still air.
3. Buffer output current should be limited so as to not exceed package dissipation.
4. These specifications apply for V_S = ± 15V, T_A = 25°C, amplifier bias current (I_{ABC}) = 500μA, pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.
5. These specifications apply for V_S = ± 15V, I_{ABC} = 500 μA, R_{OUT} = 5Ω connected from the buffer output to $-V_S$ and the input of the buffer is connected to the transconductance amplifier output.

OPERATIONAL TRANSCONDUCTANCE AMPLIFIERS LM13600/13600A

CONNECTION DIAGRAM



ANALOG DIVISION

MARCH 1982

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

MC1456/1556

DESCRIPTION

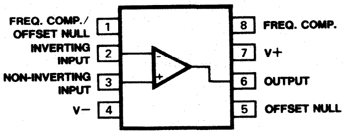
The MC1456/1556 is an internally compensated precision monolithic operational amplifier featuring extremely low offset and bias currents and offset null capability. The MC1456/1556 is short circuit protected and its high common mode and differential input voltage range provides exceptional performance when used as an integrator, summing amplifier, and voltage follower.

FEATURES

- **Low input bias current—15nA maximum**
- **Low input offset current—2.0nA maximum**
- **Low input offset voltage—4.0mV maximum**
- **High slew rate—2.5V/μs typical**
- **Large power bandwidth—40kHz typical**
- **Low power consumption—45mW maximum**
- **Offset voltage null capability**
- **Output short circuit protection**
- **Input over-voltage protection**
- **MIL-STD-883A,B,C available**

PIN CONFIGURATION

N PACKAGE



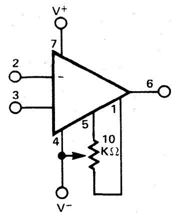
TOP VIEW

ORDER NUMBERS
MC1456N
MC1556N

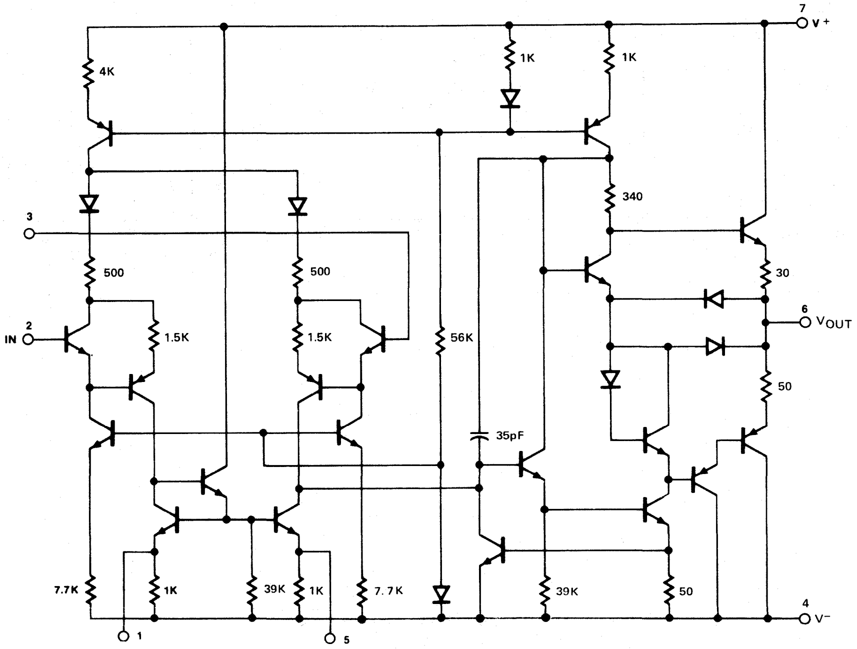
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Power supply voltage MC1556	±22	V
MC1456	±18	V
Differential input voltage	± V_{CC}	V
Common mode input voltage	± V_{CC}	V
Load current	20	mA
Output short circuit duration	Continuous	
Power dissipation	680	mW
Derate above T_A = 25°C	4.6	mW/°C
Operating temperature range		
MC1556	-55 to +125	°C
MC1456	0 to +70	°C
Storage temperature range	-65 to +150	°C

OFFSET ADJUST CIRCUIT



EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified

PARAMETER	TEST CONDITIONS	MC1556			MC1456			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OS} Offset voltage			2.0	4.0		5.0	10.0	mVdc
	Over temperature			6.0			14.0	mVdc
I_{OS} Offset current			1.0	2.0		5.0	10.0	nA
	$0°C \leq T_A \leq 70°C$						14	nA
	$25°C \leq T_A \leq 125°C$			3.0				nA
	$-55°C \leq T_A \leq 25°C$			5.0				nA
I_{BIAS} Input current			8.0	15		15.0	30.0	nA
	Over temperature			30			40	nA
V_{CM} Common mode voltage range		±12	±13		±11	±12		V
CMRR Common mode rejection ratio	$R_S \leq 10k\Omega$, $T_A = 25°C$, $f = 100Hz$	80	110		70	110		dB
Z_{IN} Common mode input impedance	$f = 20Hz$		250			250		MΩ
V_{OUT} Output voltage swing	$R_L = 2k\Omega$	±12	±13		±11	±12		V
I_{CC} Supply current			1.0	1.5		1.3	3.0	mA
P_D DC quiescent power dissipation ($V_O = 0$)			30	45		40	90	mW
PSRR Supply voltage rejection ratio	$R_S \leq 10k\Omega$		50	100		75	200	μV/V
Large signal voltage gain	$R_L \leq 2k\Omega$, $V_{OUT} = \pm 10V$, $T_A = 25°C$	100	200		70	100		V/mV
	Over temperature	40			40			V/mV

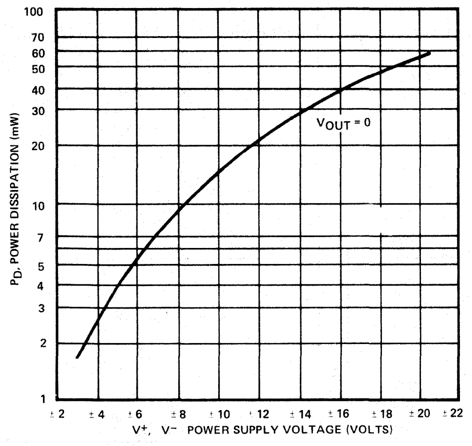
AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	MC1556			MC1456			UNIT
		Min	Typ	Max	Min	Typ	Max	
Differential input impedance								
c_p Parallel input capacitance	Open loop $f = 20Hz$		6.0			6.0		pF
r_p Parallel input resistance			5			3		MΩ
e_n Equivalent input noise voltage	$A_V = 100$, $R_S = 10k\Omega$, $f = 1.0kHz$, $BW = 1.0kHz$		45			45		$nV/\sqrt{Hz}$
BW_p Power bandwidth	$A_V = 1$, $R_L = 2k\Omega$, $THD \leq 5\%$ $V_{OUT} = \pm 10V$		40			40		kHz
Phase margin (open loop, unity gain)			70			70		degrees
Gain margin			18			18		dB
S_R Slew rate (unity gain)			2.5			2.5		V/μsec
Z_{OUT} Output impedance	$f = 20Hz$		1.0	2.0		1.0	2.5	kΩ
BW Unity gain crossover frequency (open loop)			1.0			1.0		MHz

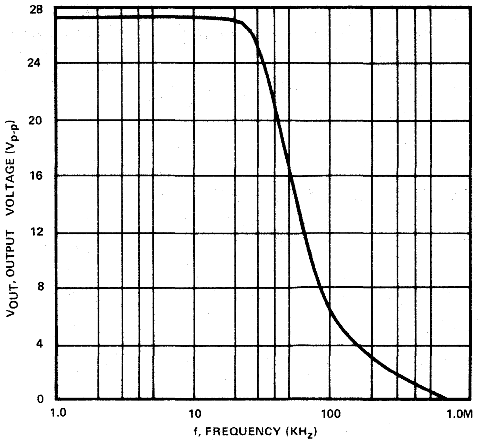
HIGH PERFORMANCE OPERATIONAL AMPLIFIER MC1456/1556

TYPICAL PERFORMANCE CHARACTERISTICS

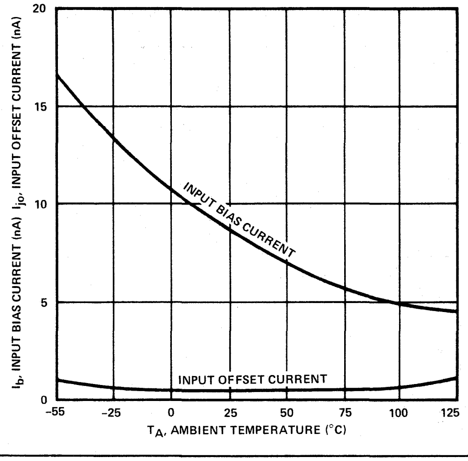
POWER DISSIPATION vs POWER SUPPLY VOLTAGE



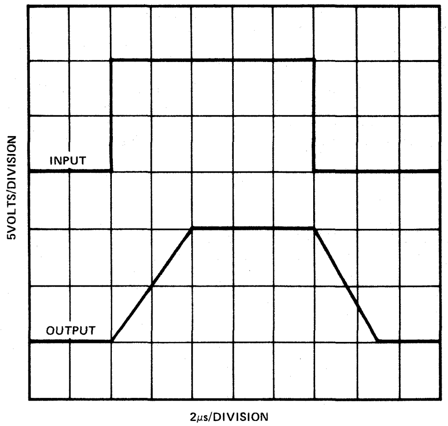
POWER BANDWIDTH



TYPICAL INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs TEMPERATURE FOR MC1556



VOLTAGE FOLLOWER PULSE RESPONSE



GENERAL PURPOSE OPERATIONAL AMPLIFIER MC/SA1458/MC1558

DESCRIPTION

The MC1458 is a high performance operational amplifier with high open loop gain, internal compensation, high common mode range and exceptional temperature stability. The MC1458 is short-circuit protected and allows for nulling of offset voltage.

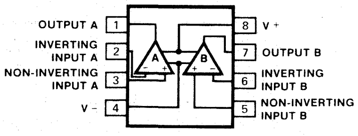
The MC1458/SA1458/MC1558 consists of a pair of 741 operational amplifiers on a single chip.

FEATURES

- **Internal frequency compensation**
- **Short circuit protection**
- **Excellent temperature stability**
- **High input voltage range**
- **No latch-up**
- **1558/1458 are 2 "op amps" in space of one 741 package**
- **MC1558 MIL-STD-883A,B,C available**

PIN CONFIGURATIONS

D,N,FE PACKAGE

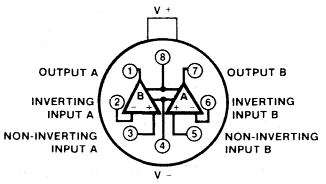


TOP VIEW

ORDER NUMBERS

MC1458N	MC1458FE
MC1558N	MC1558FE
SA1458N	MC1458D

H PACKAGE*



ORDER NUMBERS
MC1458H
MC1558H

*Metal cans (H) not recommended for new designs

ABSOLUTE MAXIMUM RATINGS

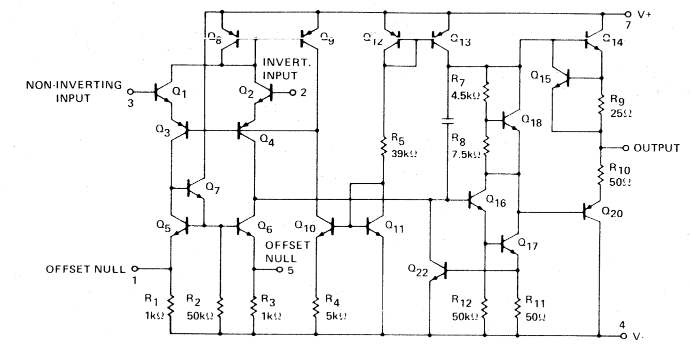
PARAMETER	RATING	UNIT
Supply voltage		
MC1458	±18	V
SA1458	±18	V
MC1558	±22	V
Internal power dissipation		
N package	500	mW
H package[1]	800	mW
F,FE package	1000	mW
Differential input voltage	±30	V
Input voltage[2]	±15	V
Output short-circuit duration	Continuous	
Operating temperature range		
MC1458	0 to +70	°C
SA1458	-40 to +85	°C
MC1558	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 60sec)	300	°C

NOTES

1. Ratings based on thermal resistances, junction to ambient, of 240°C/W, 150°C/W, 110°C/W for N, H, F and FE packages respectively, and a maximum junction temperature of 150°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

EQUIVALENT SCHEMATIC

ONE AMPLIFIER OF MC1458, SA1458, MC1558



DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm15V$, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MC1558			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage	$R_S = 10k\Omega$ $R_S = 10k\Omega$, over temp.		1.0	5.0 6.0	mV mV
I_{OS}	Offset current	 Over temp.		20	200 500	nA nA
I_{BIAS}	Input bias current	 Over temp.		80	500 1500	nA nA
V_{OUT}	Output voltage swing	$R_L = 10k\Omega$, over temp. $R_L = 2k\Omega$, over temp.	±12 ±10	±14 ±13		V V
A_{VOL}	Large signal voltage gain	$R_L = 2k\Omega$, $V_O = \pm10V$ $R_L = 2k\Omega$, $V_O = \pm10V$, over temp.	50 20	100		V/mV V/mV
	Offset voltage adjustment range			±30		mV
PSRR	Supply voltage rejection ratio	$R_S \leq 10k\Omega$		30	150	μV/V
CMRR	Common mode rejection ratio		70	90		dB
I_{CC}	Supply current			2.3	5.0	mA
V_{IN}	Input voltage range		±12	±13		V
P_d	Power consumption			70	150	mW
	Channel separation			120		dB
R_{OUT}	Output resistance			75		Ω
I_{SC}	Output short-circuit current			25		mA

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$, $V_S = \pm15V$, unless otherwise specified.

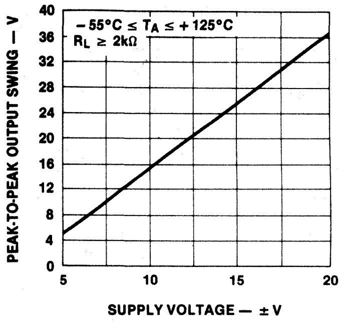
PARAMETER		TEST CONDITIONS	MC1458			SA1458			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S = 10k\Omega$ $R_S = 10k\Omega$, over temp.		2.0	6.0 7.5		2.0	6.0 7.5	mV mV
I_{OS}	Offset current	 Over temp.		20	200 300		20	200 500	nA nA
I_{BIAS}	Input bias current	 Over temp.		80	500 800		80	500 1500	nA nA
V_{OUT}	Output voltage swing	$R_L = 10k\Omega$ $R_L = 2k\Omega$, over temp.	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
A_{VOL}	Large signal voltage gain	$R_L = 2k\Omega$, $V_O = \pm10V$ $R_L = 2k\Omega$, $V_O = \pm10V$, over temp.	25 15	200		20 15	200		V/mV V/mV
	Offset voltage adjustment range			±30			±30		mV
PSRR	Supply voltage rejection ratio	$R_S \leq 10k\Omega$		30	150		30	150	μV/V
CMRR	Common mode rejection ratio		70	90		70	90		dB
I_{CC}	Supply current			2.3	5.6		2.3	5.6	mA
V_{IN}	Input voltage range		±12	±13		±12	±13		V
R_{IN}	Input resistance								MΩ
P_d	Power consumption			70	170		70	170	mW
	Channel separation			120			120		dB
I_{SC}	Output short-circuit current			25			25		mA

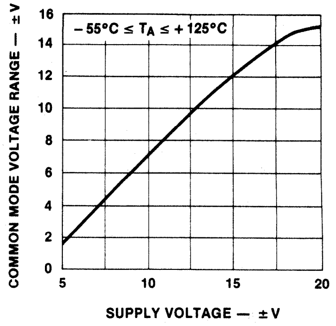
GENERAL PURPOSE OPERATIONAL AMPLIFIER MC/SA1458/MC1558

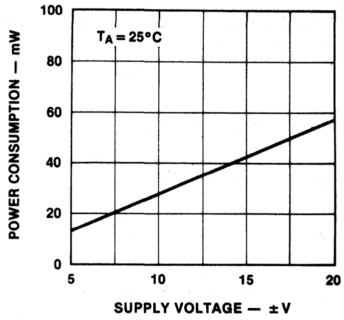
AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.

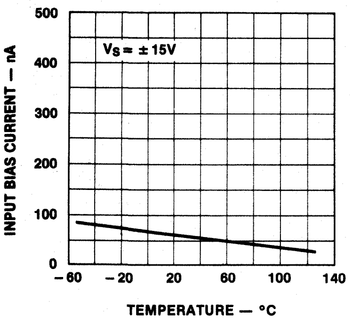
PARAMETER	TEST CONDITIONS	MC1458, SA1458, MC1558			UNIT
		Min	Typ	Max	
Parallel input resistance	Open loop, f = 20Hz	0.3			MΩ
Common mode input impedance	f = 20Hz		200		MΩ
Equivalent input noise voltage	$A_V = 100$, $R_S = 10k\Omega$, $B_W = 1.0kHz$, f = 1.0kHz		45		nV √Hz
Power bandwidth	$A_V = 1$, $R_L = 2.0k\Omega$, THD ≤ 5%, $V_{OUT} = 20Vp\text{-}p$		14		kHz
Phase margin			65		degrees
Gain margin			11		dB
Unity gain crossover frequency	Open loop		1.0		MHz
Transient response unity gain Rise time Overshoot Slew rate	$V_{IN} = 20mV$, $R_L = 2k\Omega$, $C_L \leq 100pF$ C ≤ 100pF, $R_L \geq 2k$, $V_{IN} = \pm 10V$		 0.3 5.0 0.8		 μs % V/μs

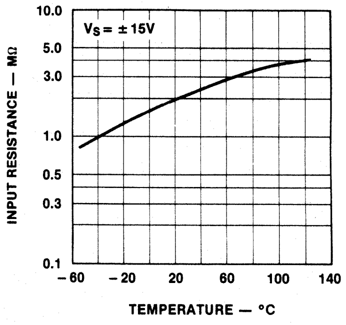
TYPICAL PERFORMANCE CHARACTERISTICS

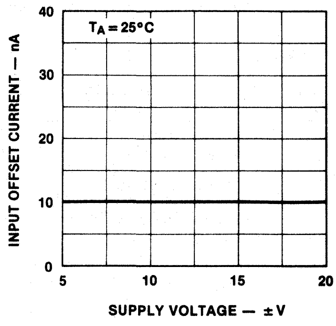

OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE


INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE


POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE

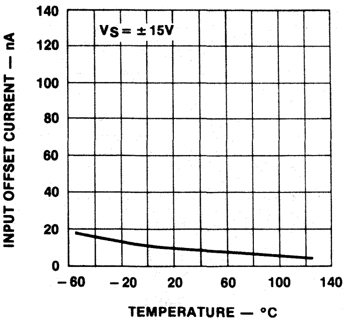

INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE


INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

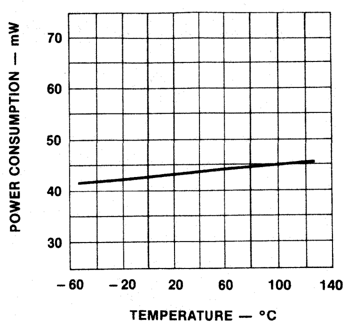

INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

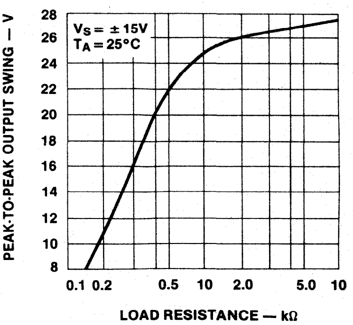
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



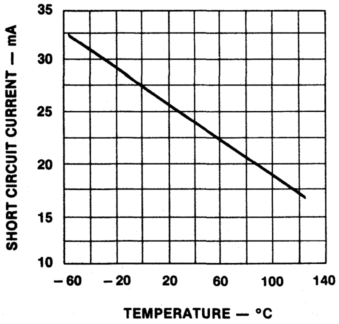
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



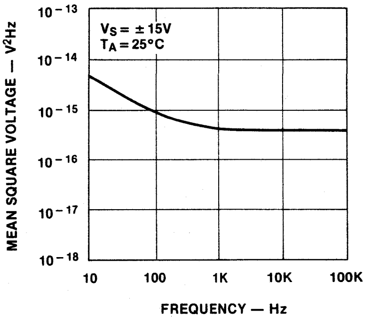
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



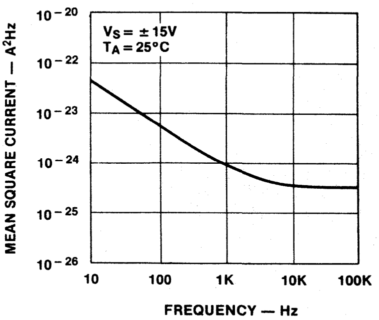
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



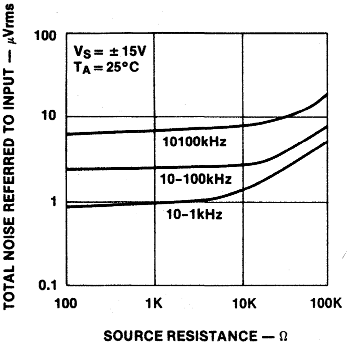
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



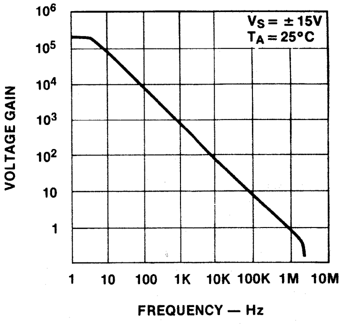
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



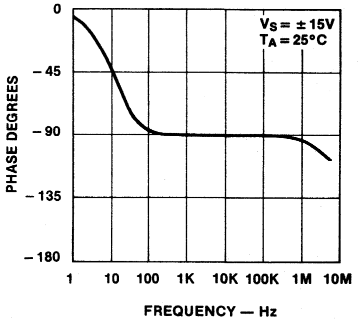
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



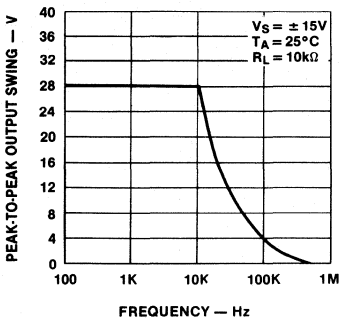
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



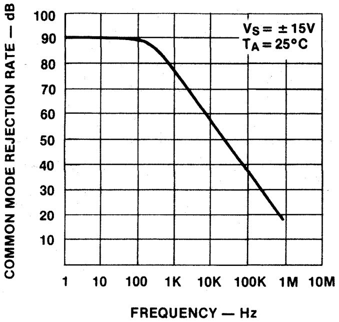
GENERAL PURPOSE OPERATIONAL AMPLIFIER MC/SA1458/MC1558

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

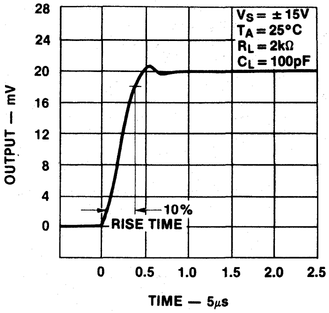
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



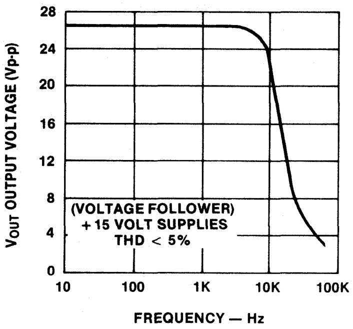
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



TRANSIENT RESPONSE



POWER BANDWIDTH (Large Signal Swing vs Frequency)



QUAD LOW POWER OPERATIONAL AMPLIFIERS MC3303/3403/3503

DESCRIPTION

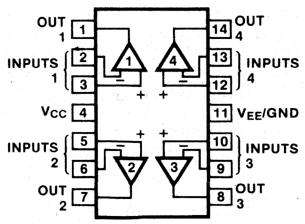
The MC3403 is a quad operational amplifier with true differential inputs. The device has electrical characteristics similar to the popular μA741. However, the MC3403 has several distinct advantages over standard operational amplifier types in single supply applications. The MC3403 can operate at supply voltages as low as 3.0V or as high as 36V. The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

FEATURES

- **Short circuit protected outputs**
- **Class AB output stage for minimal crossover distortion**
- **True differential input stage**
- **Single supply operation: 3.0 to 36V**
- **Split supply operation: ±1.5 to ±18V**
- **Low input bias currents: 500nA max**
- **Four amplifiers per package**
- **Internally compensated**

PIN CONFIGURATION

D, F, N PACKAGES



TOP VIEW

ORDER NUMBERS

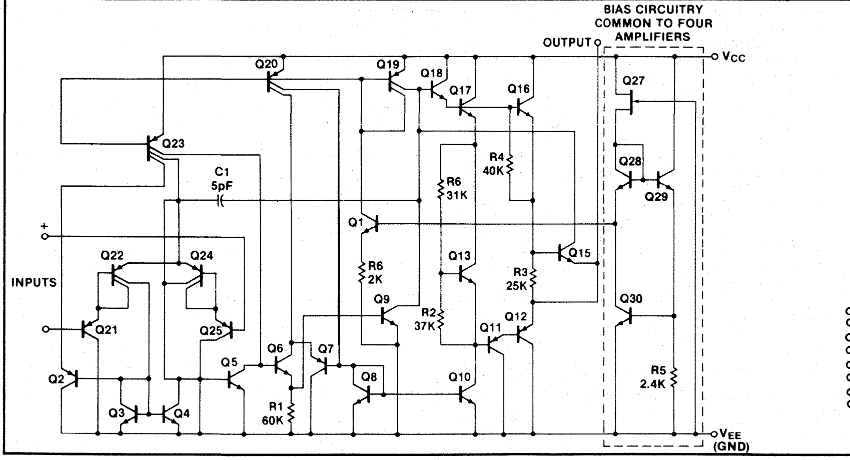
MC3303F	MC3403D	MC3503F
MC3303N	MC3403F	
	MC3403N	

ABSOLUTE MAXIMUM RATINGS

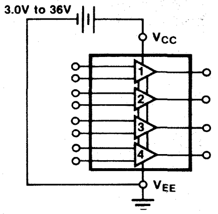
SYMBOL AND PARAMETER	RATING	UNIT
Power supply voltages		
V_{CC} Single supply	36	Vdc
V_{CC} Split supplies	+18	Vdc
V_{EE}	−18	Vdc
V_{IDR} Input differential voltage range[1]	±36	Vdc
V_{ICR} Input common mode voltage range[1,2]	±18	Vdc
T_{stg} Storage temperature range		
Ceramic package	−65 to +150	°C
Plastic package	−55 to +125	°C
T_A Operating ambient temperature range		
MC3503	−55 to +125	°C
MC3403	0 to +70	°C
MC3303	−40 to +85	°C
T_J Junction temperature		
Ceramic package	175	°C
Plastic package	150	°C

NOTES
1. Split power supplies.
2. For supply voltages less than ± 15V, the absolute maximum input voltage is equal to the supply voltage.

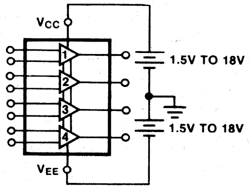
CIRCUIT SCHEMATIC (1/4 Shown)



SINGLE SUPPLY



SPLIT SUPPLIES



QUAD LOW POWER OPERATIONAL AMPLIFIERS MC3303/3403/3503

ELECTRICAL CHARACTERISTICS (V_{CC} = + 15V, V_{EE} = – 15V for MC3503, MC3403; V_{CC} = + 14V, V_{EE} = GND for MC3303. T_A = 25°C unless otherwise noted)

SYMBOL AND PARAMETER		TEST CONDITIONS	MC3503			MC3403			MC3303			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input offset voltage		—	2.0	5.0	—	2.0	10	—	2.0	8.0	mV
		$T_A = T_{HIGH}$ to T_{LOW}[1]	—	—	6.0	—	—	12	—	—	10	
I_{IO}	Input offset current		—	10	50	—	10	50	—	30	75	nA
		$T_A = T_{HIGH}$ to T_{LOW}	—	—	200	—	—	200	—	—	250	
A_{VOL}	Large signal open-loop voltage gain	$V_O = \pm 10V$, $R_L = 2.0k\Omega$	50	200	—	20	200	—	20	200	—	V/mV
		$T_A = T_{HIGH}$ to T_{LOW}	25	300	—	15	—	—	15	—	—	
I_{IB}	Input bias current		—	– 30	– 500	—	– 30	– 500	—	– 30	– 500	nA
		$T_A = T_{HIGH}$ to T_{LOW}	—	– 40	– 1200	—	—	– 800	—	—	– 1000	
z_o	Output impedance	f = 20Hz	—	75	—	—	75	—	—	75	—	Ω
z_i	Input impedance	f = 20Hz	0.3	1.0	—	0.3	1.0	—	0.3	1.0	—	MΩ
V_{OR}	Output voltage range	$R_L = 10k\Omega$	± 12	± 13.5	—	± 12	± 13.5	—	+ 12	+ 12.5	—	V
		$R_L = 2.0k\Omega$	± 10	± 13	—	± 10	± 13	—	+ 10	+ 12	—	
		$R_L = 2.0k\Omega$, $T_A = T_{HIGH}$ to T_{LOW}	± 10	—	—	± 10	—	—	+ 10	—	—	
V_{ICR}	Input common mode voltage range		+ 13V – V_{EE}	+ 13.5V – V_{EE}	—	+ 13V – V_{EE}	+ 13.5V – V_{EE}	—	+ 12V – V_{EE}	+ 12.5V – V_{EE}	—	V
CMRR	Common mode rejection ratio	$R_S \leq 10k\Omega$	70	90	—	70	90	—	70	90	—	dB
I_{CC}, I_{EE}	Power supply current ($V_O = 0$)	$R_L = \infty$	—	2.5	4.0	—	2.5	7.0	—	2.5	7.0	mA
$I_{OS\pm}$	Individual output short circuit current[2]		± 10	± 30	± 45	± 10	± 20	± 45	± 10	± 30	± 45	mA
PSRR +	Positive power supply rejection ratio		—	30	150	—	30	150	—	30	150	μV/V
PSRR –	Negative power supply rejection ratio		—	30	150	—	30	150	—	—	—	μV/V
$\Delta I_{IO}/\Delta T$	Average temperature coefficient of input offset current	$T_A = T_{HIGH}$ to T_{LOW}	—	50	—	—	50	—	—	50	—	pA/°C
$\Delta V_{IO}/\Delta T$	Average temperature coefficient of input offset voltage	$T_A = T_{HIGH}$ to T_{LOW}	—	10	—	—	10	—	—	10	—	μV/°C
BW_P	Power bandwidth	$A_V = 1$, $R_L = 2.0k\Omega$, $V_O = 20V(p-p)$ THD = 5%	—	9.0	—	—	9.0	—	—	9.0	—	kHz
BW	Small signal bandwidth	$A_V = 1$, $R_L = 10k\Omega$, $V_O = 50mV$	—	1.0	—	—	1.0	—	—	1.0	—	MHz
SR	Slew rate	$A_V = 1$, $V_i = -10V$ to $+10V$	—	0.6	—	—	0.6	—	—	0.6	—	V/μs
t_{TLH}	Rise time	$A_V = 1$, $R_L = 10k\Omega$, $V_O = 50mV$	—	0.35	—	—	0.35	—	—	0.35	—	μs
t_{THL}	Fall time	$A_V = 1$, $R_L = 10k\Omega$, $V_O = 50mV$	—	0.35	—	—	0.35	—	—	0.35	—	μs
OS	Overshoot	$A_V = 1$, $R_L = 10k\Omega$ $V_O = 50mV$	—	20	—	—	20	—	—	20	—	%
ϕm	Phase margin	$A_V = 1$, $R_L = 2.0k\Omega$, $C_L = 200pF$	—	50	—	—	50	—	—	50	—	°
—	Crossover distortion	$V_{IN} = 30mV(p-p)$, $V_{OUT} = 2.0V(p-p)$, f = 10kHz	—	1.0	—	—	1.0	—	—	1.0	—	%

NOTES

1. T_{HIGH} = 125°C for MC3503, 70°C for MC3403, 85°C for MC3303. T_{LOW} = – 55°C for MC3503, 0°C for MC3403, – 40°C for MC3303.
2. Not to exceed maximum package power dissipation.

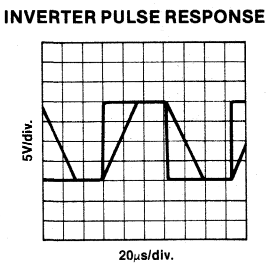
QUAD LOW POWER OPERATIONAL AMPLIFIERS MC3303/3403/3503

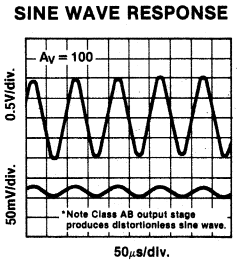
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V, V_E = GND, T_A = 25°C unless otherwise noted.)

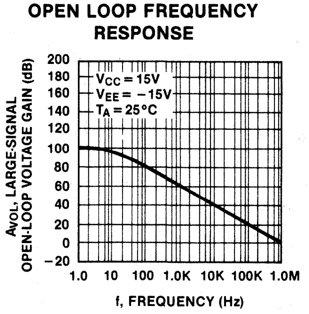
SYMBOL AND PARAMETER		TEST CONDITIONS	MC3503			MC3403			MC3303			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input offset voltage		—	2.0	5.0	—	2.0	10	—	—	10	mV
I_{IO}	Input offset current		—	30	50	—	30	50	—	—	75	nA
I_{IB}	Input bias current		—	−200	−500	—	−200	−500	—	—	−500	nA
A_{VOL}	Large signal open-loop voltage gain	R_L = 2.0kΩ	10	200	—	10	200	—	10	200	—	V/mV
PSRR	Power supply rejection ratio		—	—	150	—	—	150	—	—	150	µV/V
V_{OR}	Output voltage range(3)	R_L = 10kΩ, V_{CC} = 5.0V	3.3	3.5	—	3.3	3.5	—	3.3	3.5	—	Vp-p
		R_L = 10kΩ, 5.0V ≤ V_{CC} ≤ 30V	V_{CC} − 1.7	V_{CC} − 1.5	—	V_{CC} − 1.7	V_{CC} − 1.5	—	V_{CC} − 1.7	V_{CC} − 1.5	—	
I_{CC}	Power supply current		—	2.5	4.0	—	2.5	7.0	—	2.5	7.0	mA
—	Channel separation	f = 1.0kHz to 20kHz (input referenced)	—	−120	—	—	−120	—	—	−120	—	dB

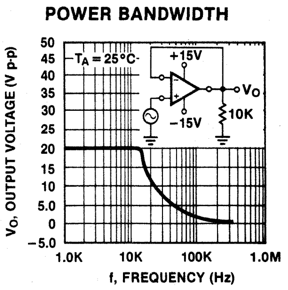
NOTE
3. Output will swing to ground.

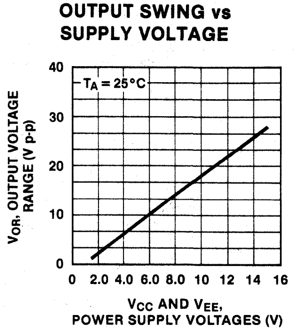
TYPICAL PERFORMANCE CURVES


INVERTER PULSE RESPONSE


SINE WAVE RESPONSE


OPEN LOOP FREQUENCY RESPONSE

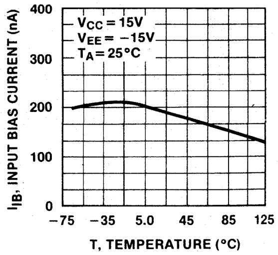

POWER BANDWIDTH


OUTPUT SWING vs SUPPLY VOLTAGE

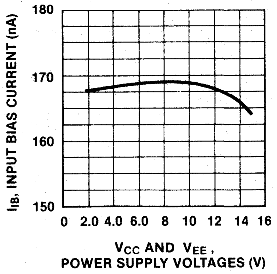
QUAD LOW POWER OPERATIONAL AMPLIFIERS MC3303/3403/3503

TYPICAL PERFORMANCE CURVES (Continued)

INPUT BIAS CURRENT vs TEMPERATURE

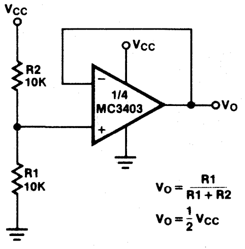


INPUT BIAS CURRENT vs SUPPLY VOLTAGE



APPLICATIONS

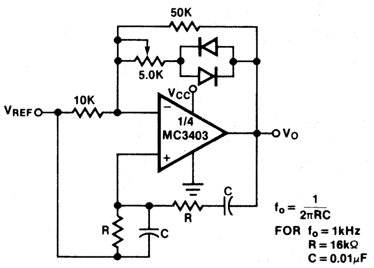
VOLTAGE REFERENCE



$$V_O = \frac{R1}{R1 + R2}$$

$$V_O = \frac{1}{2} V_{CC}$$

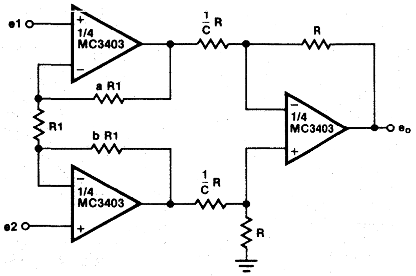
WEIN BRIDGE OSCILLATOR



$$f_o = \frac{1}{2\pi RC}$$

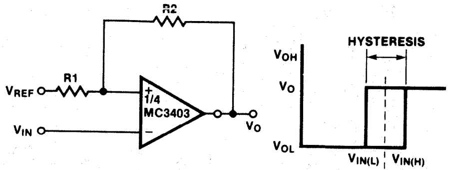
FOR f_o = 1kHz
R = 16kΩ
C = 0.01μF

HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER



e_o = C(1 + a + b) (e2 − e1)

COMPARATOR WITH HYSTERESIS



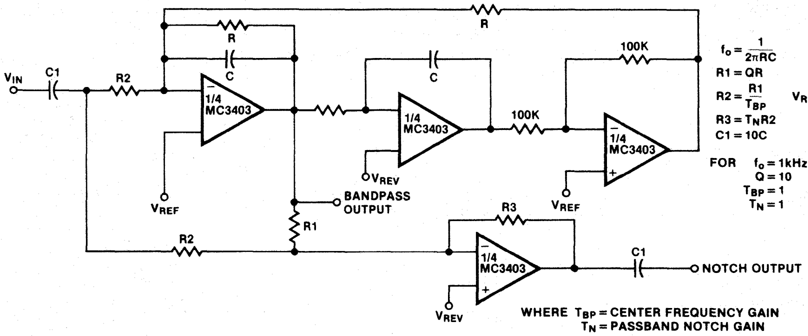
$$V_{IN(L)} = \frac{R1}{R1 + R2}(V_{OL} - V_{REF}) + V_{REF}$$

$$V_{IN(H)} = \frac{R1}{R1 + R2}(V_{OH} - V_{REF}) + V_{REF}$$

$$H = \frac{R1}{R1 + R2}(V_{OH} - V_{OL})$$

APPLICATIONS (Continued)

BI-QUAD FILTER



$f_o = \frac{1}{2\pi RC}$

R1 = QR

$R2 = \frac{R1}{T_{BP}}$ $V_{REF} = \frac{1}{2}V_{CC}$

$R3 = T_N R2$

C1 = 10C

FOR $f_o = 1kHz$

Q = 10

$T_{BP} = 1$

$T_N = 1$

R = 160kΩ

C = 0.001μF

R1 = 1.6MΩ

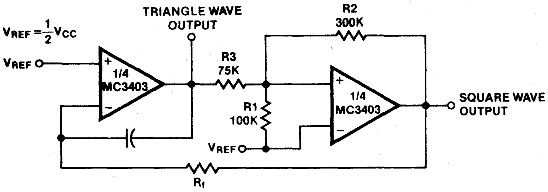
R2 = 1.6MΩ

R3 = 1.6MΩ

WHERE T_{BP} = CENTER FREQUENCY GAIN

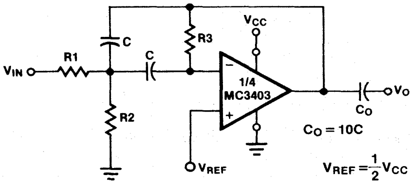
T_N = PASSBAND NOTCH GAIN

FUNCTION GENERATOR



$f = \frac{R1 + R_C}{4 CR_f R1}$ IF $R3 = \frac{R2\ R1}{R2 + R1}$

MULTIPLE FEEDBACK BANDPASS FILTER



GIVEN f_o = CENTER FREQUENCY

$A(f_o)$ = GAIN AT CENTER FREQUENCY

CHOOSE VALUE f_o, C

THEN:

$$R3 = \frac{Q}{\pi f_o C}$$

$$R1 = \frac{R3}{2\,A(f_o)}$$

$$R2 = \frac{R1\ R5}{4Q^2\,R1 - R5}$$

FOR LESS THAN 10% ERROR FROM OPERATIONAL AMPLIFIER

$\frac{Q_o f_o}{BW} < 0.1$ WHERE f_o AND BW ARE EXPRESSED IN Hz.

IF SOURCE IMPEDANCE VARIES, FILTER MAY BE PRECEDED WITH VOLTAGE FOLLOWER BUFFER TO STABILIZE FILTER PARAMETERS.

HIGH SLEW RATE OPERATIONAL AMPLIFIER NE/SE530/5530

DESCRIPTION

The 530/5530 are new generation operational amplifiers featuring high slew rates combined with improved input characteristics. Internally compensated, the SE530/5530 guarantee slew rates of 25V/μs with 2mV maximum offset voltage. Industry standard pinout and internal compensation allow the user to upgrade system performance by directly replacing general purpose amplifiers such as the 741, 747, 1458, 4558 and LF356 types.

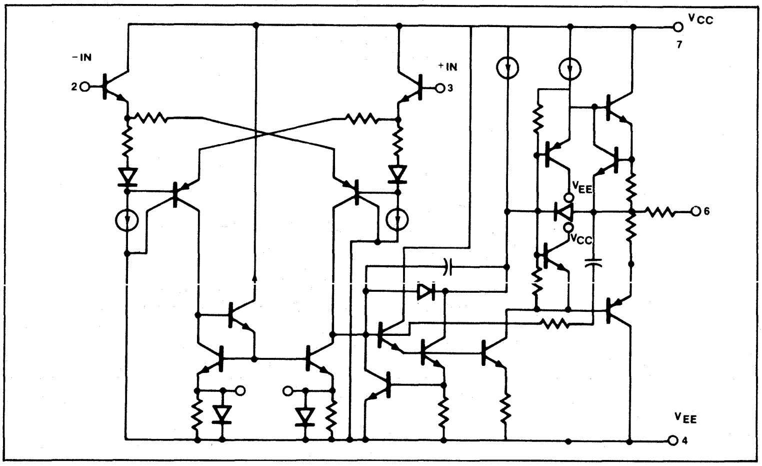
FEATURES

- **Gain bandwidth product—3MHz**
- **35V/μs slew rate (Gain = -1)**
- **Internal frequency compensation**
- **Low input offset voltage 2mV max**
- **Low input bias current-60nA max**
- **Short circuit protection**
- **Offset null capability**
- **Large common mode and differential voltage ranges**

ABSOLUTE MAXIMUM RATINGS

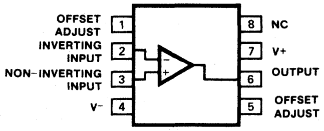
PARAMETER	RATING	UNIT
Supply voltage		
SE530/5530	±22	V
NE530/5530	±18	V
Internal power dissipation		
N Package	500	mW
H Package	800	mW
FE Package	1000	mW
Differential input voltage	±30	V
Input voltage	±15	V
Operating temperature range		
SE530/5530	-55 to +125	°C
NE530/5530	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature range (Solder, 60sec)	300	°C
Output short circuit	Indefinite	

EQUIVALENT SCHEMATIC EACH AMPLIFIER



PIN CONFIGURATIONS

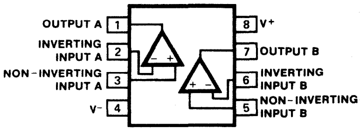
FE,N PACKAGE



TOP VIEW

ORDER NUMBERS
NE530FE, NE530N
SE530FE, SE530N

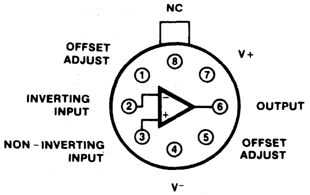
N PACKAGE



TOP VIEW

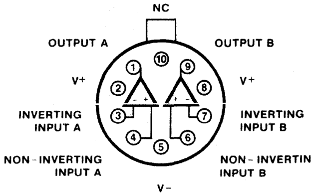
ORDER NUMBERS
NE5530N SE5530N

H PACKAGE*



ORDER NUMBERS
NE530H SE530H
*Metal cans (H) not recommended for new designs.

H PACKAGE*



ORDER NUMBERS
NE5530H SE5530H
*Metal cans (H) not recommended for new designs.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = \pm15V$ unless otherwise specified.[1]

PARAMETER	TEST CONDITIONS	SE530/5530			NE530/5530			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage	$R_S \le 10k\Omega$ Over temperature		0.7	4.0 5.0		2.0	6.0 7.0	mV mV
Temperature coefficient of input offset voltage			3	15		6		μV/°C
Input offset current	 Over temperature		5	20 40		15	40 80	nA nA
Input bias current	 Over temperature		45	80 200		65	150 200	nA nA
Input resistance		3	10		1	6		MΩ
Input voltage range		±12	±13		±12	±13		V
Large signal voltage gain	$R_L \ge 2k\Omega$, $V_O = \pm10V$ Over temperature	50 25	200		50 25	200		V/mV V/mV
Output voltage swing	$R_L \ge 10k\Omega$ $R_L \ge 2k\Omega$	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V V
Output short circuit current			25			25		mA
Output resistance			100			100		Ω
Supply current	Each amplifier Over temperature		2.0 2.2	3.0 3.6		2.0 2.2	3.0	mA mA
Common mode rejection ratio	$R_S \le 10k\Omega$ Over temperature	70	90		70	90		dB
Power supply rejection ratio	$R_S \le 10k\Omega$ Over temperature		30	150		30	150	μV/V

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = \pm15V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE530/5530			NE530/5530			UNIT
		Min	Typ	Max	Min	Typ	Max	
Transient Response								
Small signal rise time			.06			.06		μs
Small signal overshoot			13			13		%
Settling time	TO 0.1% (10V step)		0.9			0.9		μs
Slew rate	±15V supply, $V_O = \pm10V$, $R_L \ge 2k\Omega$							
Unity gain inverting		25	35		20	35		V/μs
Unity gain non-inverting		18	25		12	25		V/μs
Power bandwidth	5% THD, $V_O = \pm10V$, $R_L \ge 2k\Omega$	360	500		280	500		kHz
Small signal bandwidth	Open loop		3			3		MHz
Channel separation			120			120		dB

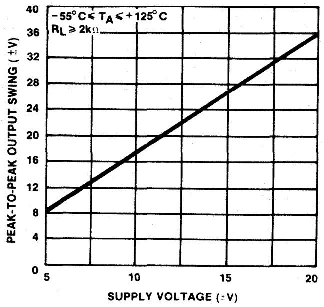
NOTE

1. Operating temperature range for the SE530/5530 is -55°C to +125°C.
   Operating temperature range for the NE530/5530 is 0°C to +70°C.

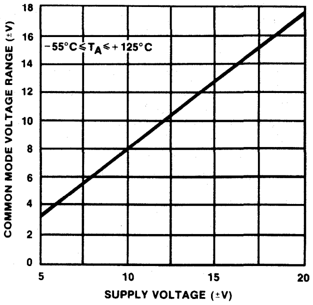
HIGH SLEW RATE OPERATIONAL AMPLIFIER NE/SE530/5530

TYPICAL PERFORMANCE CHARACTERISTICS

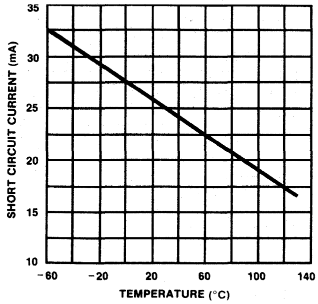
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



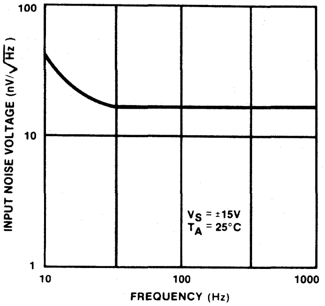
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



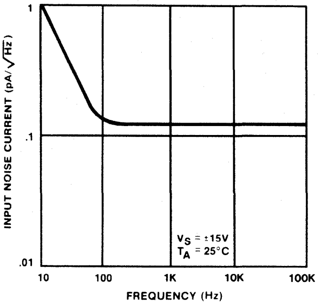
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



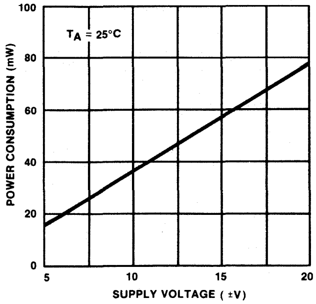
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



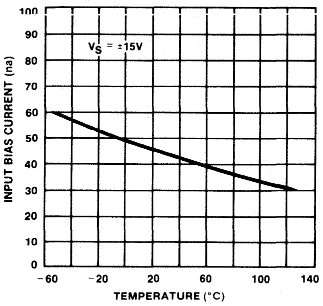
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



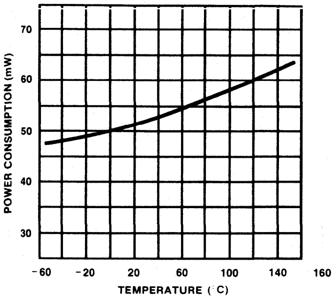
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE (EACH AMPLIFIER)



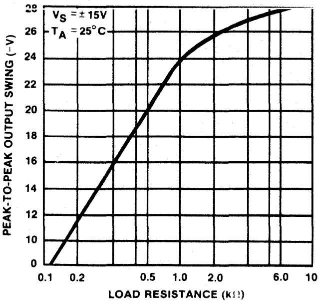
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE (EACH AMPLIFIER)

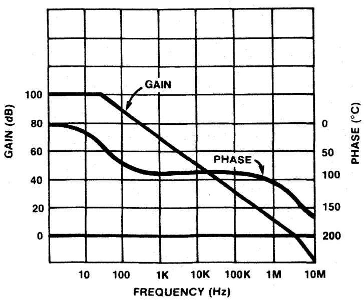


OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

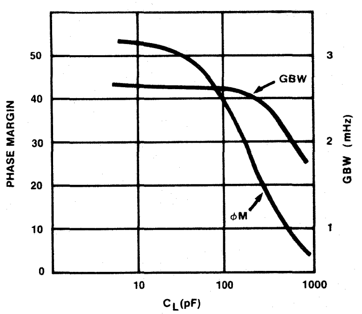


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

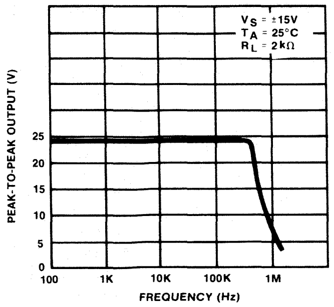
NE530 OPEN-LOOP GAIN AND PHASE vs FREQUENCY



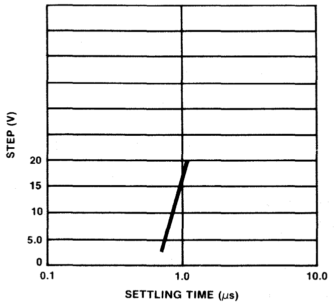
GAIN-BANDWIDTH PRODUCT AND PHASE MARGIN vs LOAD CAPACITANCE



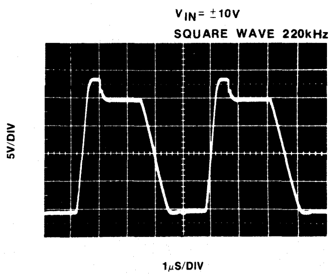
POWER BANDWIDTH



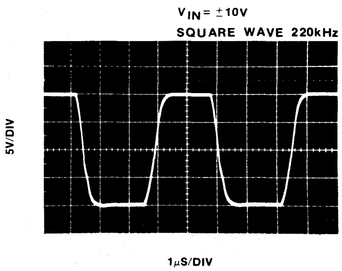
INPUT VOLTAGE STEP vs SETTLING TIME TO 10mV



SLEW RATE—VOLTAGE FOLLOWER

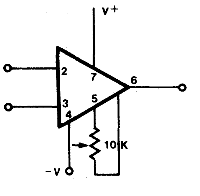


SLEW RATE (-1 AMPLIFIER)



TYPICAL CIRCUIT CONNECTION

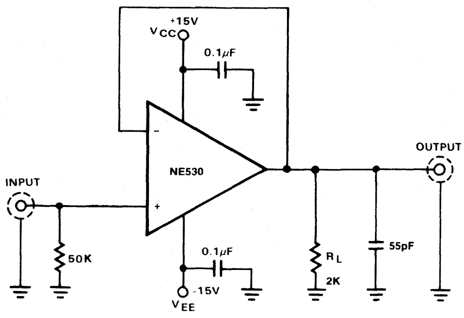
OFFSET ADJUST CIRCUIT



HIGH SLEW RATE OPERATIONAL AMPLIFIER NE/SE530/5530

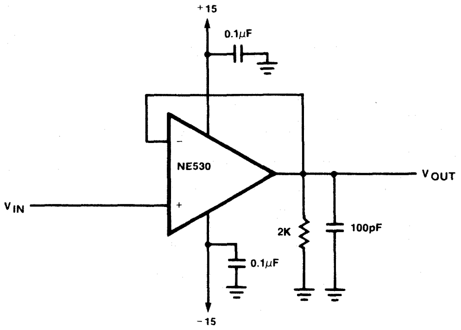
TEST LOAD CIRCUITS

SMALL SIGNAL TRANSIENT RESPONSE

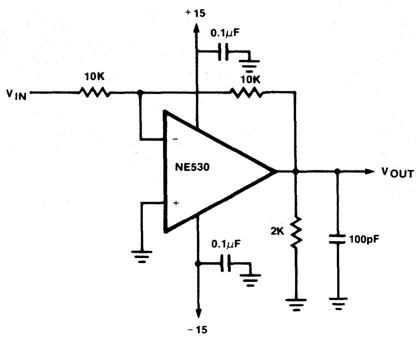


Pins not shown are not connected.
All resistor values are typical and in ohms.

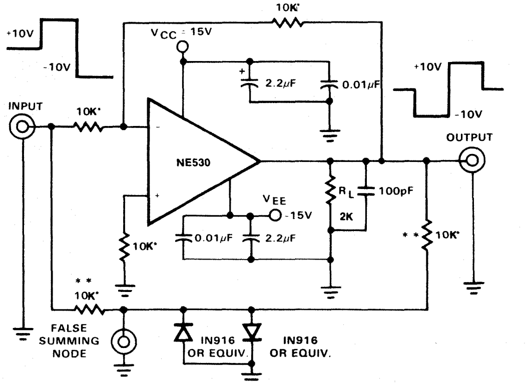
SLEW RATE—VOLTAGE FOLLOWER



SLEW RATE—INVERTING AMPLIFIER



SLEW RATE AND SETTLING TIME

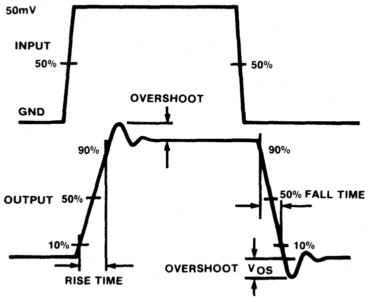


Pins not shown are not connected.
All resistor values are typical and in ohms.

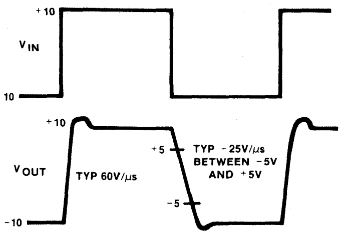
*Match to within 0.01%.
**Open for slew rate.

VOLTAGE WAVEFORMS

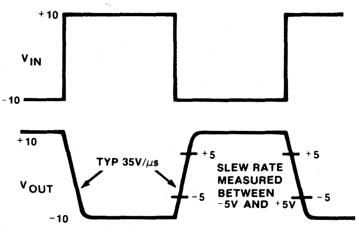
SMALL SIGNAL TRANSIENT RESPONSE DEFINITIONS



SLEW RATE—VOLTAGE FOLLOWER



SLEW RATE—INVERTING AMPLIFIER



HIGH SLEW RATE OPERATIONAL AMPLIFIER NE/SE531

DESCRIPTION

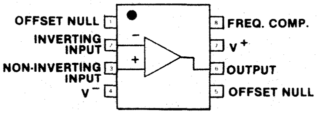
The 531 is a fast slewing high performance operational amplifier which retains dc performance equal to the best general purpose types while providing far superior large signal ac performance. A unique input stage design allows the amplifier to have a large signal response nearly identical to its small signal response. The amplifier is compensated for truly negligible overshoot with a single capacitor. In applications where fast settling and superior large signal bandwidths are required, the amplifier out performs conventional designs which have much better small signal response. Also, because the small signal response is not extended, no special precautions need be taken with circuit board layout to achieve stability. The high gain, simple compensation and excellent stability of this amplifier allow its use in a wide variety of instrumentation applications.

FEATURES

- **35V/μsec slew rate at unity gain**
- **Pin for pin replacement for μA709, μA748 or LM101**
- **Compensated with a single capacitor**
- **Same low drift offset null circuitry as μA741**
- **Small signal bandwidth 1MHz**
- **Large signal bandwidth 500KHz**
- **True op amp dc characteristics make the 531 the ideal answer to all slew rate limited operational amplifier applications.**

PIN CONFIGURATIONS

N,FE PACKAGE

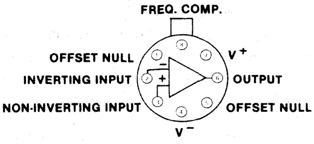


TOP VIEW

ORDER NUMBERS

NE531N	SE531N
NE531FE	SE531FE

H PACKAGE*

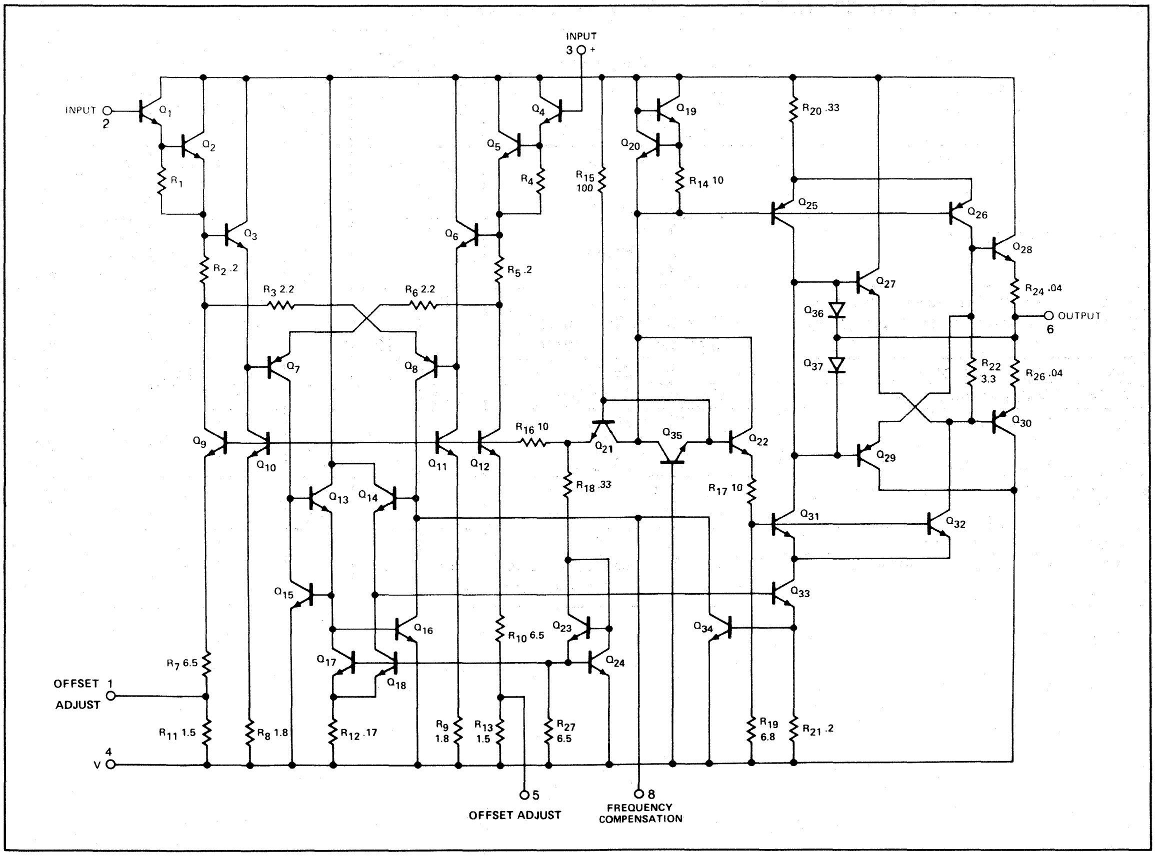


ORDER NUMBERS

NE531H/SE531H

*Metal cans (H) not recommended for new designs

EQUIVALENT SCHEMATIC



HIGH SLEW RATE OPERATIONAL AMPLIFIER NE/SE531

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	±22	V
Internal power dissipation[1]	300	mW
Differential input voltage	±15	V
Common mode input voltage[2]	±15	V
Voltage between offset null and V-	±0.5	V
Operating temperature range		
NE531	0 to +70	°C
SE531	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60 sec)	300	°C
Output short circuit duration[3]	indefinite	

NOTES

1. Rating applies for case temperature to 125°C, derate linearly at 6.5mW/°C for ambient temperatures above +75°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or to +75°C ambient temperature.

DC ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$ unless otherwise specified.

	PARAMETER	TEST CONDITIONS	SE531[1]			NE531			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S \leq 10k\Omega$, $T_A = 25°C$		2.0	5.0		2.0	6.0	mV
		$R_S \leq 10k\Omega$, over temp			6.0			7.5	mV
I_{OS}	Offset current	$T_A = 25°C$		30	200		50	200	nA
		$T_A = HIGH$			200			200	nA
		$T_A = LOW$			500			300	nA
I_{BIAS}	Input current	$T_A = 25°C$		300	500		400	1500	nA
		$T_A = HIGH$			500			1500	nA
		$T_A = LOW$			1500			2000	nA
V_{CM}	Common mode voltage range	$T_A = 25°C$	±10			±10			V
CMRR	Common mode rejection ratio	$T_A = 25°C$, $R_S \leq 10k\Omega$				70	100		dB
		Over temp $R_S \leq 10k\Omega$	70	90					dB
R_{IN}	Input resistance	$T_A = 25°C$		20			20		MΩ
V_{OUT}	Output voltage swing	$R_L \geq 10k\Omega$, over temp	±10	±13		±10	±13		V
I_{CC}	Supply current	$T_A = 25°C$			7.0			10	mA
		T_{MAX}			7.0			10	mA
P_D	Power consumption	$T_A = 25°C$			210			300	mW
PSRR	Power supply rejection ratio	$R_S \leq 10k\Omega$, $T_A = 25°C$					10	150	μV/V
		$R_S \leq 10k\Omega$, over temp		10	150				μV/V
R_{OUT}	Output resistance	$T_A = 25°C$		75			75		Ω
A_{VOL}	Large signal voltage gain	$T_A = 25°C$, $R_L \geq 10k\Omega$, $V_{OUT} = \pm 10V$	50	100		20	60		V/mV
		$R_L \geq 10k\Omega$, $V_{OUT} = \pm 10V$, over temp	25			15			V/mV

NOTE

1. Temperature range:
   SE531 $-55°C \leq T_A \leq 125°C$
   NE531 $0°C \leq T_A \leq 70°C$

HIGH SLEW RATE OPERATIONAL AMPLIFIER NE/SE531

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

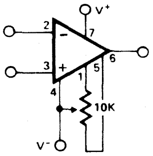
PARAMETER	TEST CONDITIONS	NE531			SE531			UNIT
		Min	Typ	Max	Min	Typ	Max	
Full power bandwidth			500			500		kHz
Settling time (1%) (.01%)	$A_V = +1$, $V_{IN} = \pm 10V$		1.5 2.5			1.5 2.5		μs μs
Large signal overshoot	$A_V = +1$, $V_{IN} = \pm 10V$		2			2		%
Small signal overshoot	$A_V = +1$, $V_{IN} = 400mV$		5			5		%
Small signal risetime	$A_V = +1$, $V_{IN} = 400mV$		300			300		ns
Slew rate	$A_V = 100$		35			35		V/μs
	$A_V = 10$		35			35		V/μs
	$A_V = 1$ (noninverting)		30		20	30		V/μs
	$A_V = 1$ (inverting)		35		25	35		V/μs

NOTE

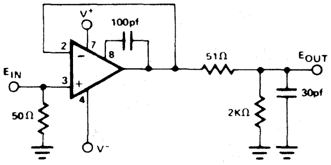
1. All AC testing is performed in the transient response test circuit.

TEST LOAD CIRCUITS

OFFSET NULL CIRCUIT

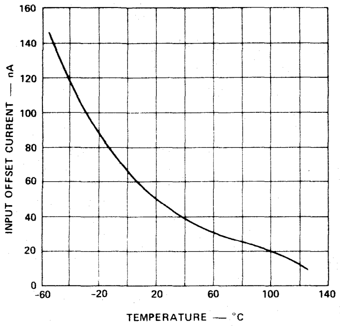


TRANSIENT RESPONSE CIRCUIT

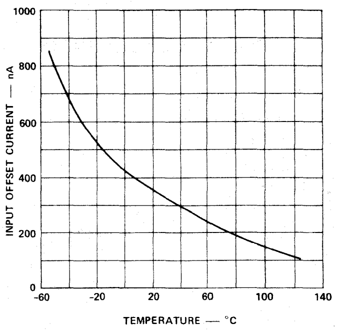


TYPICAL PERFORMANCE CHARACTERISTICS ($V_S = \pm 15V$, $T_A = +25°C$, unless otherwise specified.)

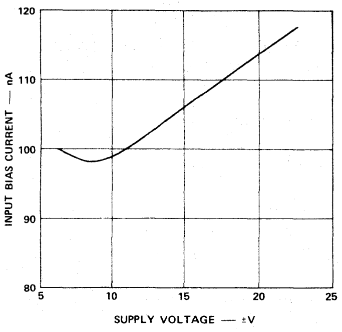
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

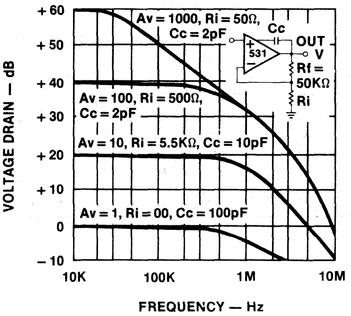


INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

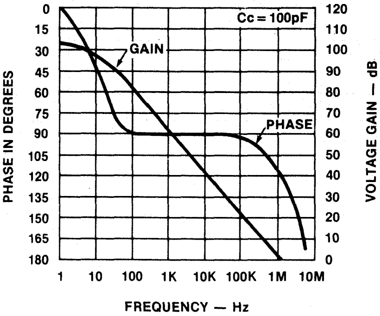


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

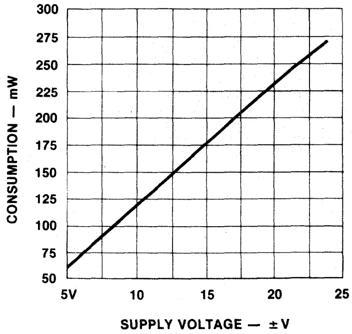
CLOSED LOOP NON-INVERTING VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



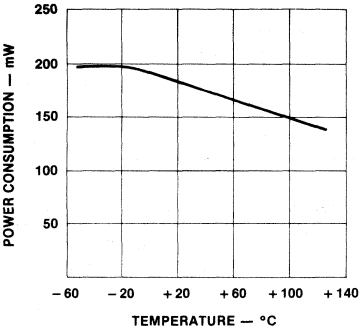
OPEN LOOP PHASE RESPONSE AND VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



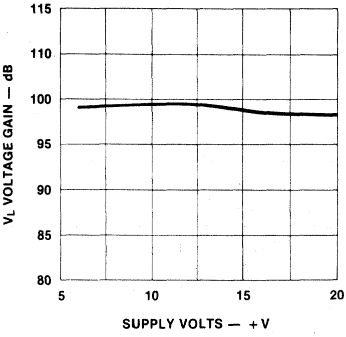
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



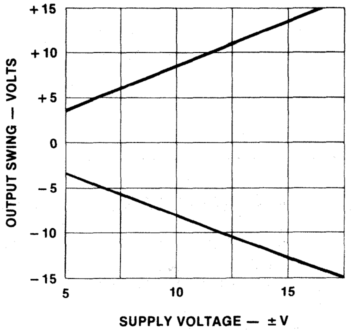
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



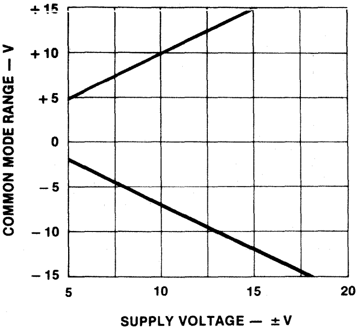
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



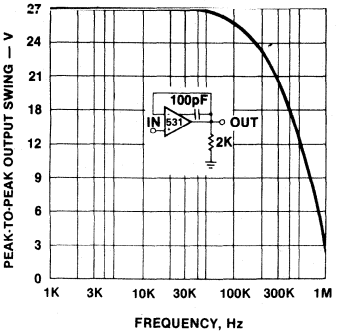
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



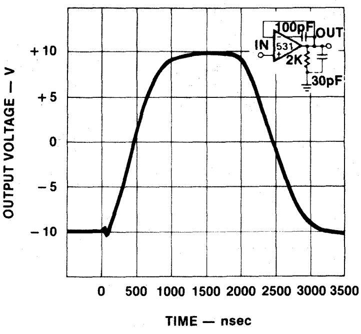
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

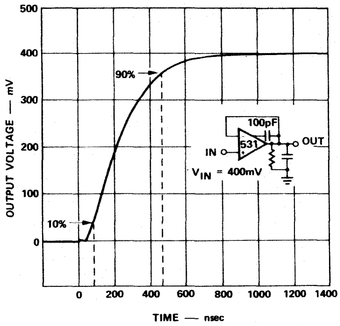


VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE

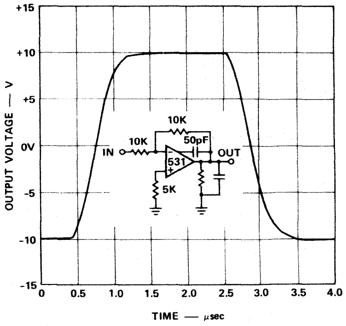


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

VOLTAGE FOLLOWER TRANSIENT RESPONSE

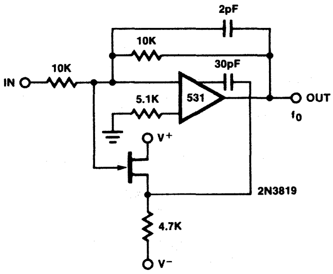


UNITY GAIN INVERTING AMPLIFIER LARGE SIGNAL RESPONSE

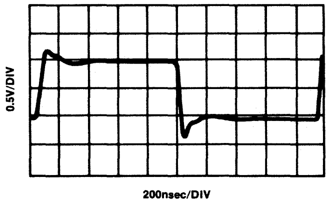


TYPICAL APPLICATIONS

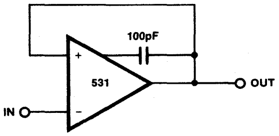
HIGH SPEED INVERTER (10MHz BANDWIDTH)



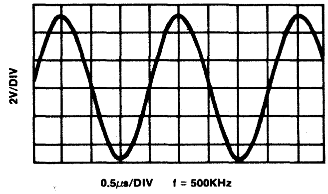
PULSE RESPONSE HIGH SPEED INVERTER



FAST SETTLING VOLTAGE FOLLOWER

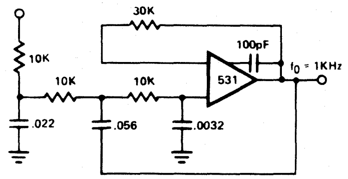


LARGE SIGNAL RESPONSE VOLTAGE FOLLOWER



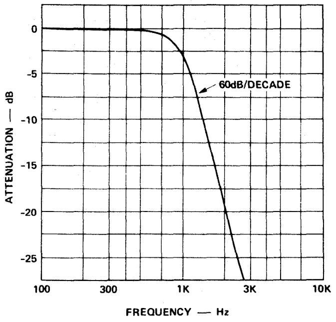
TYPICAL APPLICATIONS (Cont'd)

POLE ACTIVE LOW PASS FILTER BUTTERWORTH MAXIMALLY FLAT RESPONSE*



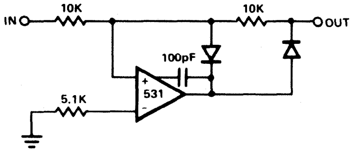
*Reference—EDN Dec. 15, 1970
Simplify 3-Pole Active Filter Design
A. Paul Brokow

RESPONSE OF 3-POLE ACTIVE BUTTERWORTH MAXIMALLY FLAT FILTER

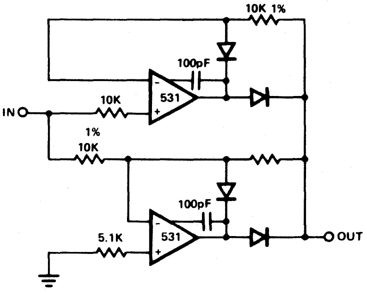


PRECISION RECTIFIERS

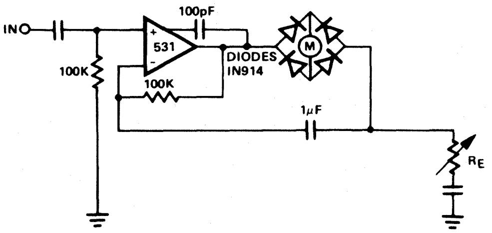
(a) HALF WAVE



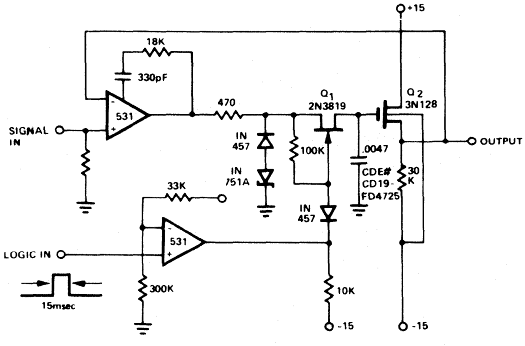
(b) FULL WAVE



AC MILLIVOLTMETER



SAMPLE AND HOLD



LOW POWER DUAL OPERATIONAL AMPLIFIERS NE/SA/SE532/LM158/258/358

DESCRIPTION

The 532/358 consists of two independent, high gain, internally frequency compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages. Operation from dual power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

FEATURES

- **Internally frequency compensated for unity gain**
- **Large dc voltage gain—(100dB)**
- **Wide bandwidth (unity gain)—1MHz (temperature compensated)**
- **Wide power supply range**
  single supply—(3Vdc to 30Vdc)
  or dual supplies—(±1.5Vdc to ±15Vdc)
- **Very low supply current drain (400μA)—essentially independent of supply voltage (1mW/op amp at +5Vdc)**
- **Low input biasing current—(45nA dc temperature compensated)**
- **Low input offset voltage—(2mVdc) and offset current—(5nA dc)**
- **Differential input voltage range equal to the power supply voltage**
- **Large output voltage—(0Vdc to V+—-1.5Vdc swing)**
- **SE532 MIL-STD-883A,B,C available**

UNIQUE FEATURES

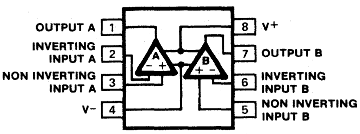
In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage. The unity gain cross frequency is temperature compensated. The input bias current is also temperature compensated.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage, V+	32 or ±16	Vdc
Differential input voltage	32	Vdc
Input voltage	-0.3 to +32	Vdc
Power dissipation[1]		
FE package	900	mW
H package	680	mW
N package	500	mW
Output short-circuit to GND[5]		
V+ < 15 Vdc and T_A = 25°C	Continuous	
Operating temperature range		
NE532/LM358	0 to +70	°C
LM258	-25 to +85	°C
SA532N	-40 to +85	°C
SE532/LM158	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 10sec)	300	°C

PIN CONFIGURATIONS

FE,N PACKAGE

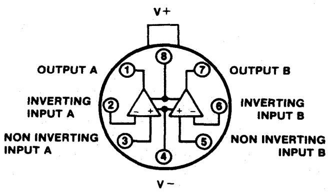


TOP VIEW

ORDER NUMBERS

LM158N, FE
LM258N, FE
LM358D, N, FE
NE523D, N, FE
SA532FE, N
SE532N, FE

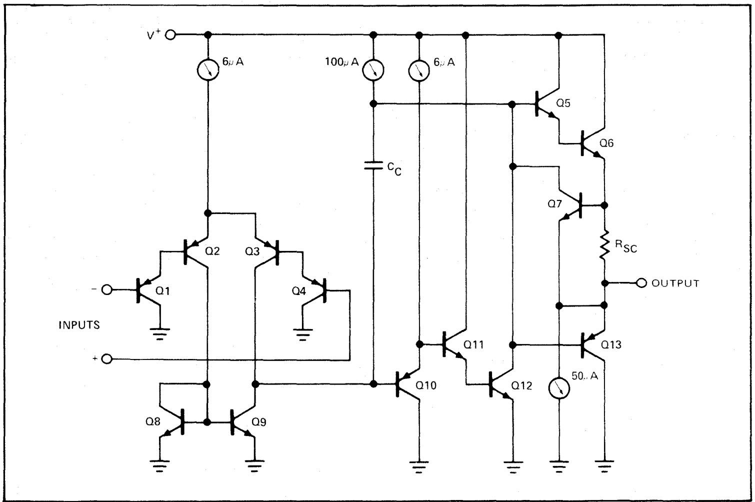
H PACKAGE*



ORDER NUMBERS
LM158/258/358H
NE/SE532H

*Metal cans (H) not recommended for new designs

EQUIVALENT CIRCUIT



LOW POWER DUAL OPERATIONAL AMPLIFIERS NE/SA/SE532/LM158/258/358

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, V+ = +5V unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE532, LM158/258			NE/SA532/LM358			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OS} Offset voltage[1]	$R_S \leq 0\Omega$		±2	±5		±2	±7	mV
	$R_S \leq 0\Omega$, over temp.			±7			±9	mV
V_{OS} Drift	$R_S = 0\Omega$, over temp.		7			7		µV/°C
I_{OS} Offset current	$I_{IN}(+) - I_{IN}(-)$		±3	±30		±5	±50	nA
	Over temp.			±100			±150	nA
I_{OS} Drift			10			10		pA/°C
I_{BIAS} Input current[2]	$I_{IN}(+)$ or $I_{IN}(-)$		45	150		45	250	nA
	Over temp., $I_{IN}(+)$ or $I_{IN}(-)$		40	300		40	500	nA
V_{CM} Common mode voltage range[3]	V+ = 30V	0		V+-1.5	0		V+-1.5	V
	Over temp., V+ = 30V	0		V+-2.0	0		V+-2.0	V
C_{MRR} Common mode rejection ratio		70	85		65	70		dB
V_{OUT} Output voltage swing (V_{OH})	$R_L \geq 2k\Omega$, V+ = 30V, over temp	26			26			V
	$R_L \geq 10k\Omega$, V+ = 30V, over temp	27	28		27	28		V
V_{OUT} Output voltage swing (V_{OL})	$R_L \leq 10k\Omega$, over temp.		5	20		5	20	mV
I_{CC} Supply current	$R_L = \infty$, V+ = 30V		1.0	2.0		1.0	2.0	mA
	$R_L = \infty$ on all amplifiers, over temp		0.5	1.2		0.5	1.2	mA
A_{VOL} Large signal voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} ± 10V, V+ = 15V	50	100		25	100		V/mV
	(for large V_O swing) Over temp.	25			15			V/mV
PSRR Supply voltage rejection ratio	$R_S \leq 0\Omega$	65	100		65	100		dB
Amplifier-to-amplifier coupling[4]	f = 1kHz to 20kHz (input referred)		-120			-120		dB
Output current Source	$V_{IN}+$ = +1Vdc, $V_{IN}-$ = 0Vdc, V+ = 15Vdc	20	40		20	40		mA
	$V_{IN}+$ = +1Vdc, $V_{IN}-$ = 0Vdc, V+ = 15Vdc, over temp.	10	20		10	20		mA
Sink	$V_{IN}-$ = +1Vdc, $V_{IN}+$ = 0Vdc, V+ = 15Vdc	10	20		10	20		mA
	$V_{IN}-$ = +1Vdc, $V_{IN}+$ = 0Vdc, V+ = 15Vdc, over temp.	5	8		5	8		mA
	$V_{IN}+$ = 0V, $V_{IN}-$ = +1Vdc, V_O = 200mV	12	50		12	50		µA
I_{SC} Short circuit current[5]			40	60		40	60	mA
Differential input voltage[6]				V+			V+	V

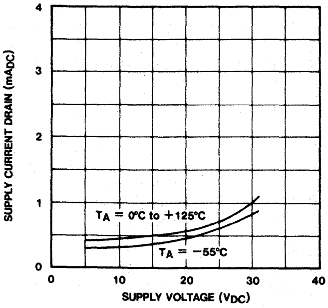
NOTES

1. $V_O \cong 1.4V$, $R_S = 0\Omega$ with V+ from 5V to 30V; and over the full input common-mode range (0V to V+ −1.5V).
2. The direction of the input current is out of the IC due to the pnp input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ −1.5V, but either or both inputs can go to +32V without damage.
4. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance coupling increases at higher frequencies.
5. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of +15Vdc, continuous short-circuits can exceed the power dissipation ratings and case eventual destruction.
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ −1.5V, but either or both inputs can go to +32Vdc without damage.
7. For operating at high temperatures, all devices must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient.

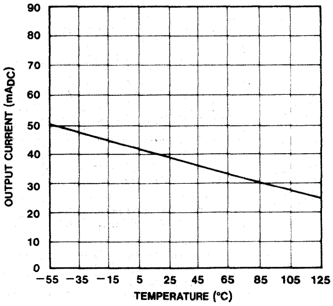
LOW POWER DUAL OPERATIONAL AMPLIFIERS NE/SA/SE532/LM158/258/358

TYPICAL PERFORMANCE CHARACTERISTICS

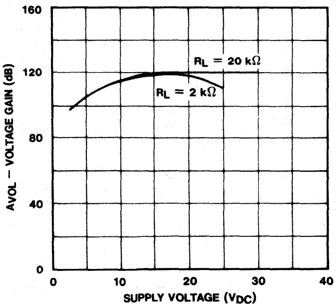
SUPPLY CURRENT



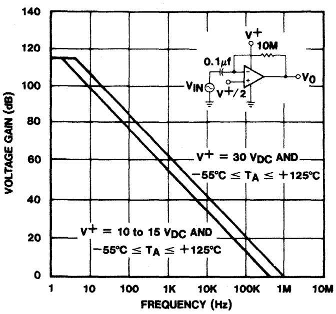
CURRENT LIMITING



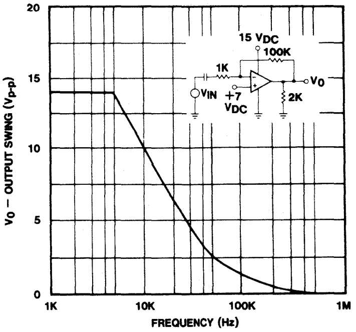
VOLTAGE GAIN



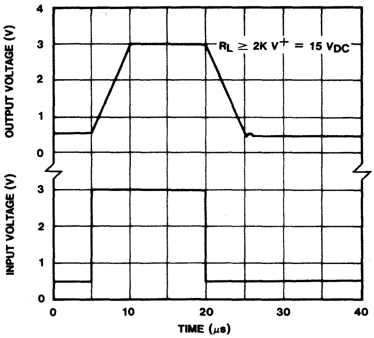
OPEN LOOP FREQUENCY RESPONSE



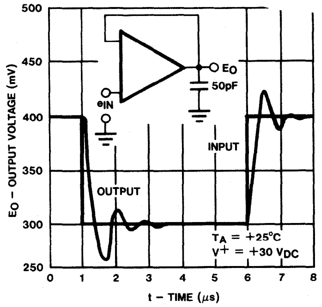
LARGE SIGNAL FREQUENCY RESPONSE



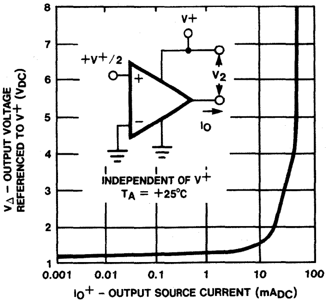
VOLTAGE FOLLOWER PULSE RESPONSE



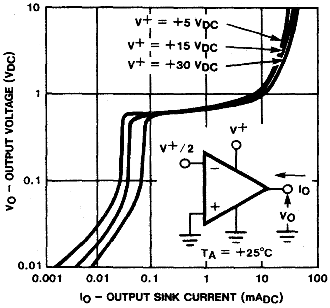
VOLTAGE FOLLOWER PULSE RESPONSE (SMALL SIGNAL)



OUTPUT CHARACTERISTICS CURRENT SOURCING

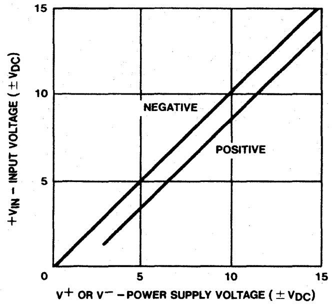


OUTPUT CHARACTERISTICS CURRENT SINKING

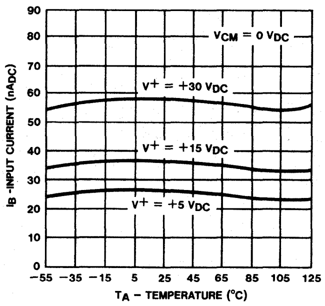


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

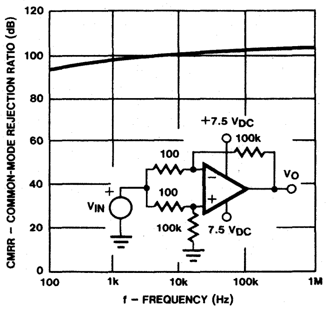
INPUT VOLTAGE RANGE



INPUT CURRENT



COMMON MODE REJECTION RATIO



DUAL GENERAL-PURPOSE OPERATIONAL AMPLIFIER

NE/SA/SE4558

DESCRIPTION

The 4558 is a dual operational amplifier internally compensated. The use of planar epitaxial process for silicon chip construction gives the IC unique performance characteristics.

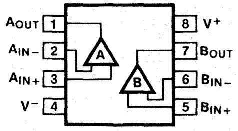
Excellent channel separation allows the use of a dual device in a single amp application, providing the highest packaging density. The NE/SA/SE4558 is a pin for pin replacement for the RC/RM/RV4558.

FEATURES

- **2.5MHz unity gain bandwidth guaranteed**
- **Supply voltage ±22V for SE4558 and ±18V for NE4558**
- **Short circuit protection**
- **No frequency compensation required**
- **No latch-up**
- **Large common mode and differential voltage ranges**
- **Low power consumption**

PIN CONFIGURATION

D, FE, N PACKAGES



TOP VIEW

ORDER NUMBERS

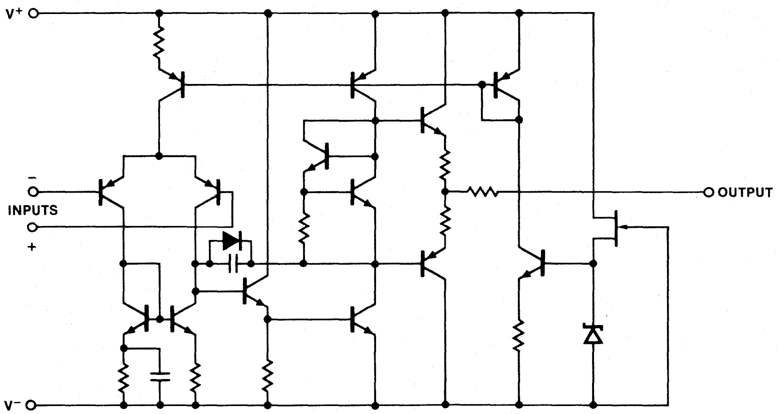
NE4558D
NE4558FE
NE4558N
SA4558FE
SE4558FE
SA4558N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
SE4558:	±22	V
NE4558, SA4558:	±18	V
Internal power dissipation (Note 1)	500	mW
Differential input voltage	±30	V
Input voltage (Note 2)	±15	V
Storage temperature range	−65 to +150	°C
Operating temperature range		
SE4558:	−55 to +125	°C
SA4558:	−40 to +85	°C
NE4558:	0 to +70	°C
Lead temperature (soldering, 60s)	300	°C
Output short circuit duration (Note 3)	Indefinite	

NOTES
1. Rating applies for case temperatures to +125°C; derate linearly at 5.6 mw/°C for ambient temperatures above +75°C for SE4558.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground on one amp only. Rating applies to +125°C case temperature or +75°C ambient temperature for NE4558 and to +85°C ambient temperature for SA4558.

EQUIVALENT SCHEMATIC



DUAL GENERAL-PURPOSE OPERATIONAL AMPLIFIER NE/SA/SE4558

ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 15V$, $T_A = 25°C$ unless otherwise specified

PARAMETER	TEST CONDITIONS	SE4558			NE/SA4558			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage	$R_S \leq 10k\Omega$		1.0	5.0		2.0	6.0	mV
Input offset current			50	200		30	200	nA
Input bias current			40	500		200	500	nA
Input resistance		0.3	1.0		0.3	1.0		MΩ
Large signal voltage gain	$R_L \geq 2K\Omega$ $V_{OUT} = \pm 10V$	50,000	300,000		20,000	300,000		
Output voltage swing	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	± 12 ± 10	± 14 ± 13		± 12 ± 10	± 14 ± 13		V
Input voltage range		± 12	± 13		± 12	± 13		V
Common mode rejection ratio	$R_S \leq 10k\Omega$	70	100		70	100		dB
Supply voltage rejection ratio	$R_S \leq 10k\Omega$		10	150		10	150	μV/V
Power consumption (all amplifiers)	$R_L = \infty$		100	170		100	170	mW
Transient response (unity gain)	$V_{IN} = 20mV$ $R_L = 2K\Omega$ $C_L \leq 100pF$							
Risetime			100			100		ns
Overshoot			15.0			15.0		%
Slew rate (unity gain)	$R_L \geq 2k\Omega$		1.0			1.0		V/μs
Channel separation (gain = 100)	f = 10kHz $R_S = 1k\Omega$		90			90		dB
Unity gain bandwidth (gain = 1)		2.5	3.0		2.0	3.0		MHz

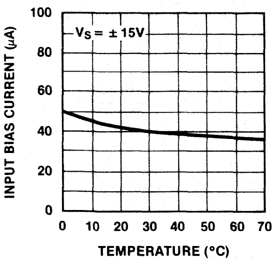
The following specifications apply for $-55°C \leq T_A \leq +125°C$ for SE4558; $0°C \leq T_A \leq +70°C$ for NE4558; $-40°C \leq T_A \leq +85°C$ for SA4558

Input offset voltage	$R_S \leq 10k\Omega$			6.0			7.5	mV
Input offset current				500			300/500*	nA
Input bias current				1500			800/1500*	nA
Large signal voltage gain	$R_L \geq 2k\Omega$ $V_{OUT} = \pm 10V$	25,000			15,000			
Output voltage swing	$R_L \geq 2k\Omega$	± 10			± 10			V
Power consumption	$V_S = \pm 15V$ $T_A = HIGH$ $T_A = LOW$		90 120	150 200		90 120	150 200	mW

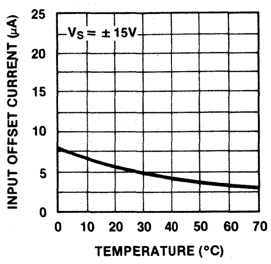
*SA4558

TYPICAL PERFORMANCE CURVES

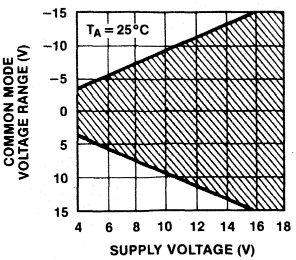
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



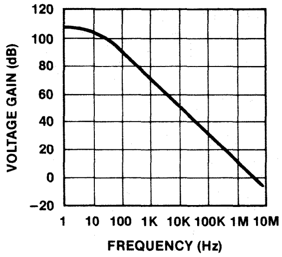
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



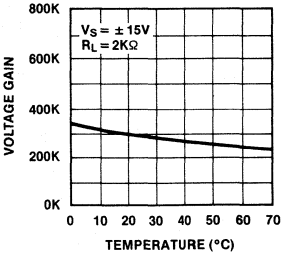
COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



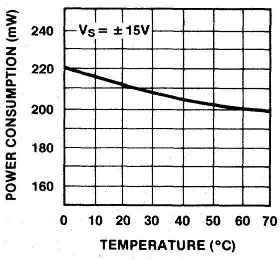
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



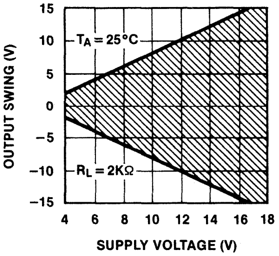
OPEN LOOP GAIN AS A FUNCTION OF TEMPERATURE



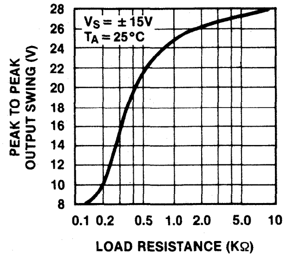
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



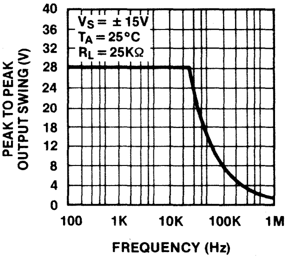
TYPICAL OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



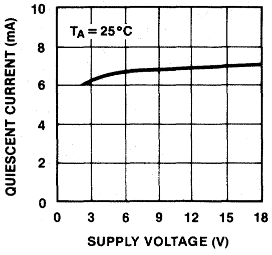
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



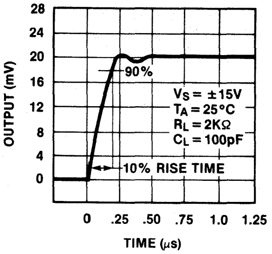
DUAL GENERAL-PURPOSE OPERATIONAL AMPLIFIER NE/SA/SE4558

TYPICAL PERFORMANCE CURVES (Continued)

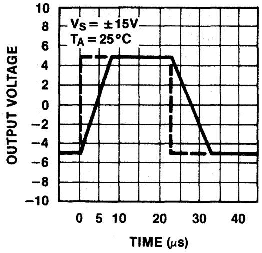
QUIESCENT CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



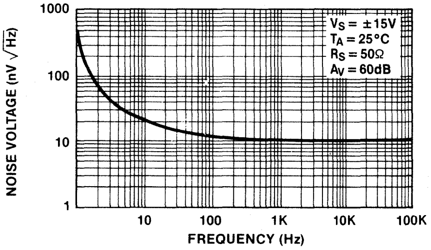
TRANSIENT RESPONSE



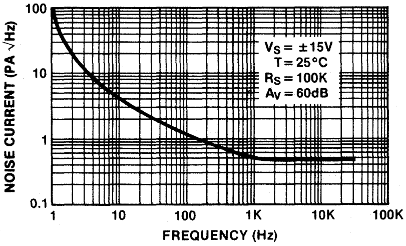
VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE



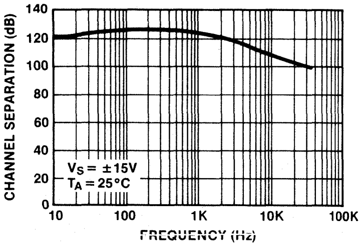
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



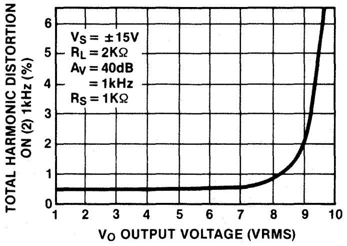
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



CHANNEL SEPARATION

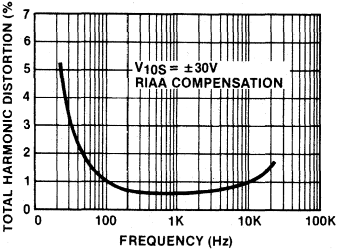


TOTAL HARMONIC DISTORTION vs OUTPUT VOLTAGE



DISTORTION vs FREQUENCY

V_O = 1vrms



SINGLE OR DUAL HIGH SLEW RATE OP AMP

NE/SE535/5535

DESCRIPTION

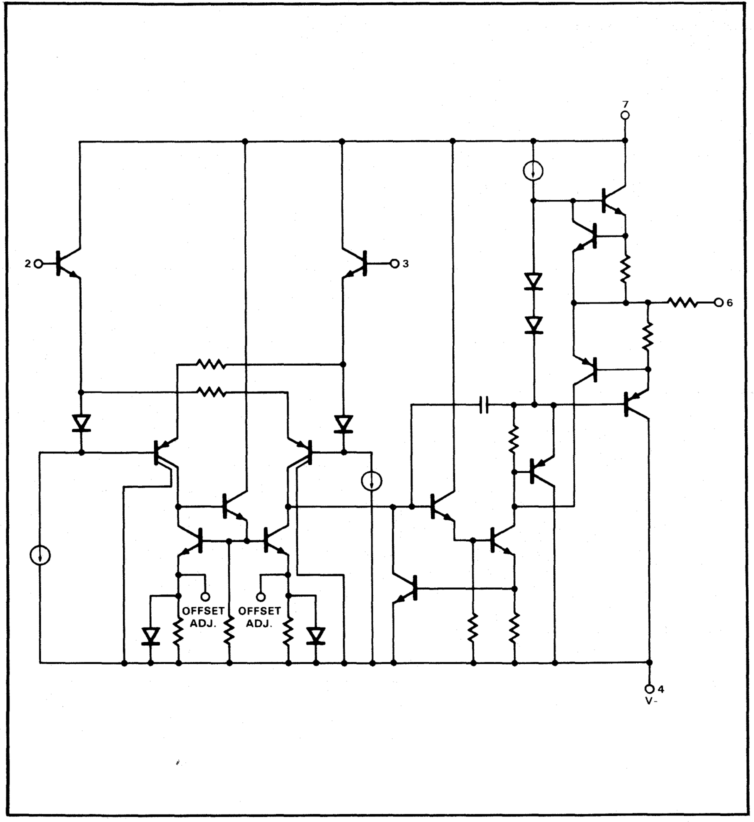
The 535 and 5535 are new generation operational amplifiers featuring high slew rates combined with improved input characteristics. The 535 is a single device while the 5535 is a dual configuration. Internally compensated for unity gain, the SE535 and SE5535 feature a guaranteed unity gain slew rate of 10V/μs with 2mV maximum offset voltage. Industry standard pin out and internal compensation allow the user to upgrade system performance by directly replacing general purpose amplifiers, such as 741, 747 and 1558.

FEATURES

- **15V/μs unity gain slew rate**
- **Internal frequency compensation**
- **Low input offset voltage—2mV**
- **Low input bias current 80nA max**
- **Short circuit protected**
- **Offset null capability**
- **Large common mode and differential voltage ranges**

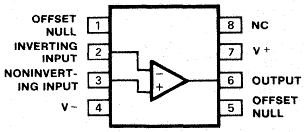
	535	5535
• **Pin compatibility**	**741**	**747,1558**
• **Configuration**	**Single**	**Dual**

EQUIVALENT SCHEMATIC (One Amplifier)



PIN CONFIGURATIONS

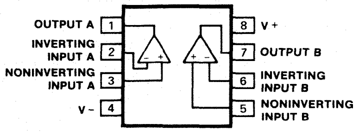
FE, N PACKAGE



TOP VIEW

ORDER NUMBERS
SE535N, FE NE535N, FE

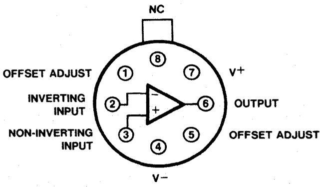
N PACKAGE



TOP VIEW

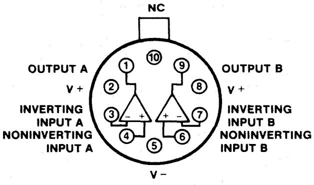
ORDER NUMBERS
SE5535N NE5535N

H PACKAGE*



ORDER NUMBERS
SE535H NE535H

H PACKAGE*



ORDER NUMBERS
SE5535H NE5535H

*Metal cans (H) not recommended for new designs

SINGLE OR DUAL HIGH SLEW RATE OP AMP NE/SE535/5535

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SE535/ SE5535	NE535/ NE5535	UNIT
Supply voltage	±22	±18	V
Internal power dissipation[1]			
N Package	500	500	mW
H Package	800	800	mW
F Package	1000	1000	mW
Differential input voltage	±30	±30	V
Input voltage[2]	±15	±15	V
Operating temperature range	-55 to +125	0 to +70	°C
Storage temperature range	-65 to +150	-65 to +150	°C
Lead temperature (solder, 60sec)	300	300	°C
Output short circuit[3]	Indefinite	Indefinite	

NOTES

1. Rating applies for thermal resistances junction to ambient of 240°C/W and 150°C/W for N and H packages, respectively. Maximum chip temperature is 150°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = ±15V$ unless otherwise specified.*

PARAMETER		TEST CONDITIONS	SE535/SE5535			NE535/NE5535			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S \leq 10k\Omega$		0.7	4.0		2.0	6.0	mV
		$R_S \leq 10k\Omega$, over temp.			5.0			7.0	mV
ΔV_{OS}	Input offset voltage drift	$R_S = 0\Omega$, over temp.		4.0			6.0		μV/°C
I_{OS}	Input offset current			5	20		15	40	nA
		Over temp.			40			80	VnA
I_B	Input current			45	80		65	150	nA
		Over temp.			200			200	nA
V_{CM}	Common mode voltage range		±12	±13		±12	±13		V
CMRR	Common mode rejection ratio	$R_S \leq 10k\Omega$, over temp.	70	90		70	90		dB
PSRR	Power supply rejection	$R_S \leq 10k\Omega$, over temp.		30	150		30	150	μV/V
R_{IN}	Input resistance		3	10		1	6		MΩ
A_{VOL}	Large signal voltage gain	$R_L \geq 2k\Omega$, $V_{OUT} = ±10V$	50	500		50	500		V/mV
		$R_L \geq 2k\Omega$, $V_{OUT} = ±10V$, over temp.	25			25			V/mV
V_{OUT}	Output voltage	$R_L \geq 2k\Omega$, over temp.	±10	±13		±10	±13		V
		$R_L \geq 10k\Omega$, over temp.	±12	±14		±12	±14		V
I_{CC}	Supply current	Per amplifier		1.8	2.8		1.8	2.8	mA
		Per amplifier, over temp.		2	3.3		2		mA
P_D	Power dissipation	Per amplifier		54	84		54	84	mW
		Per amplifier, over temp.		60	99		60		mW
I_{SC}	Output short circuit current			25			25		mA
R_{OUT}	Output resistance			100			100		Ω

*NOTE

Temperature range

SE types -55°C ≤ T_A ≤ 125°C

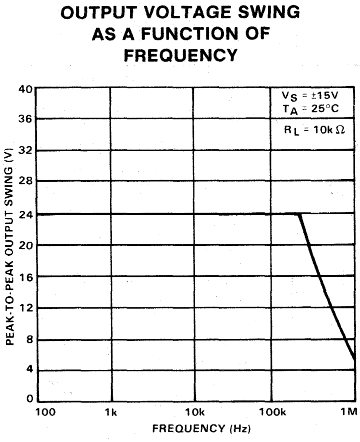
NE types 0°C ≤ T_A ≤ 70°C

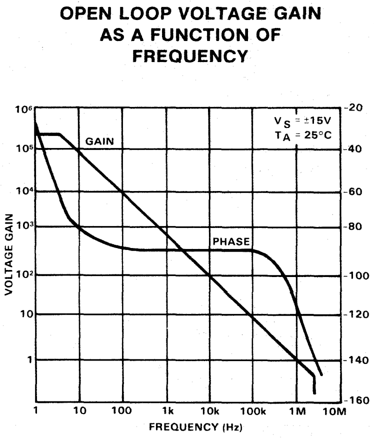
SINGLE OR DUAL HIGH SLEW RATE OP AMP NE/SE535/5535

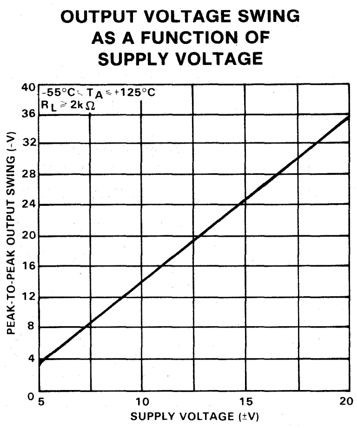
AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

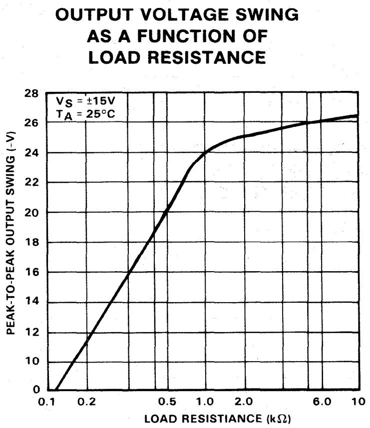
PARAMETER	TEST CONDITIONS	SE535/SE5535			NE535/NE5535			UNIT
		Min	Typ	Max	Min	Typ	Max	
Gain/bandwidth product			1			1		MHz
Transient response								
Small signal rise time			0.25			0.25		μs
Small signal overshoot			6			6		%
Settling time	To 0.1%		3			3		μs
Slew rate	$R_L \geq 10k\Omega$, unity gain, non-inverting	10	15		10	15		V/μs

TYPICAL PERFORMANCE CHARACTERISTICS


OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY


OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

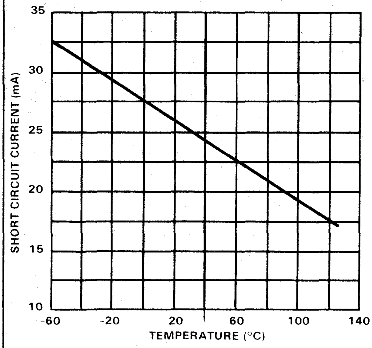

OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE


OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

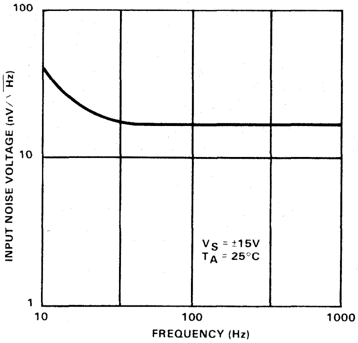
SINGLE OR DUAL HIGH SLEW RATE OP AMP NE/SE535/5535

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

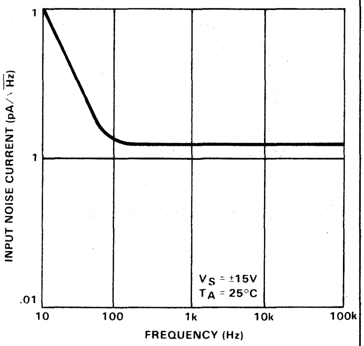
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



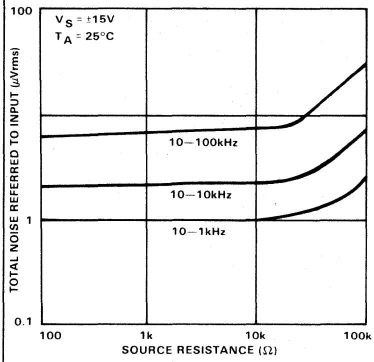
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



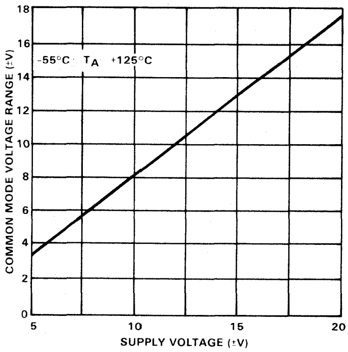
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



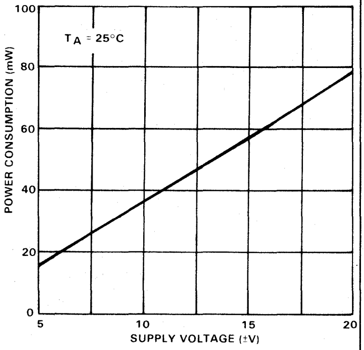
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



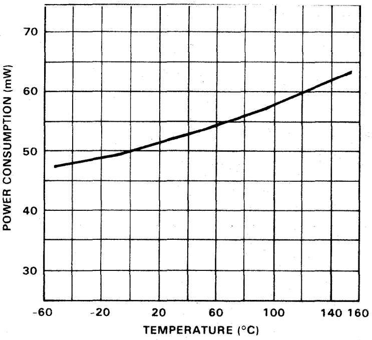
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



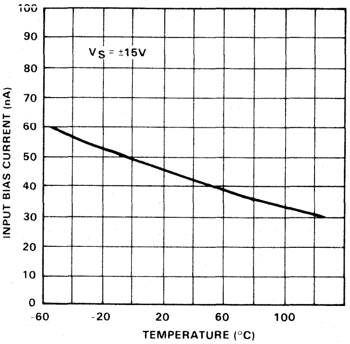
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



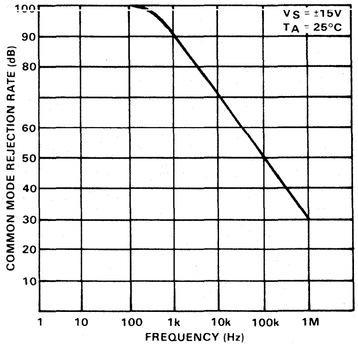
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



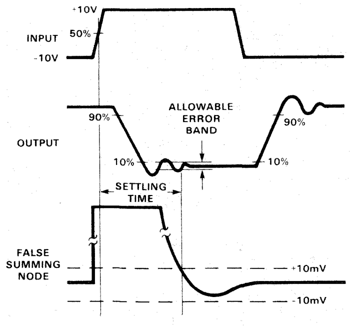
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



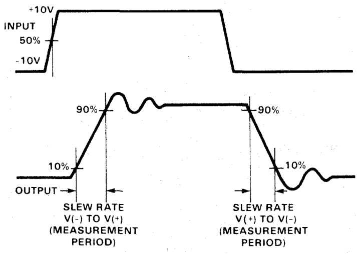
SINGLE OR DUAL HIGH SLEW RATE OP AMP NE/SE535/5535

VOLTAGE WAVEFORMS

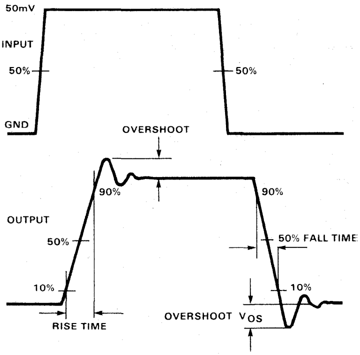
SETTLING TIME MEASUREMENT



SLEW RATE MEASUREMENT

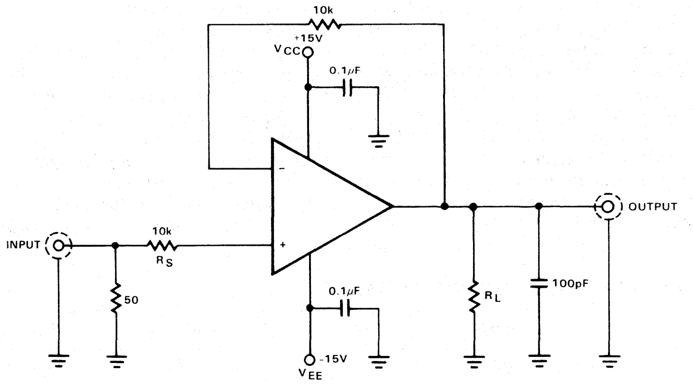


SMALL-SIGNAL TRANSIENT RESPONSE DEFINITIONS



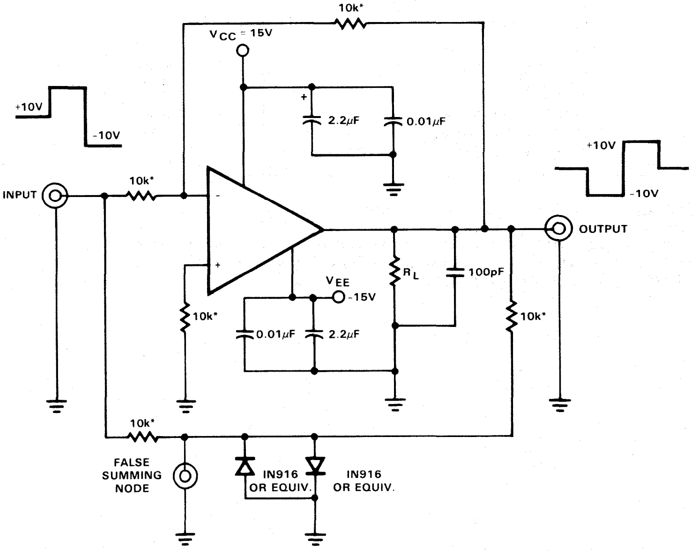
TEST CIRCUITS

SLEW RATE AND SMALL SIGNAL TRANSIENT RESPONSE



NOTE
Pins not shown are not connected.
All resistors values are typical and in ohms.

SETTLING TIME



*Match to within 0.01%.

NOTE

Pins not shown are not connected.
All resistors values are typical and in ohms.

DUAL HIGH SLEW RATE OP AMPS

NE/SE538/5538

DESCRIPTION

The NE/SE538/5538 are new generation operational amplifiers featuring high slew rates combined with improved input characteristics. Internally compensated for gains of 5 or larger, the SE538/5538 offers guaranteed minimum slew rates of 40V/μs or larger. Featuring 2mV max input offset voltage, the 538 is a single amplifier while the 5538 is a dual amplifier. Industry standard pin out and internal compensation allow the user to upgrade system performance by directly replacing general purpose amplifiers, such as 748, 101A, 741, 747 and 1458.

FEATURES

- **2mV input offset voltage**
- **80nA max input offset current**
- **Short circuit protected**
- **Offset null capability**
- **Large common mode and differential voltage ranges**
- **60V/μs slew rate (gain of +5, -4 min)**
- **6MHz gain bandwidth product (gain +5, -4 minimum)**
- **Internal frequency compensation (gain of +5, -4 minimum)**
- **Pin out: 538 same as 741 (single)**
  5538 same as 747, 1458 (dual)

ABSOLUTE MAXIMUM RATINGS[1,2,3]

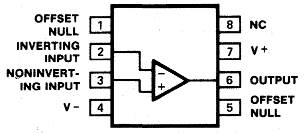
PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		
	SE military grade	±22	V
	NE commercial grade	±18	V
P_D	Internal power dissipation FE package	1000	mW
P_D	Internal power dissipation[1] N package	500	mW
P_D	Internal power dissipation[1] H package	800	mW
	Differential input voltage	±30	V
	Input voltage[2]	±15	V
	Operating temperature range		
	SE military grade	-55 to +125	°C
	NE commercial grade	0 to 70	°C
	Output short circuit[3]	indefinite	
	Storage temperature range	-65 to +150	°C
	Lead temperature (solder, 60sec.)	300	°C

NOTES

1. Rating applies for thermal resistances of 240°C/W and 150°C/W junction to ambient for N and H packages. Maximum chip temperature is 150°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.

PIN CONFIGURATIONS

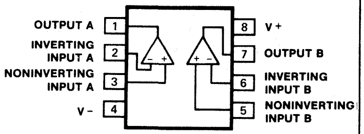
FE, N PACKAGE



TOP VIEW

ORDER NUMBERS
SE538N, FE NE538N, FE

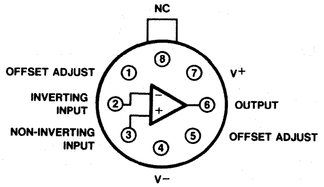
N PACKAGE



TOP VIEW

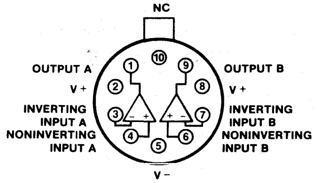
ORDER NUMBERS
SE5538N NE5538N

H PACKAGE*



ORDER NUMBERS
SE538H NE538H

H PACKAGE*

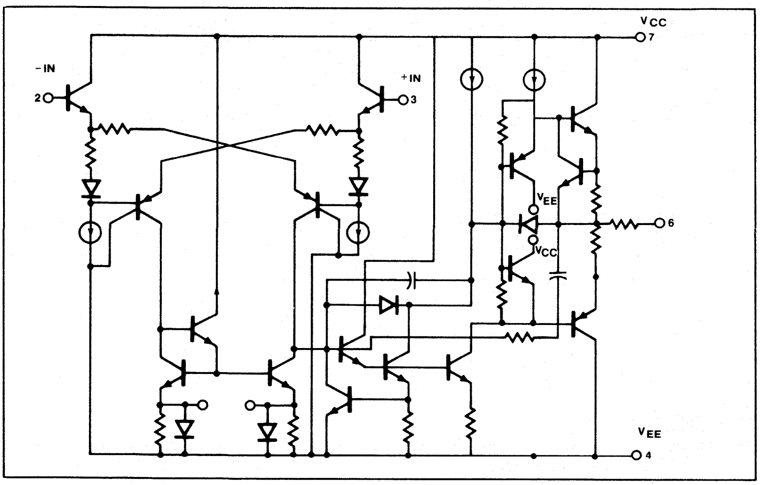


ORDER NUMBERS
SE5538H NE5538H

*Metal cans (H) not recommended for new designs

DUAL HIGH SLEW RATE OP AMPS NE/SE538/5538

EQUIVALENT SCHEMATIC (EACH AMPLIFIER)



DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SE538/SE5538			NE538/NE5538			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S \leq 10k\Omega$ $R_S \leq 10k\Omega$, over temp.		0.7	4.0 5.0		2.0	6.0 7.0	mV mV
ΔV_{OS}	Input offset voltage drift	$R_S = 0\Omega$, over temp.		4.0			6.0		$\mu V/°C$
I_{OS}	Input offset current	 Over temp.		5	20 40		15	40 80	nA nA
I_B	Input current	 Over temp.		45	80 200		65	150 200	nA nA
V_{CM}	Input common mode voltage range		±12	±13		±12	±13		V
CMRR	Common mode rejection ratio	$R_S \leq 10k\Omega$, over temp.	70	90		70	90		dB
PSRR	Power supply rejection	$R_S \leq 10k\Omega$, over temp.		30	150		30	150	$\mu V/V$
R_{IN}	Input resistance		3	10		1	6		$M\Omega$
A_{VOL}	Large signal voltage gain	$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$ Over temp., $R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	50 25	200		50 25	200		V/mV V/mV
V_{OUT}	Output voltage	Over temp., $R_L \geq 2k\Omega$ Over temp., $R_L \geq 10k\Omega$	±10 ±12	±13 ±14		±10 ±12	±13 ±14		V V
I_{CC}	Supply current	Per amplifier Over temp., per amplifier		2 2.2	3 3.6		2 2.2	3	mA mA
P_D	Power dissipation	Per amplifier Over temp., per amplifier		60 66	90 108		60 66	90	mW mW
I_{SC}	Output short circuit current			25			25		mA
R_{OUT}	Output resistance			100			100		Ω

NOTE

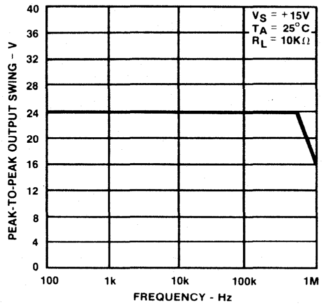
Temperature Range
SE Types $-55°C \leq T_A \leq 125°C$
NE Types $0°C \leq T_A \leq 70°C$

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

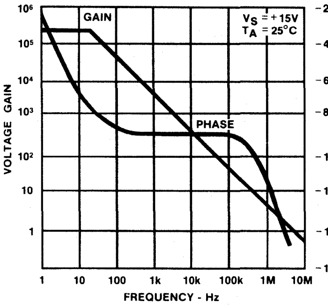
PARAMETER	TEST CONDITIONS	SE538/SE5538			SE538/NE5538			UNIT
		Min	Typ	Max	Min	Typ	Max	
Gain bandwidth product (Gain +5, -4 minimum)			6			6		MHz
Transient response Small signal rise time Small signal overshoot			0.25 6			0.25 6		μs %
Settling time	To 0.1%		1.2			1.2		μs
Slew rate	Minimum gain = 5 Noninverting $R_L \geq 2k\Omega$	40	60			60		V/μs

TYPICAL PERFORMANCE CHARACTERISTICS

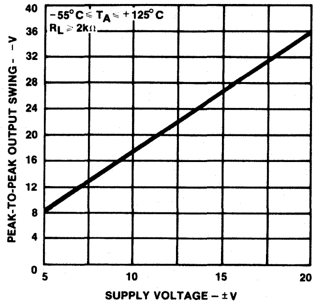
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



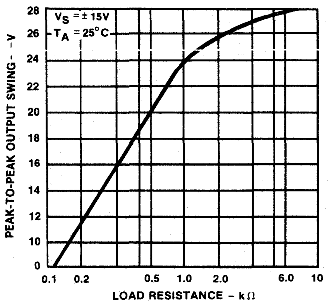
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



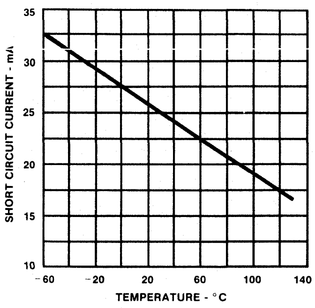
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



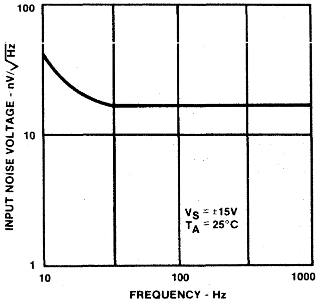
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

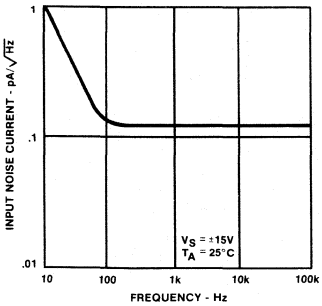


INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY

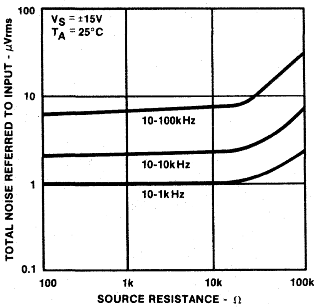


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

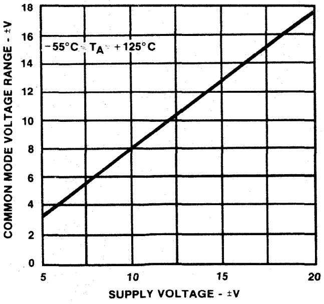
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



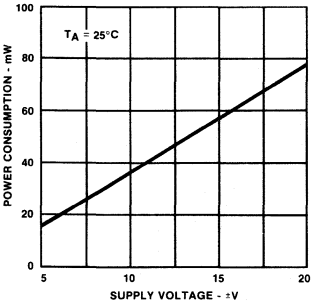
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



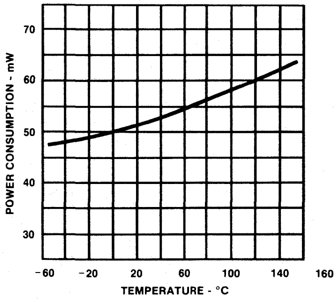
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



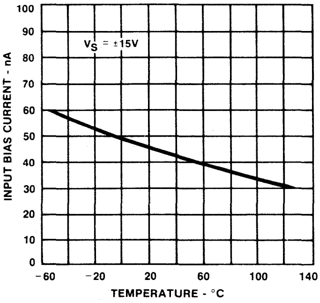
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



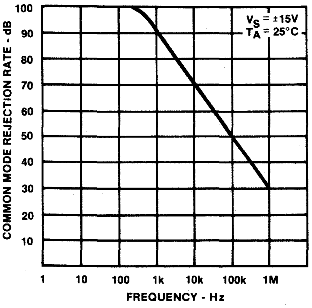
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



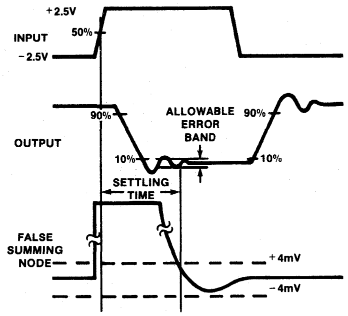
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



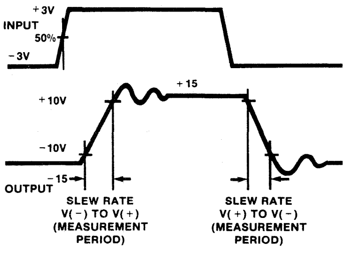
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



SETTLING TIME MEASUREMENT WAVEFORMS



SLEW RATE MEASUREMENT VCC = ±20V

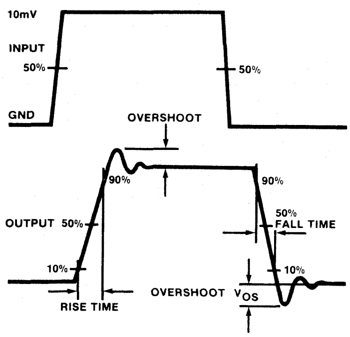


DUAL HIGH SLEW RATE OP AMPS

NE/SE538/5538

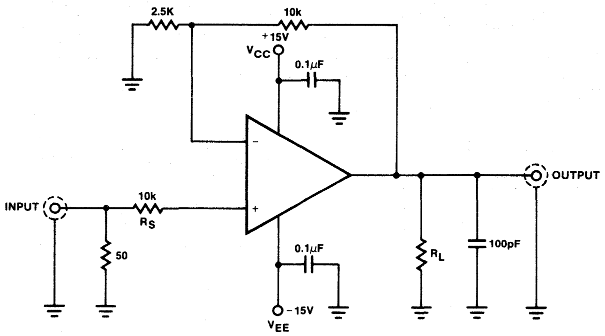
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

SMALL-SIGNAL TRANSIENT RESPONSE DEFINITIONS



TEST LOAD CIRCUITS

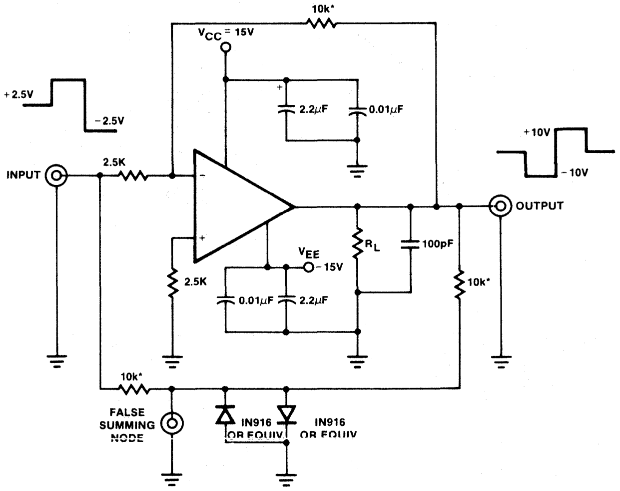
SLEW RATE AND SMALL SIGNAL TRANSIENT RESPONSE TEST CIRCUIT



NOTE
Pins not shown are not connected.
All resistors values are typical and in ohms.

TEST LOAD CIRCUITS (Cont'd)

SETTLING TIME TEST CIRCUIT



*Match to within 0.01%.
NOTE

Pins not shown are not connected.
All resistors values are typical and in ohms.

DUAL HIGH PERFORMANCE OPERATIONAL AMPLIFIER NE/SE5512

DESCRIPTION

The 5512 series of high performance operational amplifier provides very good input characteristics. These amplifiers feature low input bias and voltage characteristics such as a 108 op amp with improved CMRR and a high differential input voltage limit achieved through the use of a bias cancellation and PNP input circuits with collector to emitter clamping. The output characteristics are like those of a 741 op amp with improved slew rate and drive capability yet have low supply quiescent current.

APPLICATIONS

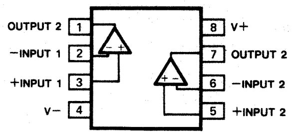
- AC amplifiers
- RC active filters
- Transducer amplifiers
- DC gain block
- Battery operation
- Instrumentation amplifiers

FEATURES

- **Low input bias < ±3nA**
- **Low input offset current < ±3nA**
- **Low input offset voltage < 1mV**
- **Low V_{OS} temperature drift 4μV/°C**
- **Low input bias temperature drift 30pA/°C**
- **Low input voltage noise 25nV/$\sqrt{Hz}$**
- **Low supply current 1.5mA/amp**
- **High slew rate 1.0V/μs**
- **High CMRR 100dB**
- **High input impedance 100MΩ**
- **High PSRR 110dB**
- **High differential input voltage limit**
- **No cross-over distortion**
- **Indefinite output short circuit protection**
- **Internally compensated for unity gain**

PIN CONFIGURATIONS

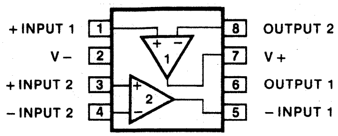
FE,N PACKAGE



TOP VIEW

ORDER NUMBERS
NE/SE5512FE NE/SE5512N

D PACKAGE



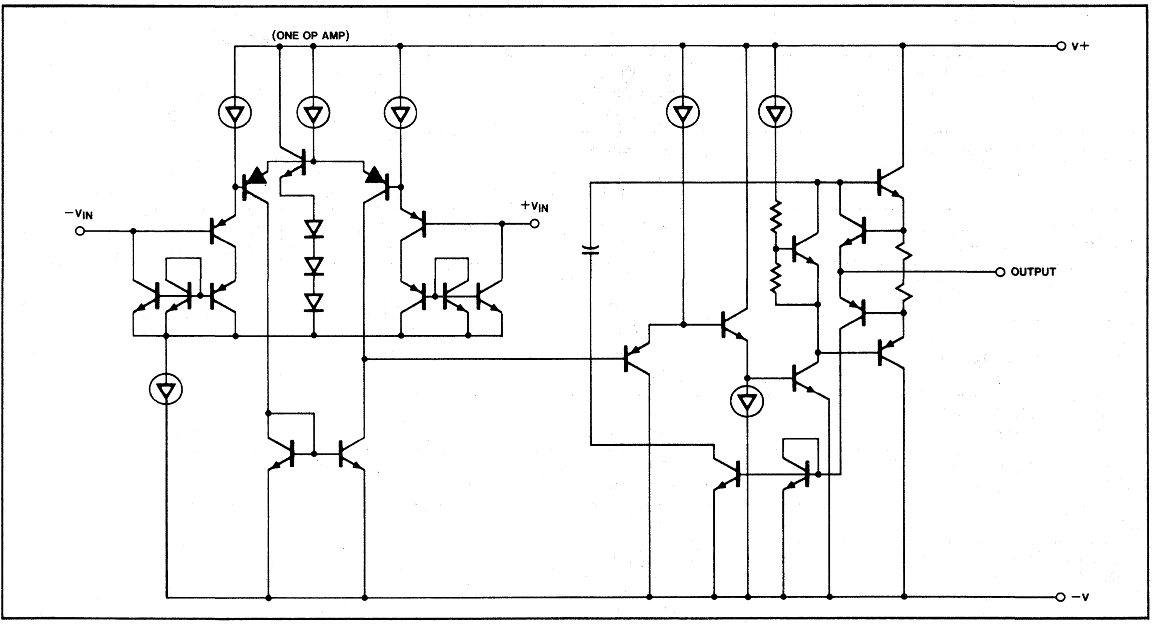
TOP VIEW

ORDER NUMBER
NE5512D

ABSOLUTE MAXIMUM RATINGS

Parameter		Rating	Unit
V_{CC}	Supply Voltage	±16	V
V_D	Power dissipation	500	mW
T_A	Operating temperature range		
	NE5512	0 to 70	°C
	SE5512	−55 to +125	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead temperature soldering	300	°C

EQUIVALENT SCHEMATIC



ELECTRICAL PERFORMANCE CHARACTERISTICS $V_{CC} = \pm 15V$, F.R. = −55°C to +125°C (SE), 0°C to +70°C (NE)

PARAMETER		TEST CONDITIONS	SE5512			NE5512			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S = 100\Omega$ $T_A = +25°C$ T_A = F.R.		0.7 1	2 3		1 1.5	5 6	mV
I_{OS}	Input offset current	$R_S = 100k\Omega$ $T_A = +25°C$ T_A = F.R.		3 4	10 20		6 8	20 30	nA
I_B	Input bias current	$R_S = 100k\Omega$ $T_A = +25°C$ T_A = F.R.		3 4	10 20		6 8	20 30	nA
R_{IN}	Input resistance Differential	$T_A = 25°C$		100			100		MΩ
V_{CM}	Input common mode range	$T_A = 25°C$ T_A = F.R.	±13.5 ±13	±13.7 ±13.2		±13.5 ±13	±13.7 ±13.2		V
CMRR	Input common-mode rejection ratio	$V_{CC} = \pm 15V$ $V_{IN} = \pm 13.5V$ (RM) $T_A = 25°C$ $V_{IN} = \pm 13V$ (F.R.) T_A = F.R.	70	100		70	100		dB
A_{VOL} GAIN	Large-signal voltage gain	$R_L = 2k\Omega$ $T_A = 25°C$ $V_O = \pm 10V$ T_A = F.R.	50 25	200		50 25	200		V/mV
S.R.	Slew rate	$T_A = 25°C$	0.6	1			1		V/μs
GBW	Small-signal unity gain bandwidth	$T_A = 25°C$		3			3		MHz
θ_M	Phase margin	$T_A = 25°C$		45			45		Degree
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$ $T_A = 25°C$ T_A = F.R.	±13 ±12.5	±13.5 ±13		±13 ±12.5	±13.5 ±13		V
V_{OUT}	Output voltage swing	$R_L = 600\Omega$* $T_A = 25°C$ T_A = F.R.	±10 ±8	±11.5 ±9		±10 ±8	±11.5 ±9		V
I_{CC}	Power supply current	R_L = Open $T_A = 25°C$ T_A = F.R.		3.4 3.6	5 5.5		3.4 3.6	5 5.5	mA
P_{SRR}	Power supply rejection ratio	$T_A = 25°C$ T_A = F.R.	80 80	110 100		80 80	110 100		dB
AA	Amplifier to amplifier coupling	f = 1kHz to 20kHz $T_A = 25°C$		−120			−120		dB
HD	Total harmonic distortion	f = 10kHz $T_A = 25°C$ $V_O = 7V_{RMS}$		0.01			0.01		%
V_{IN_N}	Input noise voltage	f = 1kHz $T_A = 25°C$		30			30		nV/√Hz
I_{IN_N}	Input noise current	f = 1kHz $T_A = 25°C$		.2			.2		pA/√Hz

NOTE

* For operation at elevated temperature, N package must be derated based on a thermal resistance of 120°/W junction to ambient. Thermal resistance of the FE package is 125°/W.

BRIDGE TRANSDUCER AMPLIFIER

In applications involving strain gauges, accelerometers and thermal sensors a bridge transducer is often used. Frequently the sensor elements are high resistance units requiring equally high bridge resistance for good sensitivity. This type of circuit then demands an amplifier with high input impedance, low bias current and low drift. The circuit shown represents a possible solution to these general requirements (Figure 1).

For V_S = 10 volts, the common mode voltage is approximately +5 volts, well within the common mode limits of the NE5512.

The sensitivity of the input stage is approximately

$$\frac{RF \cdot Vs}{2R}$$

to a change in transducer resistance ΔR. This gives a gain factor of ≃50 for V_S = 10V and R = 25kΩ. The second stage gain is ×100 giving a total gain of ≃5000.

Noise is minimized by shielding the transducer leads and taking special care to determine a good signal ground. Common mode noise rejection is particularly important making matched differential impedance critical. The NE5512 typically provides 100dB of common mode rejection and will considerably reduce this undesirable effect.

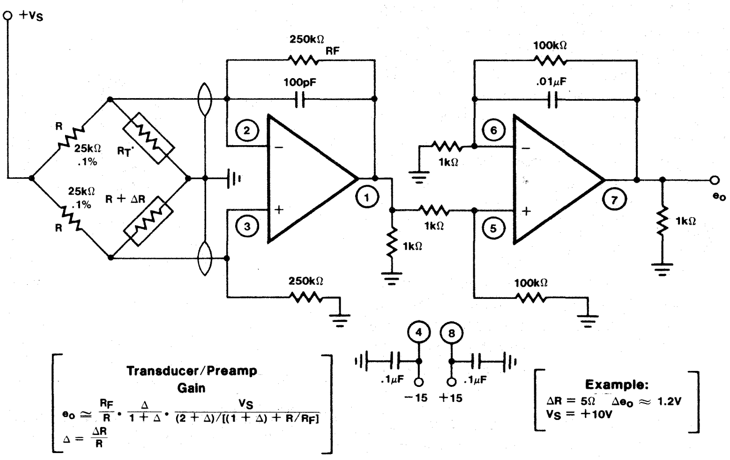
The following are sensitivity figures for the transducer circuits.

	ΔR	ΔE_{out}
leg 1	10Ω	−2.6V
	5Ω	−1.3V
leg 2	10Ω	+2.4
	5Ω	+1.2

Temperature compensation of the bridge element is accomplished by using low drift metal film resistors and also by providing a complimentary non-active sensor element to thermally track the offset in the active element.

High frequency roll-off provides attenuation of unwanted noise above the pass band of the transducer. The shunt capacitors across both stage feedback resistors are for this purpose.

NE/SE5512 BRIDGE TRANSDUCER AMPLIFIER



Transducer/Preamp Gain

$$e_o \simeq \frac{R_F}{R} \cdot \frac{\Delta}{1+\Delta} \cdot \frac{V_S}{(2+\Delta)/[(1+\Delta)+R/R_F]}$$

$$\Delta = \frac{\Delta R}{R}$$

Example:
ΔR = 5Ω $\Delta e_o \approx$ 1.2V
V_S = +10V

*NOTE
Thermal compensation transducer (non-active)

Figure 1

CURRENT TO VOLTAGE CONVERTER

Taking advantage of the very low bias current and offset of the NE5512 is demonstrated in its adaptation to a current to voltage converter as shown below (Figure 2).

NE/SE5512 CURRENT TO VOLTAGE CONVERTER WITH 1% ACCURACY [SENSITIVITY: 1 VOLT PER MICROAMP]

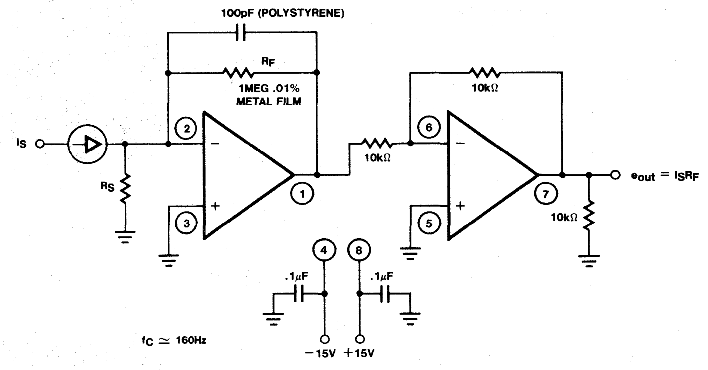


Figure 2

The lower limit of measuring accuracy is determined by I_B (inverting) which is typically 6nA. In order to attain a measurement accuracy of 1% the following inequality must hold,

$$I_B \leqq (.01)\ I_{Smin}$$

Where I_B = input bias current, I_{Smin} = minimum measured current. For I_B = 6nA and I_{Smin} = 1μA,

$$6nA \leqq (.01)\ 1\mu A = 10nA$$

and the inequality hold.

DC offset and current noise gain is determined by

$$\frac{R_F + R_S}{R_S}$$

which ≃ 1 for $R_S \gg R_F$.

The measured results for this circuit appear below (V_{CC} = ± 15 volts).

INPUT CURRENT	OUTPUT VOLTAGE
1μA	1.008 Volts
5μA	5.00 Volts
10.00μA	10.00 Volts

NE5512 OPERATIONAL DIFFERENTIATOR

By utilizing the very high input impedance characteristic of the NE5512, an excellent active differentiator can be realized. Using the circuit shown (Figure 3), good results were obtained as shown by the wave forms in figures 4, 5 and 6. One of the primary problems with such circuits is the tendency toward instability and distortion either due to loading caused by input bias currents or amplifier non-linearity. In addition, gain increases with frequency requiring low input noise in the amplifier.

The relative stability is shown by the output signal wave forms mentioned above. Adding R_1 provides added compensation in the form of a zero near the amplifier unity gain frequency. Frequency range is 100Hz to 10kHz.

In order to obtain good differentiation, the network time constant, RC, must be small relative to the period of the highest frequency present at the input. Since the differentiator will attenuate the signal by a factor of ωRC which may be 100:1 in the operating region, the second amplifier stage is used to compensate for this loss. Various circuits are easily interfaced with the differentiator block due to the inherently low output impedance of the NE5512.

NE/SE5512 ACTIVE DIFFERENTIATOR WITH INVERTING ×10 BUFFER

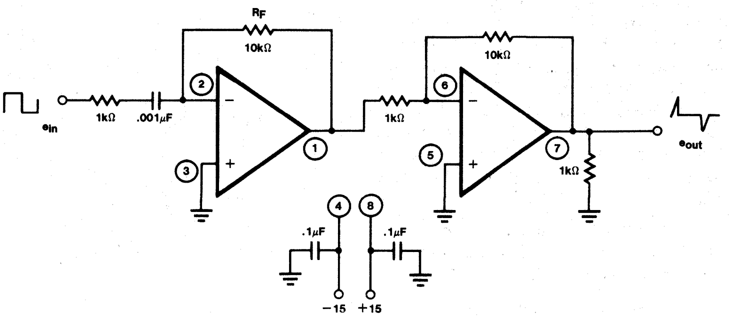


Figure 3

DIFFERENTIATOR WAVEFORMS

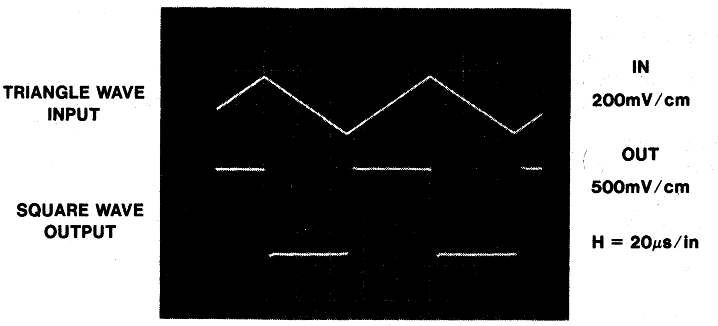


Figure 4

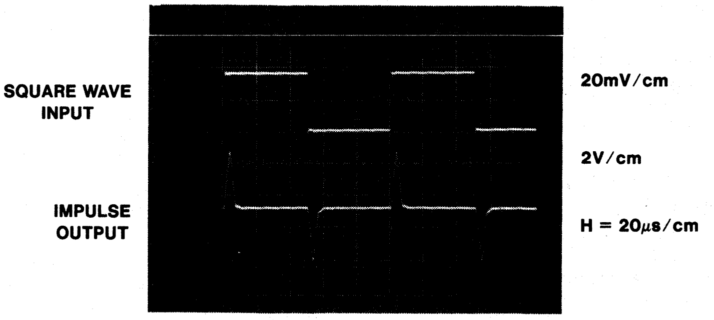


Figure 5

THE OPERATIONAL INTEGRATOR

The operational compliment of the active differentiator is the active integrator. The NE5512 is easily adapted to this function as shown in the circuit below (Figure 7). To obtain satisfactory integration the time constant must fulfill the following requirement:

$$RC \geqq 15T$$

Where T is the period of the input wave form. For the ideal integrator

$$e_{out} = \frac{1}{RC} \int e_{in}\, dt$$

The factor 1/RC represents an attenuation of the input signal. The low signal level is increased by using the second half of the NE5512 as a gain stage following the operational integration. The wave forms in Figures 8 and 9 show the input-output relationship for both a sine wave and a square wave function. A good integrator must exhibit a phase shift of $\geqq 89°$ for sine wave input over the active frequency range. For a square wave the resultant output must be a linear ramp. The circuit shown fulfills this requirement (see Figure 7). No external compensation is required since the amplifier is unity gain stable.

DIFFERENTIATOR WAVEFORMS

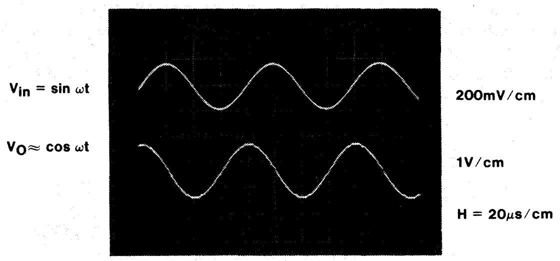


Figure 6

NE/SE5512 ACTIVE INTEGRATOR WITH INVERTING BUFFER

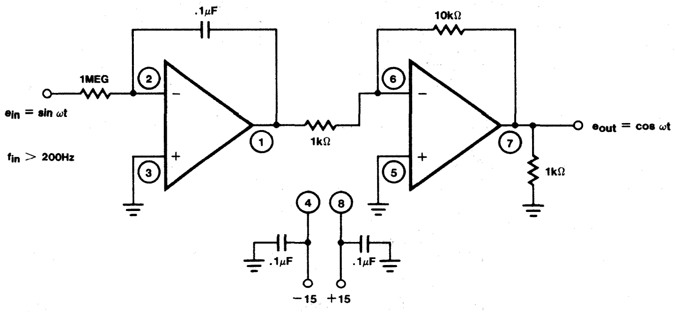


Figure 7

INTEGRATOR WAVEFORMS

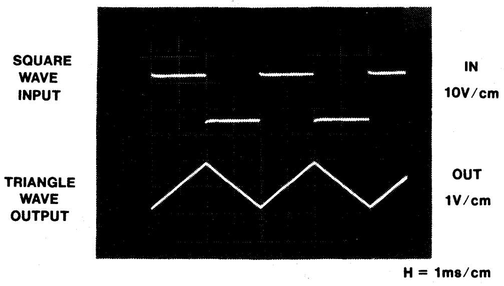


Figure 8

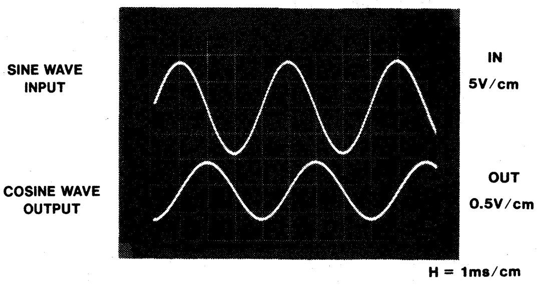


Figure 9

QUAD HIGH PERFORMANCE OP AMP NE/SE5514

DESCRIPTION

The NE/SE5514 family of Quad Operational Amplifiers sets new standards in Bipolar Quad Amplifier Performance. The amplifiers feature low input bias current and low offset voltages. Pin-out is identical to LM324/LM348 which facilitates direct product substitution for improved system performance. Output characteristics are similar to a μA741 with improved slew and drive capability.

FEATURES

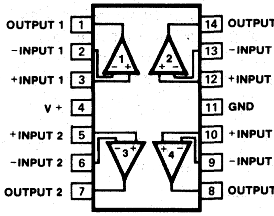
- **Low input bias current: <±3nA**
- **Low input offset current: <±3nA**
- **Low input offset voltage: <1mV**
- **Low supply current: 1.5mA/Amp**
- **1 V/μsec slew rate**
- **High input impedance: 100MΩ**
- **High common mode impedance: 10GΩ**
- **Internal compensation for unity gain**

APPLICATIONS

- **AC amplifiers**
- **RC active filters**
- **Transducer amplifiers**
- **DC gain block**
- **Instrumentation amplifier**

PIN CONFIGURATION

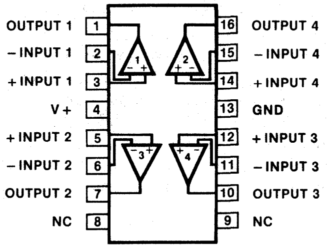
F,N PACKAGE



TOP VIEW

ORDER NUMBERS
NE5514F, N SE5514F, N

D PACKAGE



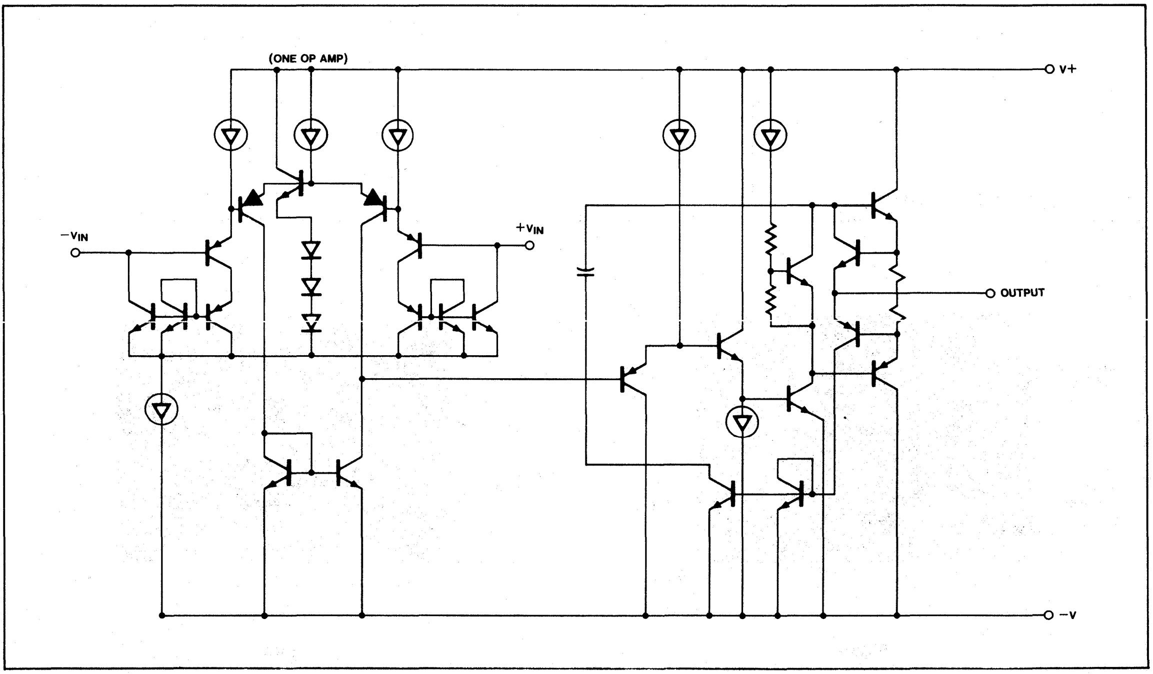
TOP VIEW

ORDER NUMBER
NE5514D

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	±16	V
V_{DIFF}	Differential input voltage	32	V
V_{IN}	Input voltage	0 to 32	V
	Output short to ground	Continuous	
TS	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature	300	°C
T_A	Operating temperature range		
	NE5514	0 to 70	°C
	SE5514	−55 to +125	°C

EQUIVALENT SCHEMATIC



QUAD HIGH PERFORMANCE OP AMP NE/SE5514

ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 15V$, F.R. = −55°C to +125°C (SE) 0°C to 70°C (NE)

PARAMETER		TEST CONDITIONS	SE5514			NE5514			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S = 100\Omega$, $T_A = +25°C$, T_A = F.R.		0.7 1	2 3		1 1.5	5 6	mV
I_{OS}	Input offset current	$R_S = 100k\Omega$, $T_A = +25°C$, T_A = F.R.		3 4	10 20		6 8	20 30	nA
I_B	Input bias current	$R_S = 100k\Omega$, $T_A = +25°C$, T_A = F.R.		3 4	10 20		6 8	20 30	nA
R_{IN}	Input resistance differential	$T_A = 25°C$		100			100		MΩ
V_{CM}	Input common mode range	$T_A = 25°C$, T_A = F.R.	±13.5 ±13.5	±13.7 ±13.2		±13.5 ±13	±13.7 ±13.2		V
CMRR	Input common-mode rejection ratio	$V_{CC} = \pm 15V$, $V_{IN} = \pm 13.5V$ (RM), $T_A = 25°C$, $V_{IN} = \pm 13V$ (F.R.), T_A = F.R.	70	100		70	100		dB
AVOL GAIN	Large-signal voltage gain	$R_L = 2k\Omega$, $T_A = 25°C$ $V_C = \pm 10V$, T_A = F.R.	50 25	200		50 25			V/mV
S.R.	Slew rate	$T_A = 25°C$	0.6	1		0.6	1		V/μs
GBW	Small-signal unity gain bandwidth	$T_A = 25°C$		3			3		MHz
θ_M	Phase margin	$T_A = 25°C$		45			45		Degr
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$, $T_A = 25°C$ T_A = F.R.	±13 ±12.5	±13.5 ±13		±13 ±12.5	±13.5 ±13		V
V_{OUT}	Output voltage swing	$R_L = 600\Omega$*, $T_A = 25°C$ T_A = F.R.	±10 ±8	±11.5 ±9		±10 ±8	±11.5 ±9		V
I_{CC}	Power supply current	R_L = Open, $T_A = 25°C$ T_A = F.R.		6 7	10 12		6 7	10 12	mA
PSRR	Power supply rejection ratio	$T_A = 25°C$, T_A = F.R.	80 80	110 100		80 80	110 100		dB
AA	Amplifier to amplifier coupling	f = 1kHz to 20kHz, $T_A = 25°C$		−120			−120		dB
HD	Total harmonic distortion	f = 10kHz, $T_A = 25°C$ V_O = 7VRMS		0.01			0.01		%
V_{INN}	Input-noise voltage	f = 1kHz, $T_A = 25°C$		30			30		$nV/\sqrt{Hz}$

NOTE

*For operation at elevated temperature, N package must be derated based on a thermal resistance of 95°C/W junction to ambient.

FOUR QUADRANT PHOTO-CONDUCTIVE DETECTOR AMPLIFIER

When operating a photo diode in the photo-conductive mode (reverse biased) very small currents in the micro ampere range must be sensed in the photo active operating region. Dark currents in the nano amperes are common. Generally, for this reason, J-FET input preamps are used to prevent interaction and accuracy degradation due to input bias currents.

The 5514 has sufficiently low input bias current (6na) to allow its use under these circuit constraints as shown in a possible design used to sense four quadrant motion of a light source. By proper summing of the signals from the X and Y axes, four quadrant output may be fed to an X-Y plotter, oscilloscope or computer for simulation. (See figure 1).

The wide input common mode voltage range of the device allows a +10 volt supply to be used to drive the signal bridge giving high sensitivity and improved signal to noise. Obviously, input balancing is critical to achieving common mode signal rejection in addition to adequate shielding of the sensor leads. The sensor head itself must be shielded and the shield grounded to signal common to avoid unwanted noise pick up from power line and other local noise sources. Amplifier response may be shaped to aid in noise reduction by more complex filter configurations. If possible the 5514 should be located in close proximity to the sensor head.

System balance may be done under dark field conditions if adequate photo detector tracking results. However, for high accuracy systems a bipolar balance adjust added to the non-inverting output stage is more desirable. With this latter method the signal bridge is balanced for a null output under uniform light field conditions using the bridge balance pot as shown. D.C. offset is then adjusted using the balance pot on the output amplifier under dark field conditions.

FOUR QUADRANT PHOTO DETECTOR

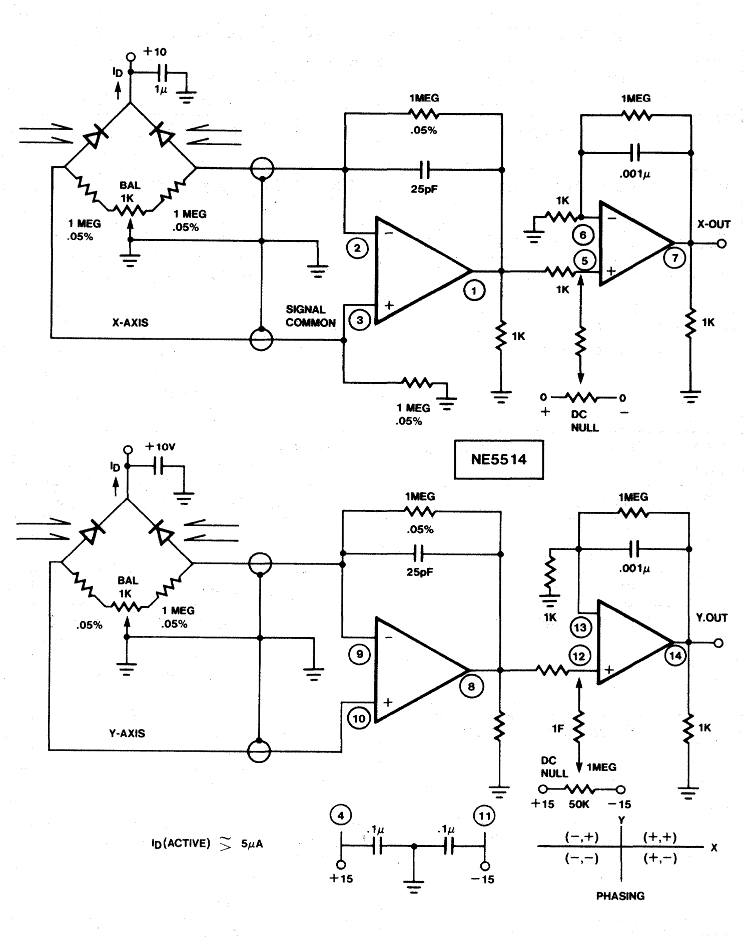


Figure 1

MULTI-TONE BANDPASS FILTER FOR PLL TONE DECODER

In the design of a multiple tone signaling system, particularly where signals are transmitted over long lines, noise and adjacent channel interference may be a significant barrier to reliable communications.

By the use of narrow band active pre-filters to attain selectivity and gain, the effective signal to noise ratio is greatly improved. The NE/SE5514 is easily adapted to such filter configurations due to its inherent stability. In addition its very high input impedance drastically reduces loading on the passive networks and allows for increased "Q" and large value resistors.

The circuit in Figure 2 demonstrates multiple feedback filters operating at four of the standard signaling frequencies. More channels may be added to increase the capacity of the system.

Test results obtained from this filter configuration were as follows:

Wide band signal to noise	63dB
Gain (Mid band)	30dB
Q (effective)	≈ 30
Output	OdBM $(.775v_{rms})$

Note that the amplifiers are operated from a single +12 volt supply and are biased to half V_{CC} by a simple resistive divider at point B which connects to all non-inverting inputs.

4-STATION 0–50° TEMPERATURE SENSOR

By using an NPN transistor as a temperature sensing element, the NE5514 forms the basis for a multi-station temperature sensor as shown in Figure 3. The principle used is fundamental to the current-voltage relationship of a forward biased junction. The current flow across the base-emitter junction is determined by absolute temperature in the following way:

$$I_E = -(I_C + I_B)$$

and $I_E \infty I_S \exp (V_{BE}/V_T)$; $V_T = \frac{kt}{q}$

therefore, $V_{BE} \infty V_T \ln I_E/I_S$

Where I_E is the forward current and I_S is the saturation current inherent in the junction, I_E must be high enough such that the I_S variation with temperature is small relative to I_E ($I_E >> I_S$). I_S is typically .05 pA, therefore, setting I_E to 1 or 2 μA gives the desired condition.

Diode D_1 serves to substantially reduce error due to power supply variation by giving a fixed voltage reference. To calibrate the sensor adjust R_4 for "O" volts output from the NE5514 at 0°C. Adjust R_6 tracking resistor for a scale factor of 100 millivolts per °C output.

Only the transistor need be placed in the temperature controlled environment. Figure 4 shows the addition of an A/D converter and display to give a digital thermometer.

NE/SE5514
MFB BANDPASS FILTER
FOR
MULTI-CHANNEL TONE DECODER

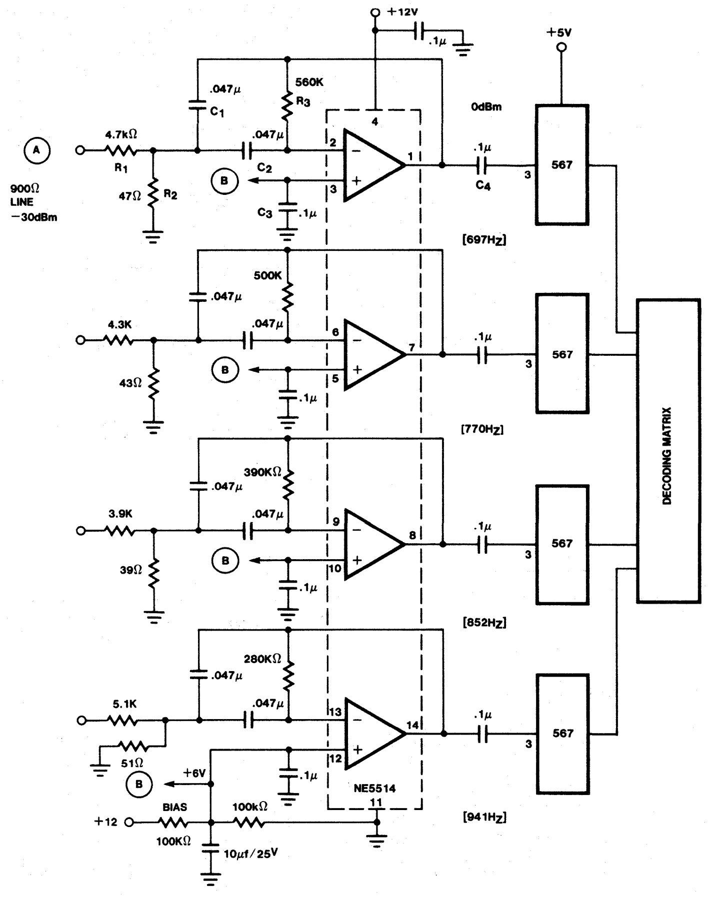


Figure 2

4-CHANNEL TEMPERATURE SENSOR
(0–50°C)

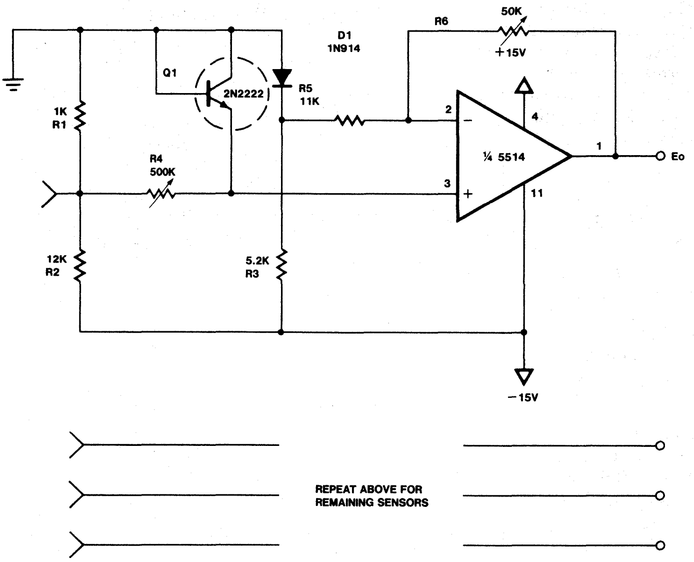


Figure 3

μP-CONTROLLED DIGITAL THERMOMETER

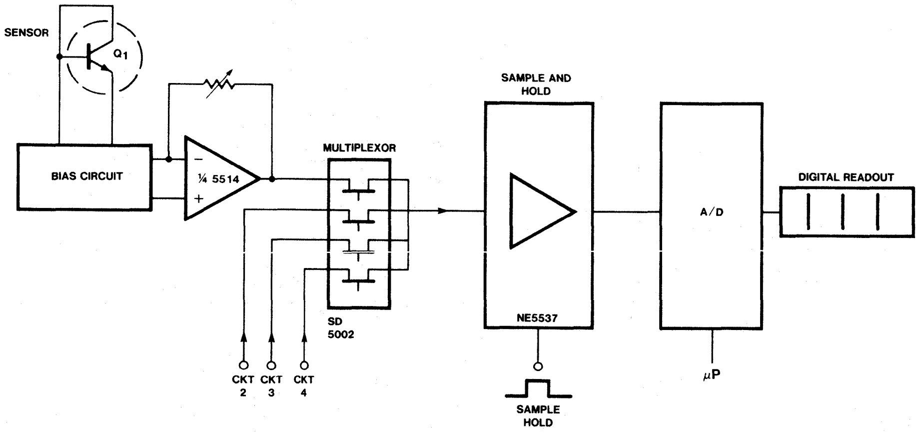


Figure 4

OPERATIONAL TRANSCONDUCTANCE AMPLIFIER NE5517/5517A

DESCRIPTION

The NE5517 contains two current controlled transconductance amplifiers, each with a differential input and push-pull output. The NE5517 offers significant design and performance advantages over similar devices for all types of programmable gain applications. Constant impedance buffers are provided which effectively eliminate changes in output offset voltage as the amplifier bias current is varied. Circuit performance is enhanced through the use of linearizing diodes at the inputs which enable a 10 dB signal to noise improvement referenced to .5 percent THD. The NE5517 is suited for a wide variety of industrial and consumer applications and is recommended as the preferred circuit in the Dolby* HX (Headroom Extension) system.

FEATURES

- **Constant impedance buffers**
- **ΔV_{BE} of buffer is constant with amplifier I_{BIAS} change**
- **Pin compatible with LM13600**
- **Excellent matching between amplifiers**
- **Linearizing diodes**
- **High output signal-to-noise ratio**

APPLICATIONS

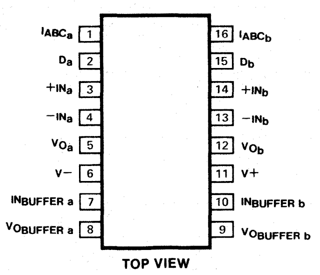
- **Multiplexers**
- **Timers**
- **Electronic music synthesizers**
- **Dolby* HX Systems**
- **Current-controlled amplifiers, filters**
- **Current-controlled oscillators, impedances**

NOTE

*Dolby is a registered trademark of Dolby Laboratories Inc., San Francisco, Calif.

PIN CONFIGURATION

D,N PACKAGE



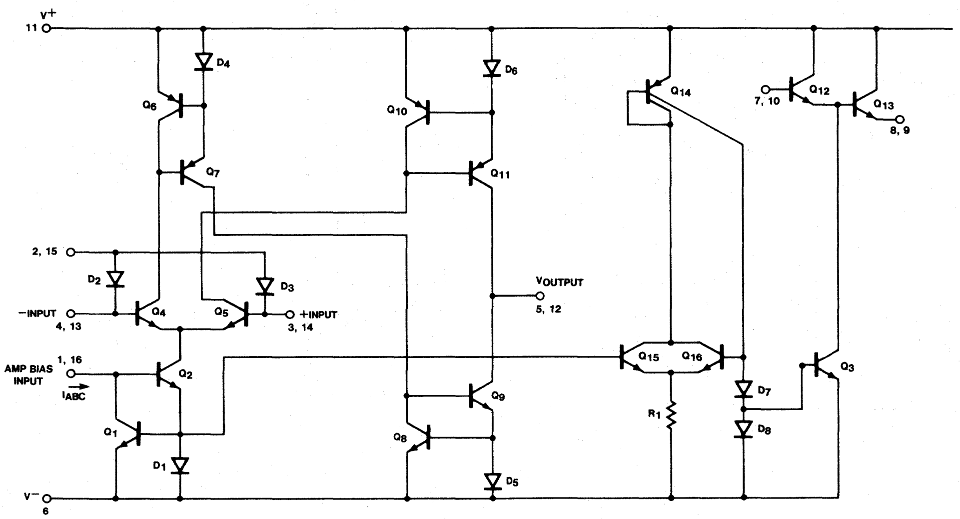
TOP VIEW

ORDER NUMBERS
NE5517N NE5517D NE5517AN

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply Voltage[1]		
NE5517	36 V_{DC} or ±18	V
NE5517A	44 V_{DC} or ±22	V
Power Dissipation[2] T_A = 25°C		
NE5517N, NE5517AN	570	mW
Differential Input Voltage	±5	V
Diode Bias Current (I_D)	2	mA
Amplifier Bias Current (I_{ABC})	2	mA
Output Short Circuit Duration	Indefinite	
Buffer Output Current[3]	20	mA
Operating Temperature Range		
NE5517N, NE5517AN	0°C to +70	°C
DC Input Voltage	$+V_S$ to $-V_S$	
Storage Temperature Range	−65°C to +150	°C
Lead Temperature (Soldering, 10 Seconds)	300	°C

CIRCUIT SCHEMATIC



ANALOG DIVISION MARCH 1982

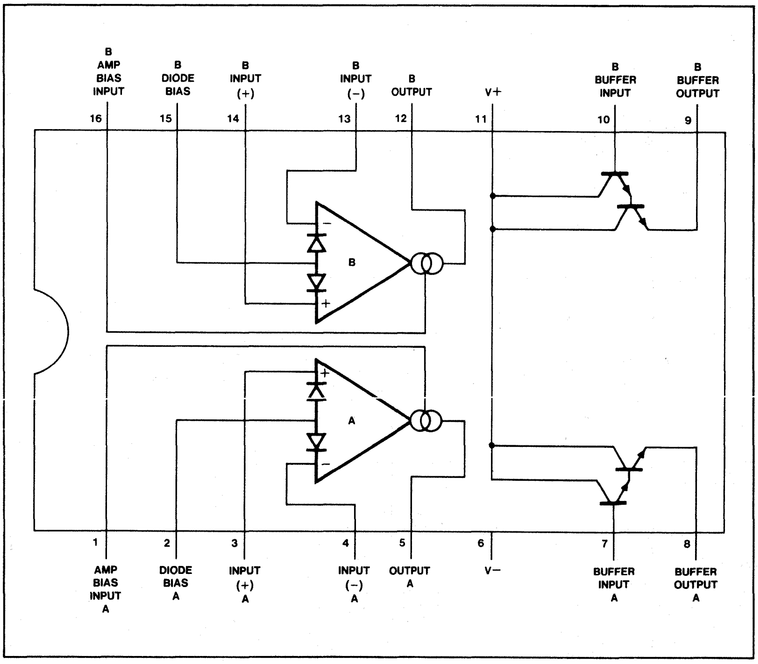
OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

NE5517/5517A

PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	I_{ABCa}	Amplifier bias input A
2	D_a	Diode bias A
3	$+IN_a$	Non-inverting input A
4	$-IN_a$	Inverting input A
5	V_{oa}	Output A
6	V−	negative supply
7	$IN_{Buffer (a)}$	Buffer input A
8	$Vo_{Buffer (a)}$	Buffer output A
9	$Vo_{Buffer (b)}$	Buffer output B
10	$IN_{Buffer (b)}$	Buffer input B
11	V+	Positive supply
12	V_{ob}	Output B
13	$-IN_b$	Inverting input B
14	$+IN_b$	Non-inverting input B
15	D_b	Diode bias B
16	I_{ABCb}	Amplifier bias input B

CONNECTION DIAGRAM



ELECTRICAL CHARACTERISTICS[4]

PARAMETER	TEST CONDITIONS	NE5517			NE5517A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage (V_{OS})			0.4	5		0.4	2	mV
	Over temperature range						5	mV
	I_{ABC} 5μA		0.3	5		0.3	2	mV
V_{OS} including diodes	Diode bias current (I_D) = 500μA		0.5	5		0.5	2	mV
Input offset change	5μA ≤ I_{ABC} ≤ 500μA		0.1			0.1	3	mV
Input offset current			0.1	0.6		0.1	0.6	μA
Input bias current			0.4	5		0.4	5	μA
	Over temperature range		1	8		1	7	μA
Forward Transconductance (gm)		6700	9600	13000	7700	9600	12000	μmho
	Over temperature range	5400			4000			μmho
gm tracking			0.3			0.3		dB
Peak output current	RL = 0, I_{ABC} = 5μA		5		3	5	7	μA
	RL = 0, I_{ABC} = 500μA	350	500	650	350	500	650	μA
	RL = 0,	300			300			μA
Peak output voltage								
Positive	RL = ∞, 5μA ≤ I_{ABC} ≤ 500μA	+12	+14.2		+12	+14.2		V
Negative	RL = ∞, 5μA ≤ I_{ABC} ≤ 500μA	−12	−14.4		−12	−14.4		V
Supply current	I_{ABC} = 500μA, both channels		2.6			2.6		mA
V_{OS} sensitivity								
Positive	$\Delta V_{OS}/\Delta V+$		20	150		20	150	μV/V
Negative	$\Delta V_{OS}/\Delta V-$		20	150		20	150	μV/V
CMRR		80	110		80	110		dB
Common mode range		±12	±13.5		±12	±13.5		V
Crosstalk	Referred to input[5] 20Hz < f < 20kHz		100			100		dB
Diff. input current	I_{ABC} = 0, input = ±4V		0.02	100		0.02	10	nA
Leakage current	I_{ABC} = 0 (Refer to test circuit)		0.2	100		0.2	5	nA
Input resistance		10	26		10	26		KΩ
Open loop bandwidth			2			2		MHz
Slew rate	Unity gain compensated		50			50		V/μSec
Buff. input current	5		0.4	5		0.4	5	μA
Peak buffer output voltage	5	10			10			V
ΔV_{BE} of buffer	6 Refer to Buffer V_{BE} test circuit		0.5	5		0.5	5	mV

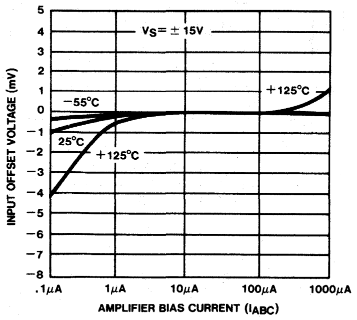
NOTES

1. For selections to a supply voltage above ±22V, contact factory.
2. For operating at high temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 175° C/W which applies for the device soldered in a printed circuit board, operating in still air.
3. Buffer output current should be limited so as to not exceed package dissipation.
4. These specifications apply for V_S = ±15V, T_A = 25°C, amplifier bias current (I_{ABC}) = 500μA, pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.
5. These specifications apply for V_S = ±15V, I_{ABC} = 500μA, R_{OUT} = 5kΩ connected from the buffer output to $-V_S$ and the input of the buffer is connected to the transconductance amplifier output.
6. V_S = ±15, R_{OUT} = 5Ω connected from Buffer output to $-V_S$ and 5μA ≤ I_{ABC} ≤ 500μA.

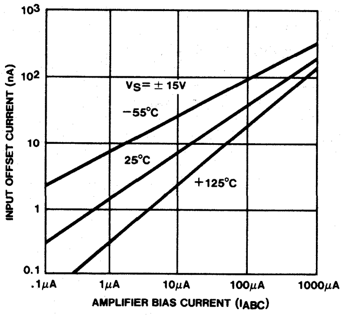
OPERATIONAL TRANSCONDUCTANCE AMPLIFIER NE5517/5517A

TYPICAL PERFORMANCE CHARACTERISTICS

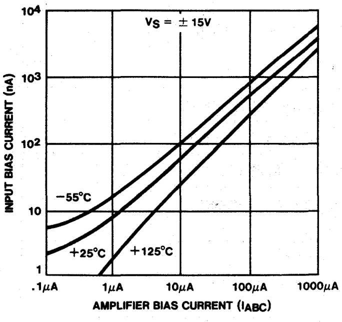
INPUT OFFSET VOLTAGE



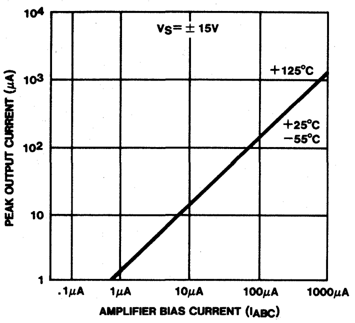
INPUT OFFSET CURRENT



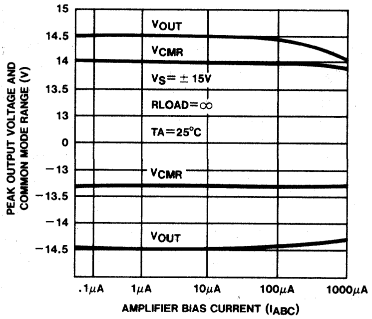
INPUT BIAS CURRENT



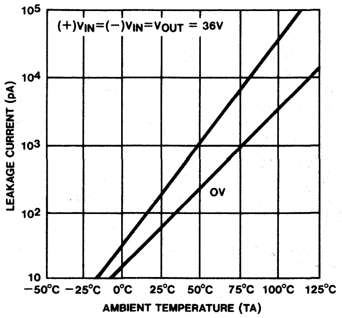
PEAK OUTPUT CURRENT



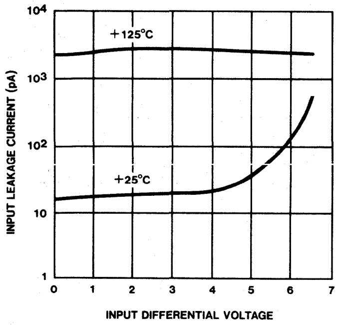
PEAK OUTPUT VOLTAGE AND COMMON MODE RANGE



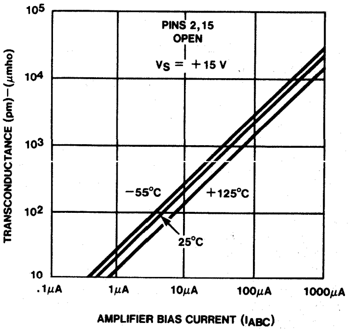
LEAKAGE CURRENT



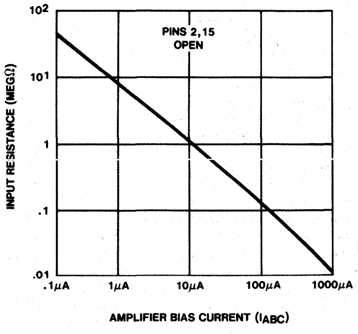
INPUT LEAKAGE



TRANSCONDUCTANCE

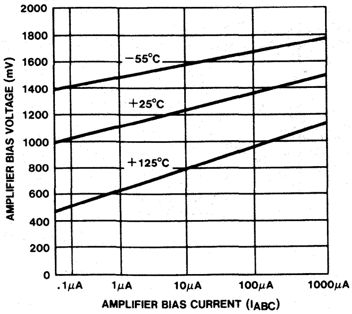


INPUT RESISTANCE

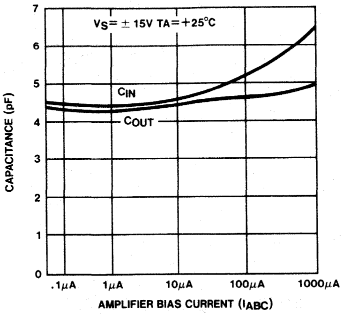


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

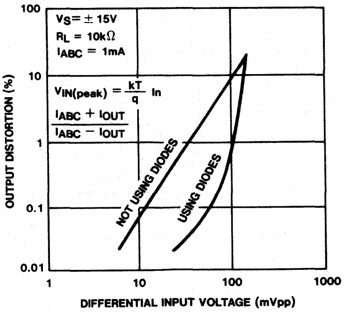
AMPLIFIER BIAS VOLTAGE vs AMPLIFIER BIAS CURRENT



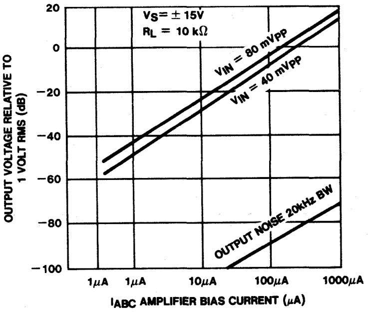
INPUT AND OUTPUT CAPACITANCE



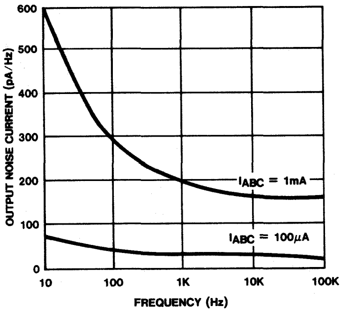
DISTORTION vs DIFFERENTIAL INPUT VOLTAGE



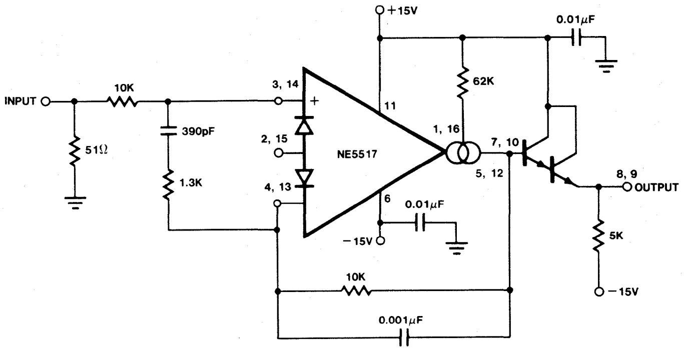
VOLTAGE vs AMPLIFIER BIAS CURRENT



OUTPUT NOISE vs FREQUENCY

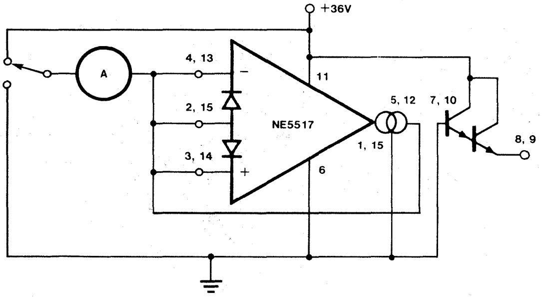


UNITY GAIN FOLLOWER

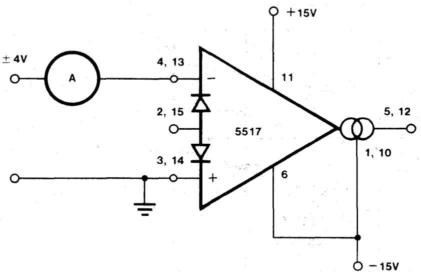


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

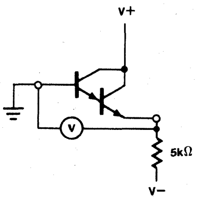
LEAKAGE CURRENT TEST CIRCUIT



DIFFERENTIAL INPUT CURRENT TEST CIRCUIT



BUFFER V_{BE} TEST CIRCUIT



INTERNALLY COMPENSATED DUAL LOW NOISE OP AMP NE/SE5532/5532A

DESCRIPTION

The 5532 is a dual high-performance low noise operational amplifier. Compared to most of the standard operational amplifiers, such as the 1458, it shows better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

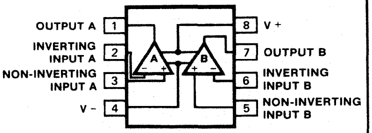
This makes the device especially suitable for application in high quality and professional audio equipment, instrumentation and control circuits, and telephone channel amplifiers. The op amp is internally compensated for gains equal to one. If very low noise is of prime importance, it is recommended that the 5532A version be used which has guaranteed noise specifications.

FEATURES

- **Small-signal bandwidth: 10MHz**
- **Output drive capability: 600Ω, 10V (rms)**
- **Input noise voltage: 5nV/√Hz**
- **DC voltage gain: 50000**
- **AC voltage gain: 2200 at 10kHz**
- **Power bandwidth: 140kHz**
- **Slew-rate: 9V/μs**
- **Large supply voltage range: ±3 to ±20V**

PIN CONFIGURATION

FE,N PACKAGE



TOP VIEW

ORDER NUMBERS

NE5532FE, N	SE5532FE
NE5532AFE, N	SE5532AFE

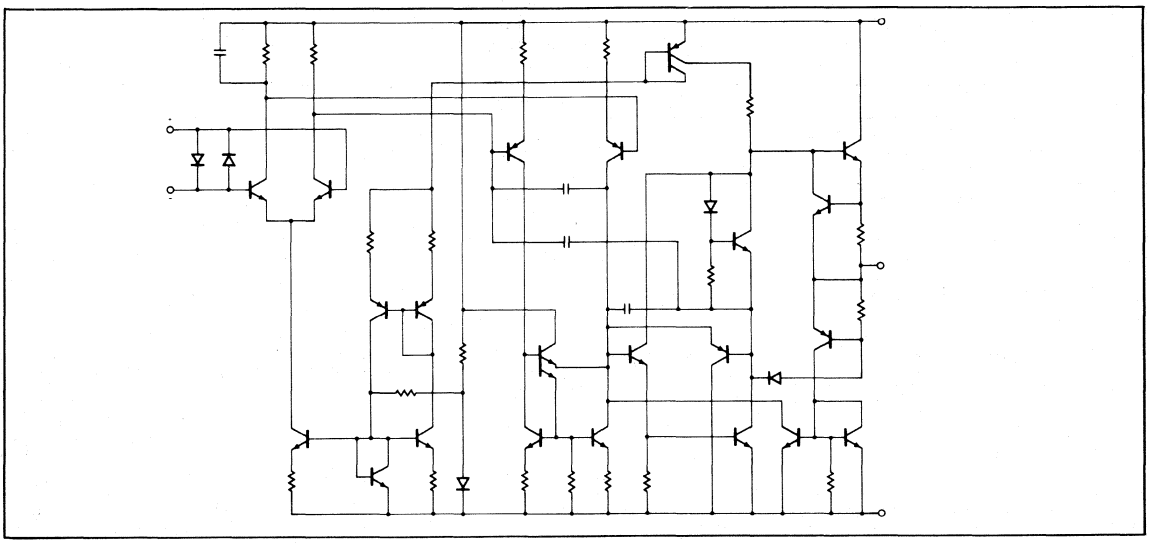
ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_S	Supply voltage	±22	V
V_{IN}	Input voltage	±V supply	V
V_{DIFF}	Differential input voltage[1]	±.5	V
T_A	Operating temperature range	0 to 70	°C
T_{STG}	Storage temperature	−65 to +150	°C
T_J	Junction temperature	150	°C
P_D	Power dissipation		
	5532FE	1000	mW
	Lead temperature (soldering, 10 sec)	300	°C

NOTES:

1. Diodes protect the inputs against over-voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ±10mA.
2. Thermal resistance of the FE package is 125°C/W.

EQUIVALENT SCHEMATIC (EACH AMPLIFIER)



INTERNALLY COMPENSATED DUAL LOW NOISE OP AMP NE/SE5532/5532A

DC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_S = ±15V unless otherwise specified.[1, 2]

PARAMETER		TEST CONDITIONS	SE5532/5532A			NE5532/5532A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage			.5	2		.5	4	mV
		Over temperature			3			5	mV
I_{OS}	Offset current				100		10	150	nA
		Over temperature			200			200	nA
I_B	Input current			200	400		200	800	nA
		Over temperature			700			1000	nA
I_{CC}	Supply current						8	16	mA
		Over temperature			13				mA
V_{CM}	Common mode input range		±12	±13		±12	±13		V
CMRR	Common mode rejection ratio		80	100		70	100		dB
PSRR	Power supply rejection ratio			10	50		10	100	μV/V
A_{VOL}	Large signal voltage gain	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	50			25	100		V/mV
		Over temperature	25			15			V/mV
		$R_L \geq 600\Omega$, $V_O = \pm 10V$	40			15	50		V/mV
		Over temperature	20			10			V/mV
V_{OUT}	Output swing	$R_L \geq 600\Omega$				±12	±13		V
		$R_L \geq 600\Omega$, $V_S = \pm 18V$				±15	±16		V
		$R_L \geq 2k\Omega$	±12	±13					V
R_{IN}	Input resistance		30	300		30	300		kΩ
I_{SC}	Output short circuit current			38			38		mA

NOTES

1. For NE5532, NE5532A, T_{Min} = 0°C, T_{Max} = 70°C.
2. For SE5532/5532A, T_{Min} = −55°C, T_{Max} = +125°C.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_S = ±15V unless otherwise specified.

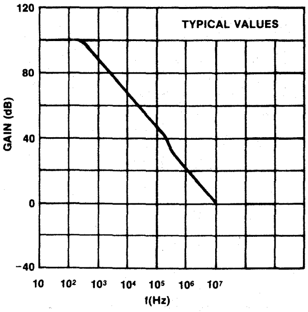
PARAMETER		TEST CONDITIONS	NE/SE5532/5532A			UNIT
			Min	Typ	Max	
R_{OUT}	Output resistance	A_V = 30dB Closed loop f = 10kHz, R_L = 600Ω		0.3		Ω
	Overshoot	Voltage follower V_{IN} = 100mV p-p C_L = 100pF R_L = 600Ω		10		%
	Gain	f = 10kHz		2.2		V/mV
	Gain bandwidth product	C_L = 100pF R_L = 600Ω		10		MHz
	Slew rate			9		V/μs
	Power bandwidth	$V_{OUT} = \pm 10V$		140		kHz
		$V_{OUT} = \pm 14V$, R_L = 600Ω, $V_{CC} = \pm 18V$		100		kHz

ELECTRICAL CHARACTERISTICS T_A = 25°C, V_S = ±15V unless otherwise specified.

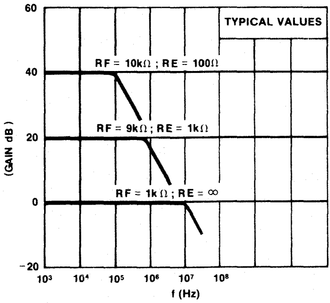
PARAMETER	TEST CONDITIONS	NE/SE5532			NE/SE5532A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input noise voltage	f_O = 30Hz		8			8	12	nV/√Hz
	f_O = 1kHz		5			5	6	nV/√Hz
Input noise current	f_O = 30Hz		2.7			2.7		pA/√Hz
	f_O = 1kHz		0.7			0.7		pA/√Hz
Channel separation	f = 1kHz, RS = 5kΩ		110			110		dB

TYPICAL PERFORMANCE CHARACTERISTICS

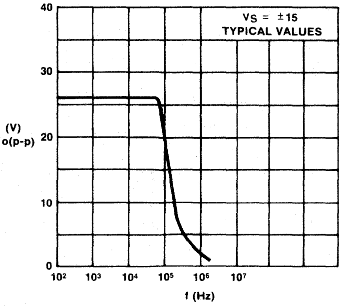
OPEN LOOP FREQUENCY RESPONSE



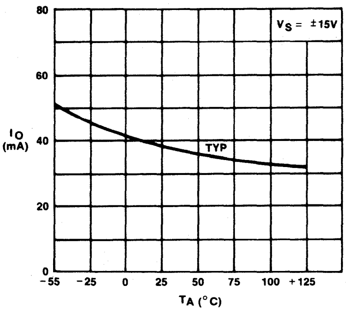
CLOSED LOOP FREQUENCY RESPONSE



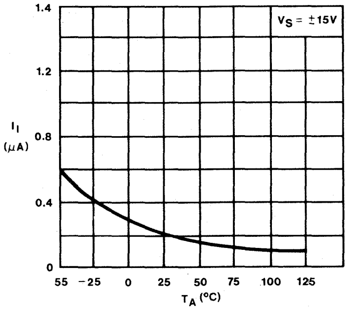
LARGE-SIGNAL FREQUENCY RESPONSE



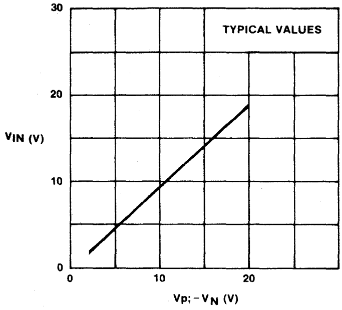
OUTPUT SHORT-CIRCUIT CURRENT



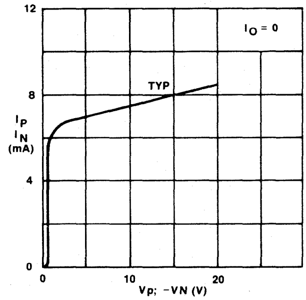
INPUT BIAS CURRENT



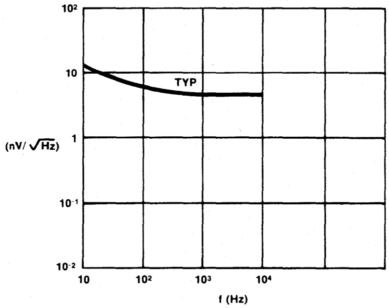
INPUT COMMON MODE VOLTAGE RANGE



SUPPLY CURRENT

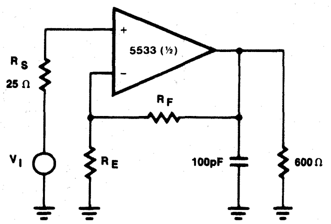


INPUT NOISE VOLTAGE DENSITY

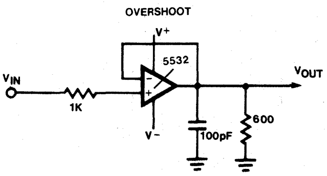


TEST CIRCUITS

CLOSED LOOP FREQUENCY RESPONSE



VOLTAGE FOLLOWER



INTERNALLY COMPENSATED DUAL LOW NOISE OP AMP NE/SE5532/5532A

APPLICATIONS

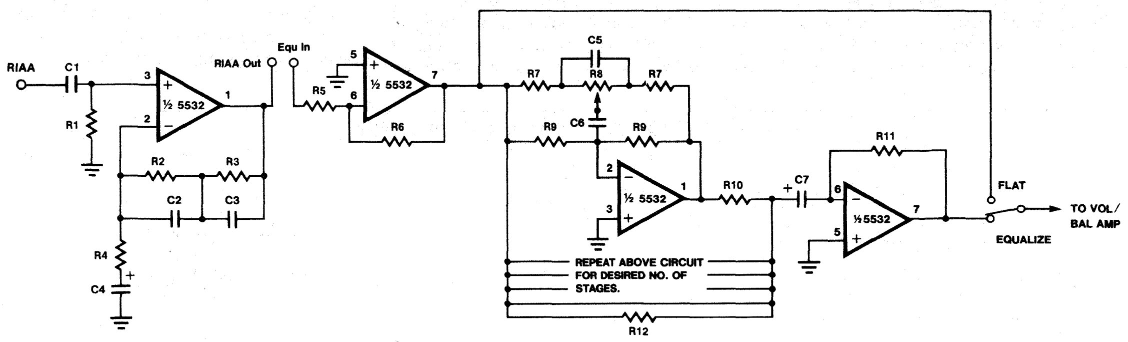
The Signetics 5532 High Performance Op Amp is an ideal amplifier for use in high quality and professional audio equipment which requires low noise and low distortion.

The circuit included in this application note has been assembled on a P.C. board, and tested with actual audio input devices (Tuner and Turntable). It consists of an RIAA pre-amp, input buffer, 5-band equalizer, and mixer. Although the circuit design is not new, its performance using the 5532 has been improved.

The RIAA pre-amp section is a standard compensation configuration with low frequency boost provided by the Magnetic cartridge and the RC network in the op amp feedback loop. Cartridge loading is accomplished via R1. 47k was chosen as a typical value, and may differ from cartridge to cartridge.

The Equalizer section consists of an input buffer, 5 active variable band pass/notch (depending on R9's setting) filters, and an

RIAA—EQUALIZER SCHEMATIC



COMPONENT VALUE TABLES

R8 = 25k R7 = 2.4k R9 = 240k			R8 = 50k R7 = 5.1k R9 = 510k			R8 = 100k R7 = 10k R9 = 1meg		
fo	C5	C6	fo	C5	C6	fo	C5	C6
23 Hz	1µF	.1µF	25 Hz	.47µF	.047µF	12 Hz	.47µF	.047µF
50 Hz	.47µF	.047µF	36 Hz	.33µF	.033µF	18 Hz	.33µF	.033µF
72 Hz	.33µF	.033µF	54 Hz	.22µF	.022µF	27 Hz	.22µF	.022µF
108 Hz	.22µF	.022µF	79 Hz	.15µF	.015µF	39 Hz	.15µF	.015µF
158 Hz	.15µF	.015µF	119 Hz	.1µF	.01µF	59 Hz	.1µF	.01µF
238 Hz	.1µF	.01µF	145 Hz	.082µF	.0082µF	72 Hz	.082µF	.0082µF
290 Hz	.082µF	.0082µF	175 Hz	.068µF	.0068µF	87 Hz	.068µF	.0068µF
350 Hz	.068µF	.0068µF	212 Hz	.056µF	.0056µF	106 Hz	.056µF	.0056µF
425 Hz	.056µF	.0056µF	253 Hz	.047µF	.0047µF	126 Hz	.047µF	.0047µF
506 Hz	.047µF	.0047µF	360 Hz	.033µF	.0033µF	180 Hz	.033µF	.0033µF
721 Hz	.033µF	.0033µF	541 Hz	.022µF	.0022µF	270 Hz	.022µF	.0022µF
1082 Hz	.022µF	.0022µF	794 Hz	.015µF	.0015µF	397 Hz	.015µF	.0015µF
1588 Hz	.015µF	.0015µF	1191 Hz	.01µF	.001µF	595 Hz	.01µF	.001µF
2382 Hz	.01µF	.001µF	1452 Hz	.0082µF	820pF	726 Hz	.0082µF	820pF
2904 Hz	.0082µF	820pF	1751 Hz	.0068µF	680pF	875 Hz	.0068µF	680pF
3502 Hz	.0068µF	680pF	2126 Hz	.0056µF	560pF	1063 Hz	.0056µF	560pF
4253 Hz	.0056µF	560pF	2534 Hz	.0047µF	470pF	1267 Hz	.0047µF	470pF
5068 Hz	.0047µF	470pF	3609 Hz	.0033µF	330pF	1804 Hz	.0033µF	330pF
7218 Hz	.0033µF	330pF	5413 Hz	.0022µF	220pF	2706 Hz	.0022µF	220pF
10827 Hz	.0022µF	220pF	7940 Hz	.0015µF	150pF	3970 Hz	.0015µF	150pF
15880 Hz	.0015µF	150pF	11910 Hz	.001µF	100pF	5955 Hz	.001µF	100pF
23820 Hz	.001µF	100pF	14524 Hz	820pF	82pF	7262 Hz	820pF	82pF
			17514 Hz	680pF	68pF	8757 Hz	680pF	68pF
			21267 Hz	560pF	56pF	10633 Hz	560pF	56pF
						12670 Hz	470pF	47pF
						18045 Hz	330pF	33pF

COMPONENT VALUES

R1	1meg	C1	.22µF
R2	100k	C2	750pF
R3	1meg	C3	.0033µF
R4	1.1k	C4	33µF
R5	100k	C5	SEE TABLE
R6	100k	C6	SEE TABLE
R7	SEE TABLE	C7	2.2µF
R8	(pot) SEE TABLE		
R9	SEE TABLE		
R10	100k		
R11	100k		
R12	20k (5 STAGES)		

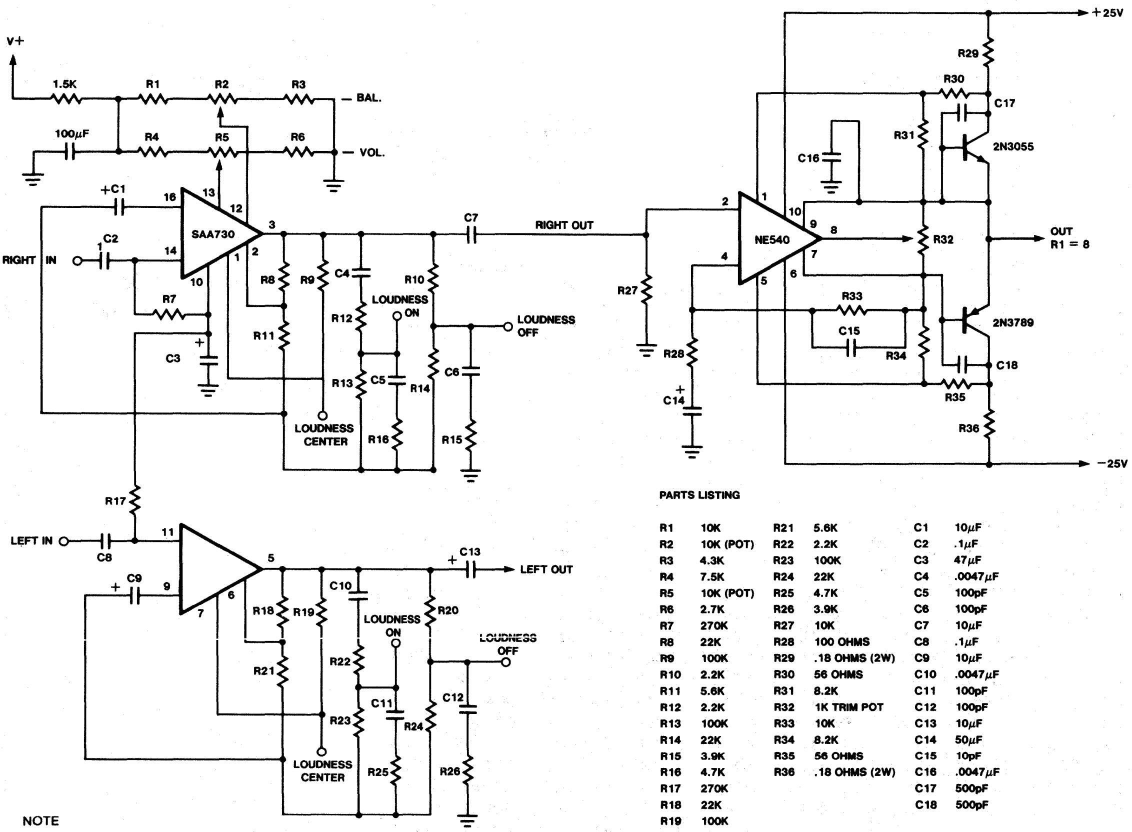
Figure 1

output summing amplifier. The input buffer is a standard unity gain design providing impedance matching between the pre amplifiers and the equalizer section. Because the 5532 is internally compensated, no external compensation is required. The 5-band active filter section is actually 5 individual active filters with the same feedback design for all 5. The main differance in all five stages is the values of C5 and C6 which are responsible for setting the center frequency of each stage. Linear pots are recommended for R9. To simplify use of this circuit, a component value table is provided, which lists center frequencies and their associated capacitor values. Notice that C5 equals (10) C6, and that the Value of R8 and R10 are related to R9 by a factor of 10 as well. The values listed in the table are common and easily found standard values.

The final stage is the summing amplifier/buffer stage, to sum the individual filters (Figure 2). Note the original signal is subtracted from the sum by a factor dependant on the number of filter stages. This subtraction is necessary to maintain a unity gain configuration at the output with all pots set to the flat position. If R13 were omitted the output with 1 volt at each stage would equal 5 volts (in this case) instead of the desired 1 volt. Full boost and cut using the table values is about ± 15dB. Although 5 bands were chosen for this application, the user may have as many bands as are required. Please note that the subtracting resistor R13, must be adjusted to meet the unity requirement using $R13 = \frac{100K}{\#\text{ of stages}}$ i.e. 5 stages = 20k.

The remainder of the circuit employs the Philips TCA 730H volume, balance, and loudness-control circuit and the Signetics NE540 power driver circuit, which as shown will net about 35 watts per channel RMS. The NE540 can be found in the Signetics Analog Data Manual, and Applications Manual. Information on the TCA730A may be obtained from Signetics Analog Division.

VOLUME, BALANCE, LOUDNESS & POWER AMPS



PARTS LISTING

R1	10K	R21	5.6K	C1	10µF
R2	10K (POT)	R22	2.2K	C2	.1µF
R3	4.3K	R23	100K	C3	47µF
R4	7.5K	R24	22K	C4	.0047µF
R5	10K (POT)	R25	4.7K	C5	100pF
R6	2.7K	R26	3.9K	C6	100pF
R7	270K	R27	10K	C7	10µF
R8	22K	R28	100 OHMS	C8	.1µF
R9	100K	R29	.18 OHMS (2W)	C9	10µF
R10	2.2K	R30	56 OHMS	C10	.0047µF
R11	5.6K	R31	8.2K	C11	100pF
R12	2.2K	R32	1K TRIM POT	C12	100pF
R13	100K	R33	10K	C13	10µF
R14	22K	R34	8.2K	C14	50µF
R15	3.9K	R35	56 OHMS	C15	10pF
R16	4.7K	R36	.18 OHMS (2W)	C16	.0047µF
R17	270K			C17	500pF
R18	22K			C18	500pF
R19	100K				
R20	2.2K				

NOTE
All resistors ¼W 1% to 5% unless otherwise noted

For additional information on the NE540, refer to Signetics Analog Data and Applications Manuals.

For additional information on the SAA730, contact Signetics Analog Division, Philips Representative.

Figure 2

SINGLE AND DUAL LOW NOISE OP AMP NE5533/5533A / NE/SE5534/5534A

DESCRIPTION

The 5533/5534 are dual and single high-performance low noise operational amplifiers. Compared to other operational amplifiers, such as TL083, they show better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

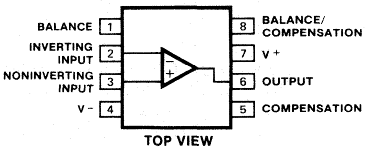
This makes the devices especially suitable for application in high quality and professional audio equipment, in instrumentation and control circuits and telephone channel amplifiers. The op amps are internally compensated for gain equal to, or higher than, three. The frequency response can be optimized with an external compensation capacitor for various applications (unity gain amplifier, capacitive load, slew-rate, low overshoot, etc.) If very low noise is of prime importance, it is recommended that the 5533A/5534A version be used which has guaranteed noise specifications.

FEATURES

- **Small-signal bandwidth: 10MHz**
- **Output drive capability: 600Ω, 10V (rms) at $V_S = \pm 18V$**
- **Input noise voltage: 4nV/$\sqrt{Hz}$**
- **DC voltage gain: 100000**
- **AC voltage gain: 6000 at 10kHz**
- **Power bandwidth: 200kHz**
- **Slew-rate: 13V/μs**
- **Large supply voltage range: ±3 to ±20V**

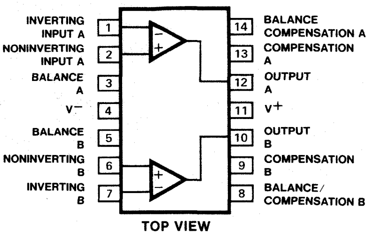
PIN CONFIGURATIONS

D,FE,N PACKAGE



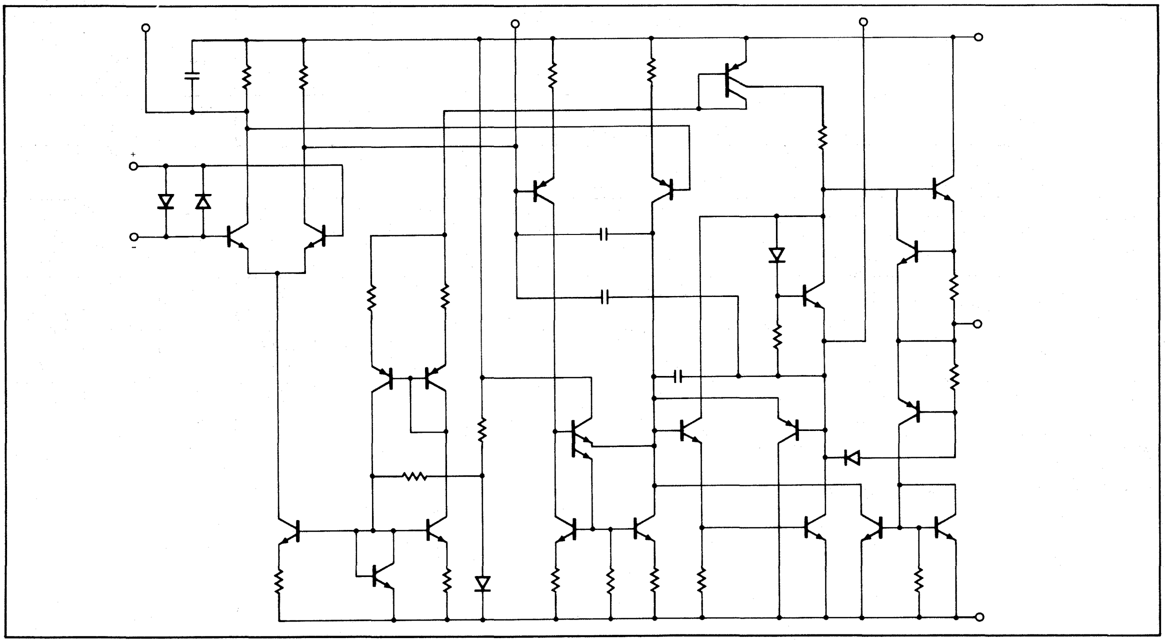
ORDER NUMBERS
NE/SE5534N, FE NE/SE5534AN, AFE
NE5534D

F,N PACKAGE



ORDER NUMBERS
NE5533N, F
NE5533AN, AF

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_S	Supply voltage	±22	V
V_{IN}	Input voltage	±V supply	V
V_{DIFF}	Differential input voltage[1]	±.5	V
T_A	Operating temperature range		
	SE5534/5534A	-55 to +125	°C
	NE5533/5533A/5534/5534A	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C
T_J	Junction temperature	150	°C
P_D	Power dissipation at 25°C[2]		
	5533N, 5534N, 5534FE	800	mW
	5533F	1000	mW
	Output short circuit duration[3]	indefinite	
	Lead temperature (soldering 10 sec)	300	°C

NOTES

1. Diodes protect the inputs against over-voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ±10mA.
2. For operation at elevated temperature, derate packages based on the following junction-to-ambient thermal resistances:

8-pin ceramic (FE)	140°C/W
14-pin ceramic (F)	110°C/W
8-pin plastic (N)	162°C/W
14-pin plastic (N)	150°C/W

3. Output may be shorted to ground at V_S = ±15V, T_A = 25°C. Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.

DC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_S = ±15V unless otherwise specified.[1,2]

PARAMETER		TEST CONDITIONS	SE5534/5534A			NE5533/5533A 5534/5534A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage			.5	2		.5	4	mV
		Over temperature			3			5	mV
I_{OS}	Offset current			10	200		20	300	nA
		Over temperature			500			400	nA
I_B	Input current			400	800		500	1500	nA
		Over temperature			1500			2000	nA
I_{CC}	Supply current			4	6.5		4	8	mA
	Per op amp	Over temperature			9				mA
V_{CM}	Common mode input range		±12	±13		±12	±13		V
CMRR	Common mode rejection ratio		80	100		70	100		dB
PSRR	Power supply rejection ratio			10	50		10	100	μV/V
A_{VOL}	Large signal voltage gain	$R_L \geq 600\Omega$, $V_O = \pm 10V$	50	100		25	100		V/mV
		Over temperature	25			15			V/mV
V_{OUT}	Output swing	$R_L \geq 600\Omega$	±12	±13		±12	±13		V
		$R_L \geq 600\Omega$ $V_S = \pm 18V$	±15	±16		±15	±16		V
R_{IN}	Input resistance		50	100		30	100		kΩ
I_{SC}	Output short circuit current			38			38		mA

NOTES

1. For NE5533/5533A/5534/5534A, T_{MIN} = 0°C, T_{MAX} = 70°C
2. For SE5534/5534A, T_{MIN} = −55°C, T_{MAX} = +125°C

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm15V$ unless otherwise specified.

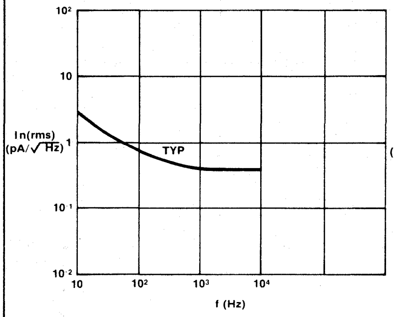
PARAMETER		TEST CONDITIONS	SE5534/5534A			NE5533/5533A 5534/5534A			UNIT
			Min	Typ	Max	Min	Typ	Max	
R_{OUT}	Output resistance	A_V = 30dB closed loop f = 10kHz, R_L = 600Ω, C_C = 22pF		0.3			0.3		Ω
Transient response		Voltage follower, V_{IN} = 50mV R_L = 600Ω, C_C = 22pF, C_L = 100pF							
T_R	Rise time			20			20		ns
	Overshoot			20			20		%
Transient response		V_{IN} = 50mv, R_L = 600Ω C_C = 47pF, C_L = 500pF							
T_R	Rise time			50			50		ns
	Overshoot			35			35		%
AC	Gain	f = 10kHz, C_C = 0		6			6		V/mV
		f = 10kHz, C_C = 22pF		2.2			2.2		V/mV
	Gain bandwidth product	C_C = 22pF, C_L = 100pF		10			10		mHz
	Slew rate	C_C = 0		13			13		V/μS
		C_C = 22pF		6			6		V/μS
	Power bandwidth	$V_{OUT} = \pm10V$, C_C = 0		200			200		kHz
		$V_{OUT} = \pm10V$, C_C = 22pF		95			95		kHz
		$V_{OUT} = \pm14V$, R_L = 600Ω C_C = 22pF, $V_{CC} = \pm18V$		70			70		kHz

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm15V$ unless otherwise specified.

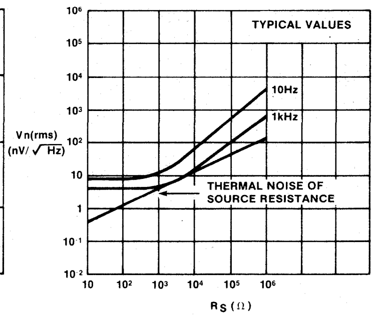
PARAMETER	TEST CONDITIONS	5533/5534			5533A/5534A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input noise voltage	f_O = 30Hz		7			5.5	7	$nV/\sqrt{Hz}$
	f_O = 1kHz		4			3.5	4.5	$nV/\sqrt{Hz}$
Input noise current	f_O = 30Hz		2.5			1.5		$pA/\sqrt{Hz}$
	f_O = 1kHz		0.6			0.4		$pA/\sqrt{Hz}$
Broadband noise figure	f = 10Hz – 20kHz, R_S = 5kΩ					0.9		dB
Channel separation	f = 1kHz, R_S = 5kΩ		110			110		dB

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

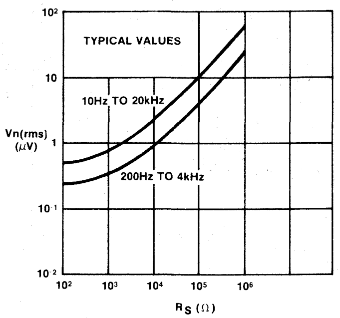
INPUT NOISE CURRENT DENSITY



TOTAL INPUT NOISE DENSITY

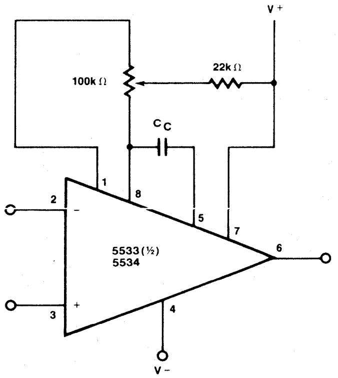


BROADBAND INPUT NOISE VOLTAGE

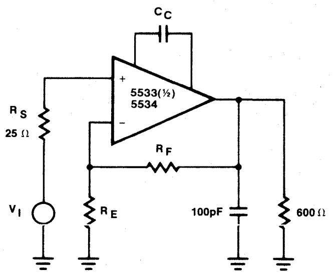


TEST LOAD CIRCUITS

FREQUENCY COMPENSATION AND OFFSET VOLTAGE ADJUSTMENT CIRCUIT

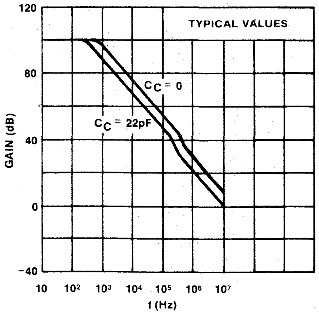


CLOSED LOOP FREQUENCY RESPONSE

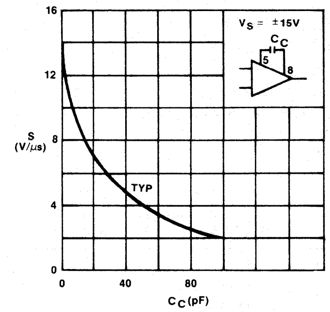


TYPICAL PERFORMANCE CHARACTERISTICS

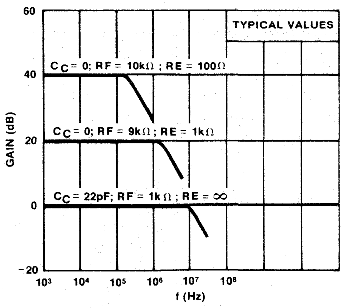
OPEN LOOP FREQUENCY RESPONSE



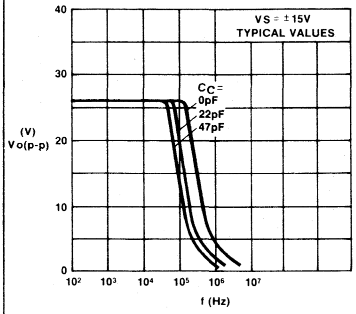
SLEW-RATE AS A FUNCTION OF COMPENSATION CAPACITANCE



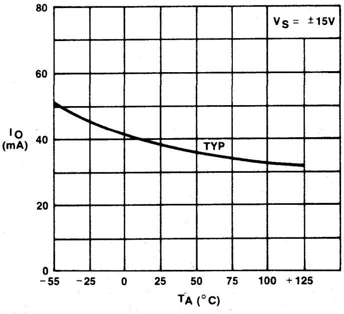
CLOSED LOOP FREQUENCY RESPONSE



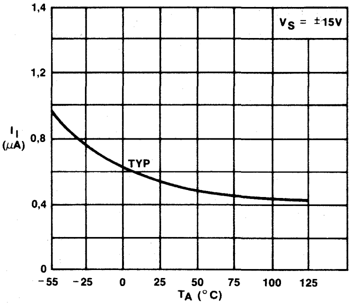
LARGE-SIGNAL FREQUENCY RESPONSE



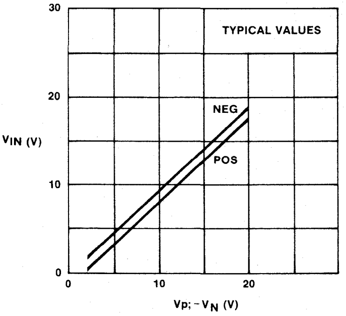
OUTPUT SHORT-CIRCUIT CURRENT



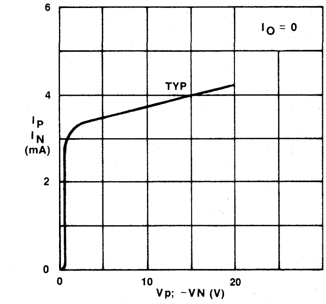
INPUT BIAS CURRENT



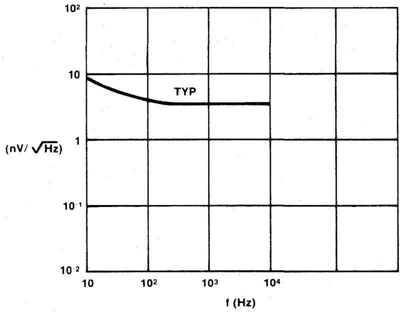
INPUT COMMON MODE VOLTAGE RANGE



SUPPLY CURRENT PER OP AMP



INPUT NOISE VOLTAGE DENSITY



ULTRA HIGH FREQUENCY OPERATIONAL AMPLIFIER NE/SE5539

DESCRIPTION

The Signetics NE5539 is a very wide bandwidth, high slew rate, monolithic operational amplifier for use in video amplifiers, RF amplifiers, and extremely high slew rate amplifiers.

Emitter follower inputs provide a true differential high input impedance device. Proper external compensation will allow design operation over a wide range of closed loop gains, both inverting and non-inverting, to meet specific design requirements.

FEATURES

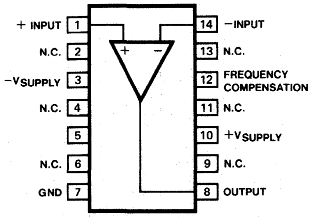
- **Gain bandwidth product: 1.2GHz**
- **Slew rate: 600V/μsec**
- **Full power response: 48MHz**
- **A_{VOL}: 50dB**

APPLICATIONS

- **Fast pulse amplifiers**
- **RF oscillators**
- **Fast sample and hold**
- **High gain video amplifiers (BW > 20MHz)**

PIN CONFIGURATION

D,F,N PACKAGE



TOP VIEW

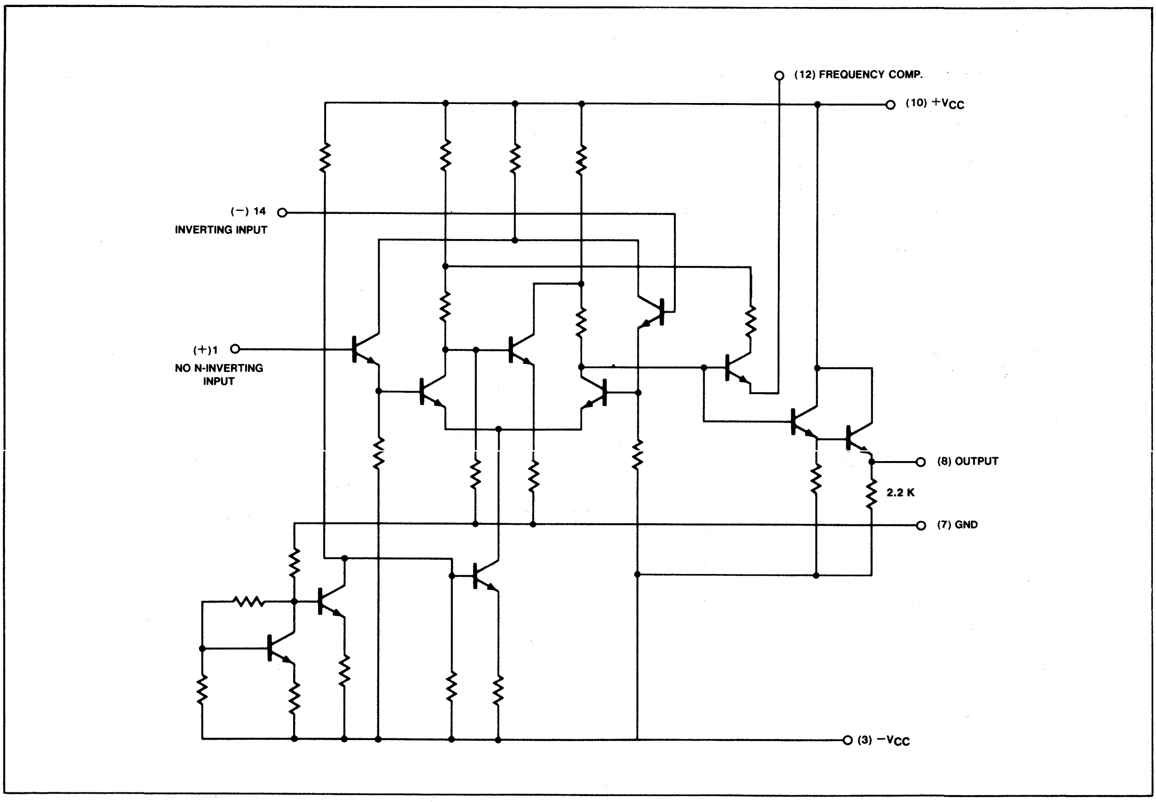
ORDER NUMBERS

NE/SE5539F NE/SE5539N
NE5539D

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	±12	V
P_D	Internal power dissipation	550	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_J	Max junction temperature	150	°C
T_A	Operating temperature range		
	NE	0 to 70	°C
	SE	−55 to +125	°C
	Lead temperature	300	°C

EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V$, $T_A = 25°C$ unless otherwise specified

PARAMETER	TEST CONDITIONS			SE5539			NE5539			UNIT
				Min	Typ	Max	Min	Typ	Max	
V_{OS} Input offset voltage	$V_O = 0V$, $R_S = 100\Omega$		Over temp		2	5				mV
			$T_A = 25°C$		2	3		2.5	5	
I_{OS} Input offset current			Over temp		.1	3				μA
			$T_A = 25°C$		.1	1			2	
I_B Input bias current			Over temp		6	25				μA
			$T_A = 25°C$		5	13		5	20	
CMRR Common mode rejection ratio	$F = 1$ kHz, $R_S = 100\Omega$, $V_{CM} = 1.7V$			70	80		70	85		dB
R_{IN} Input impedance					100			100		kΩ
R_{OUT} Output impedance					10			10		Ω
V_{OUT} Output voltage swing	$R_L = 150\Omega$ to GND and 470Ω to $-V_{CC}$		+Swing				+2.3	+2.7		V
			−Swing				−1.7	−2.2		
V_{OUT} Output voltage swing	$R_L = 2k\Omega$ to GND	Over temp	+Swing	+2.3	+3.0					V
			−Swing	−1.5	−2.1					
		$T_A = 25°C$	+Swing	+2.5	+3.1					V
			−Swing	−2.0	−2.7					
$I_{CC}+$ Positive supply current	$V_O = 0$, $R_1 = \infty$		Over temp		14	18				mA
			$T_A = 25°C$		14	17		14	18	
$I_{CC}-$ Negative supply current	$V_O = 0$, $R_1 = \infty$		Over temp		11	15				mA
			$T_A = 25°C$		11	14		11	15	
PSRR Power supply rejection ratio	$\Delta V_{CC} = \pm 1V$		Over temp		300	1000				$\mu V/V$
			$T_A = 25°C$					200	1000	
A_{VOL} Large signal voltage gain	$V_O = +2.3V, -1.7V$ $R_L = 150\Omega$ to GND, 470Ω to $-V_{CC}$						47	52	57	dB
A_{VOL} Large signal voltage gain	$V_O = +2.3V, -1.7V$ $R_L = 2K$ to GND		Over temp							dB
			$T_A = 25°C$				47	52	57	
A_{VOL} Large signal voltage gain	$V_O = +2.5V, -2.0V$ $R_L = 2\Omega$ to GND		Over temp	46		60				dB
			$T_A = 25°C$	48	53	58				

NOTE

1. Differential input voltage should not exceed 0.25 volts to prevent excessive input bias current and common mode voltage 2.5 volts. These voltage limits may be exceeded if current limit is 10mA.

AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V$, $R_L = 150\Omega$ to GND & 390Ω to $-V_{CC}$ unless otherwise specified

PARAMETER	TEST CONDITIONS	SE5539			NE5539			UNIT
		Min	Typ	Max	Min	Typ	Max	
Gain bandwidth product	$A_{CL} = 7$ $V_O = 0.1$ Vp-p		1200					MHz
Small signal bandwidth	$A_{CL} = 2$ $R_L = 150\Omega$		110					MHz
Settling time	$A_{CL} = 2$ $R_L = 150\Omega$		15					nSec
Slew rate	$A_{CL} = 2$ $R_L = 150\Omega$		600			330		V/μSec
Propagation delay	$A_{CL} = 2$ $R_L = 150\Omega$		7			10		nSec
Full power response	$A_{CL} = 2$ $R_L = 150\Omega$		48			20		MHz
Full power response	$A_V = 7$, $R_L = 150\Omega$		20					MHz
Wide band noise (RMS)	$B_W = 5MHz$, $R_S = 50\Omega$		5					μV

ULTRA HIGH FREQUENCY OPERATIONAL AMPLIFIER NE/SE5539

DC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 6V$, $T_A = 25°C$ unless otherwise specified

PARAMETERS		TEST CONDITIONS			SE5539			UNIT
					Min	Typ	Max	
V_{OS}	Input offset voltage			Over temp		2	5	mV
				$T_A = 25°C$		2	3	
I_{OS}	Input offset current			Over temp		.1	3	μA
				$T_A = 25°C$		.1	1	
I_B	Input bias current			Over temp		5	20	μA
				$T_A = 25°C$		4	10	
CMRR	Common mode rejection ratio	$V_{CM} = \pm 1.3V$, $R_S = 100\Omega$			70	85		dB
$I_{CC}+$	Positive supply current			Over temp		11	14	mA
				$T_A = 25°C$		11	13	
$I_{CC}-$	Negative supply current			Over temp		8	11	mA
				$T_A = 25°C$		8	10	
PSRR	Power supply rejection ratio	$\Delta V_{CC} = \pm 1V$		Over temp		300	1000	μV/V
				$T_A = 25°C$				
V_{OUT}	Output voltage swing	$R_L = 150\Omega$ to GND and 390Ω to $-V_{CC}$	Over temp	+ Swing	+ 1.4	+ 2.0		V
				− Swing	− 1.1	− 1.7		
			$T_A = 25°C$	+ Swing	+ 1.5	+ 2.0		
				− Swing	− 1.4	− 1.8		

AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V$, $R_l = 150\Omega$ to GND and 390Ω to $-V_{CC}$ unless otherwise specified

PARAMETER	TEST CONDITIONS	SE5539			UNIT
		Min	Typ	Max	
Gain bandwidth product	$A_{CL} = 7$		700		MHz
Small signal bandwidth	$A_{CL} = 2$		120		MHz
Settling time	$A_{CL} = 2$		23		ns
Slew rate	$A_{CL} = 2$		330		V/μs
Propagation delay	$A_{CL} = 2$		4.5		ns
Full power response	$A_{CL} = 2$		20		MHz

NE5539 COLOR VIDEO AMPLIFIER

The NE5539 wide band operational amplifier is easily adapted for use as a color video amplifier. A typical circuit is shown (figure 1) along with the Vectorscope photograph showing the amplifier response to a standard NTSC color signal. (Note that the input reference vectors are displayed simultaneously with the output.) The polar representation indicates amplifier differential phase error overall to be less than 2°. Gain also remains linear or constant with the varying input amplitudes.

The amplifier circuit was optimized for a 75Ω input and output termination impedance with a gain of 10 (20dB).

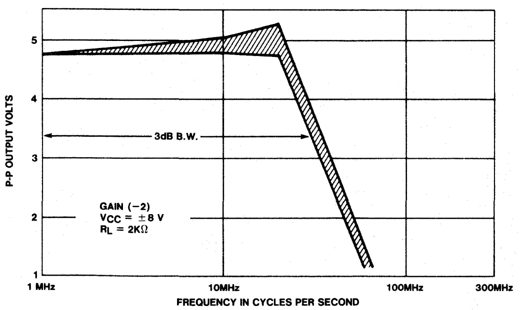
A second series of test waveforms show the amplifier's response to a 3.58MHz burst signal (figures 2 and 3).

Finally, the amplifier response is shown as a function of time for the NTSC signal with no perceptible droop or overshoot in response to step functions (see figure 4). Note that no external compensation was required since the gain was greater than 7 (17dB).

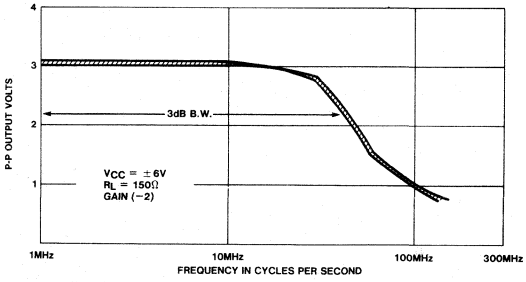
V_{CC} is ±8 volts for all cases shown.

ULTRA HIGH FREQUENCY OPERATIONAL AMPLIFIER NE/SE5539

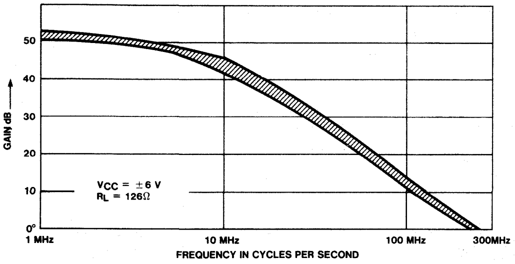
POWER BANDWIDTH (SE)



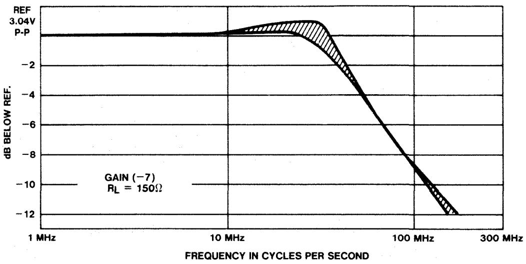
POWER BANDWIDTH (NE)



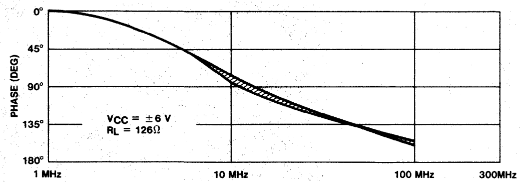
SE5539 OPEN LOOP GAIN vs FREQUENCY



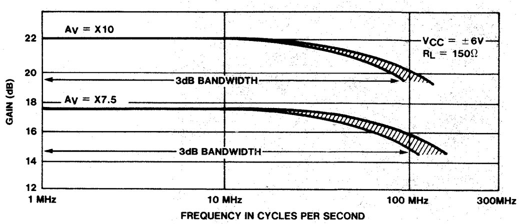
POWER BANDWIDTH



SE5539 OPEN LOOP PHASE vs FREQUENCY



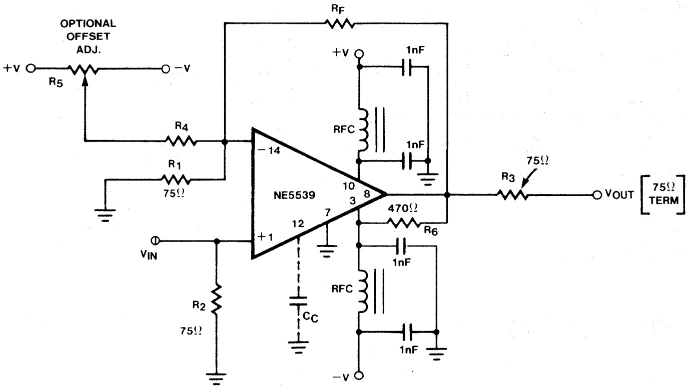
GAIN BANDWIDTH PRODUCT vs FREQUENCY



NOTE

▨ Indicates typical distribution $-55°C \leq T_A \leq 125°C$

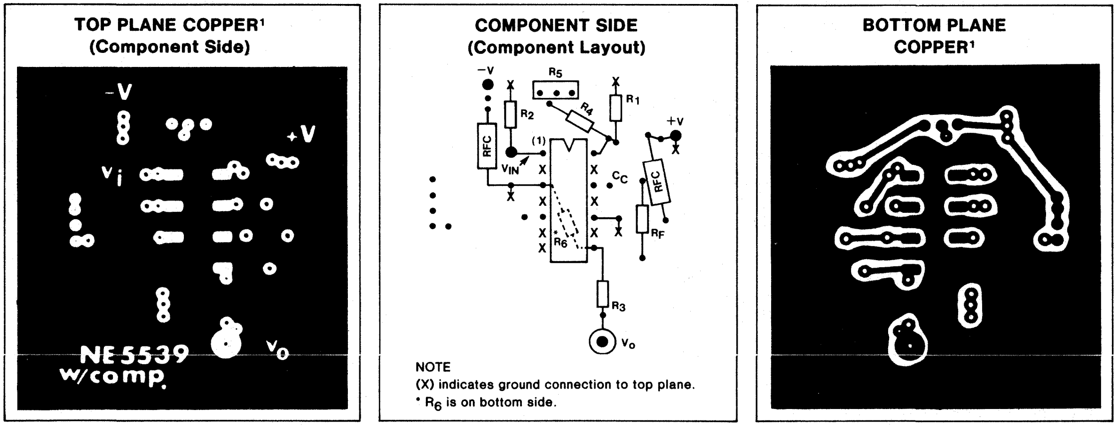
28dB NON-INVERTING AMP
SAMPLE P.C. LAYOUT



R_1 = 75Ω 5% CARBON
R_2 = 75Ω 5% CARBON
R_3 = 75Ω 5% CARBON
R_4 = 36K 5% CARBON

R_5 = 20K TRIMPOT (CERMET)
R_F = 1.5K (28dB GAIN)
R_6 = 470Ω 5% CARBON

RFC 3T # 26 BUSSWIRE ON
FERROXCUBE VK 200 09/3B CORE
BYPASS CAPACITORS
1nF CERAMIC
(MEPCO OR EQUIV.)



TOP PLANE COPPER[1] (Component Side)

COMPONENT SIDE (Component Layout)

NOTE
(X) indicates ground connection to top plane.
* R_6 is on bottom side.

BOTTOM PLANE COPPER[1]

NOTE
Bond edges of top and bottom ground plane copper.

Figure 10

SMALL SIGNAL RESPONSE

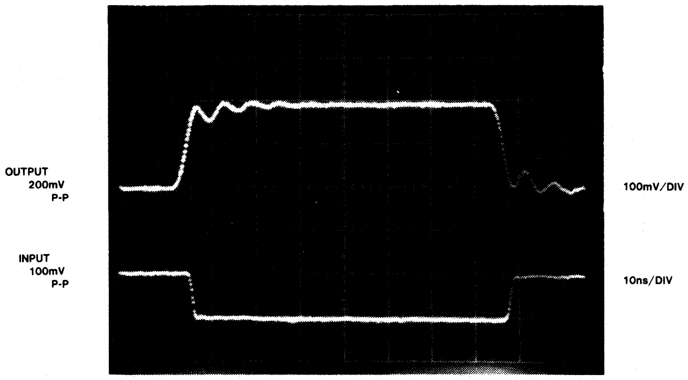


Figure 8

LARGE SIGNAL RESPONSE

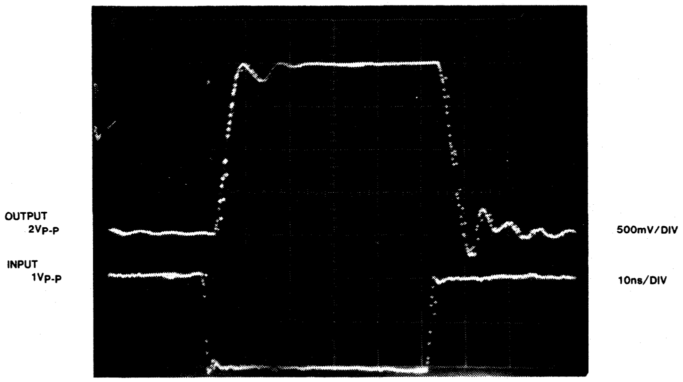


Figure 9

ULTRA HIGH FREQUENCY OPERATIONAL AMPLIFIER NE/SE5539

The primary reasoning behind this procedure is to force the closed loop circuit to appear as a gain of X7 above the critical frequency where phase changes rapidly (approx. 70MHz; refer to figure 7a). The lag network raises the phase at the upper operating frequencies, greatly improving the phase margin.

The calculations below show the application of these principles to the circuit in figure 7b.

The circuit shown has an inverting gain of 2, therefore solving for R_2:

$$R_2 \leqq \frac{R_f}{7-|A_{CL}|} \leqq \frac{2K}{7-2} = 400$$

Let $R_2 = 330\Omega$

Assuming a gain band width product of 350 MHz, C_G may now be calculated as follows:

$$\therefore C_G \simeq \frac{5}{\pi \cdot 330 \cdot 350 \cdot 10^6} \simeq \boxed{14pF}$$

In the circuit shown, a lead compensation capacitor of $\simeq$ 1.6pF was used with a value of R_2 of 330Ω and C_G was a 2 – 20pF trimmer cap (JFD piston-type). Rise and fall times of 2.8 to 3ns were measured in the small signal mode with quite adequate range in the lag compensation trimmer to optimize overshoot and reduce ringing (see pulse response—figures 9 and 10).

INVERTING GAIN OF 7
GAIN-PHASE RESPONSE
(UNCOMPENSATED)

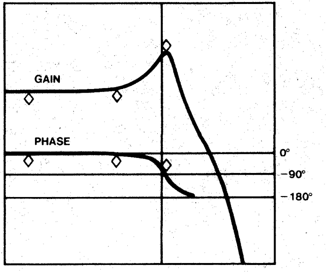
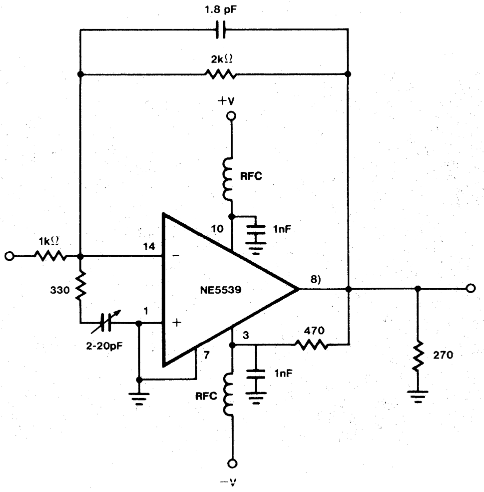


Figure 7a

NE5539
INVERTING GAIN OF 2 AMPLIFIER



Note
Resistors - ¼ watt carbon.
RFC-3T #26 buss wire on Ferroxcube VK200 09/3B wideband threaded core.

Figure 7b

CIRCUIT LAYOUT CONSIDERATIONS

As may be expected for an ultra-high frequency, wide gain bandwidth amplifier, the physical circuit layout is extremely critical. A double-sided printed circuit board will result in more favorable system operation (see figure 10).

The effect of the distributed and input capacitance added by the inverting node of the amplifier must be considered when calculating actual system closed loop performance. The RC product of the input resistor (R_{IN}) in parallel with C_{dist}. and feedback resistor (R_F) create a pole at pin 14 (figure 5). This frequency must fall beyond the unity gain frequency of the system in order to maintain stability and system performance.

CLOSED LOOP GAIN LESS THAN 7

The NE5539 is stable for all closed loop gains greater than seven (7). When operating at gains less than seven (7), the device can become unstable. The circuit in figure 7 is an example of a unity gain inverting amplifier. The compensation components are added to obtain stable operation.

Capacitor C_L improves the phase margin (of the operational amplifier) by compensating for the lag introduced by the distributed capacitor (C_D).

It can be shown that the optimal conditions for amplifier stability occur when $R_1C_D = R_FC_L$; however, when the stability criteria is obtained, it should be noted that the actual bandwidth of the closed loop amplifier will be reduced.

The actual value for C_L, based on a distributed capacitance of 3.5pFd, would be $\simeq$ 2pF.

NON-INVERTING BLOCK DIAGRAM

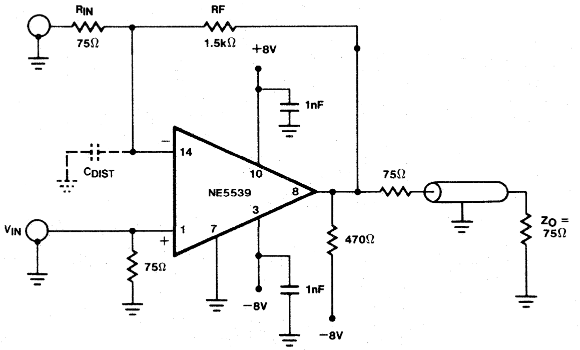


Figure 5

WIDE BAND UNITY GAIN INVERTING AMPLIFIER CIRCUIT IN A 75Ω SYSTEM

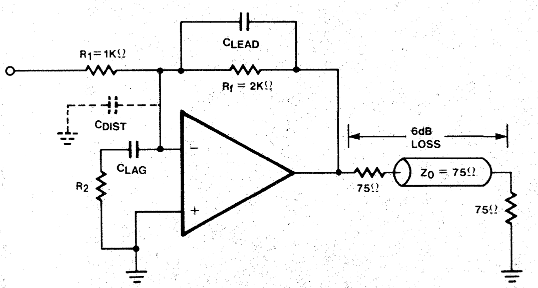


Figure 6

Determination of Compensation Capacitance:

$$C_{lead} = \frac{C_{dist}}{A_{CL}}$$

The above equation defines the relationship between the distributed capacitance, closed loop gain (A_{CL}), and the compensation capacitor (C_L). For closed loop stability and gains less than 5, C_{lead} becomes a practical consideration. When bandwidth is of primary concern, the simple lead compensation will usually be adequate. However, if transient response is also a factor in the design, then a lag compensation network (C_G, R_2) may be necessary.

For practical applications, the following equations can be used to determine the proper lag compensation components:

$$\frac{R_f}{R_1 \,||\, R_2} \geq 7 \qquad \text{(Equation 1)}$$

$$\therefore R_2 \leq \frac{R_f}{7 - A_{CL}} \qquad \text{(Equation 2)}$$

(Using Equation 1 to insure a closed loop gain of X7 above the network break frequency allows you to solve for R_2, the lag network resistor.)

C_{lag} may be approximated by the following equations. First set the lag network break frequency in relation to the amplifier total gain product (open loop).

$$\text{Set } \omega_{lag} \simeq \frac{2\pi \cdot GBW}{10} \text{ rad/sec}$$

$$\simeq \frac{\pi \cdot GBW}{5} \text{ rad/sec,}$$

$$\text{then } \omega_{lag} = \frac{1}{R_2C_{lag}}$$

and C_{lag} may now be determined.

$$\therefore C_{lag} \simeq \frac{5}{\pi \cdot R_2 \cdot GBW}$$

< Assume GBW = 350MHz > (Equation 3)

ULTRA HIGH FREQUENCY OPERATIONAL AMPLIFIER NE/SE5539

NE5539 VIDEO AMPLIFIER

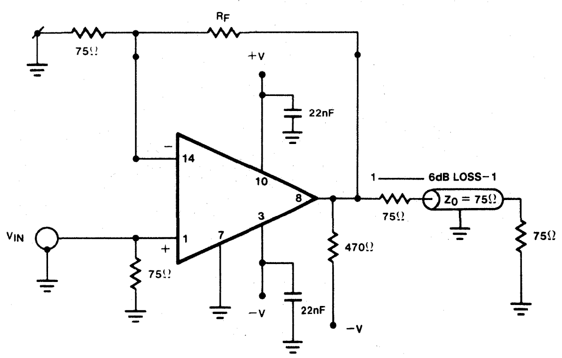


Figure 1

NE5539 NTSC VECTOR POLAR GRAPH

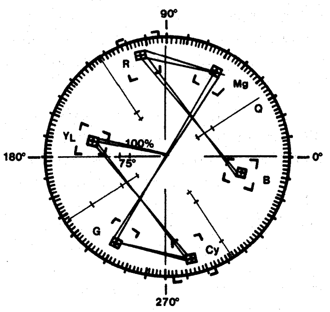
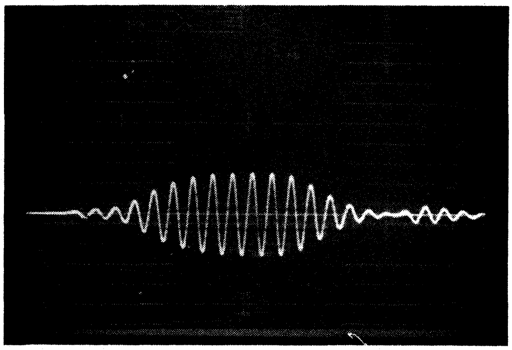


Figure 2

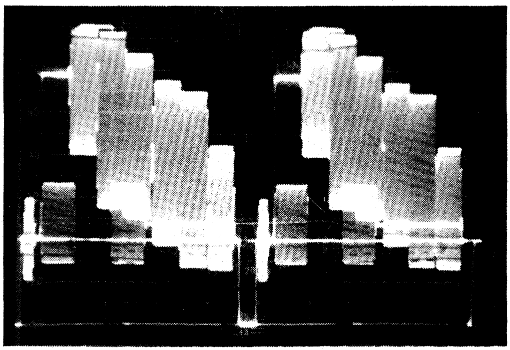
3.58MHz BURST SIGNAL



NOTE
3.58MHz burst through a 5539 20dB amplifier.

Figure 3

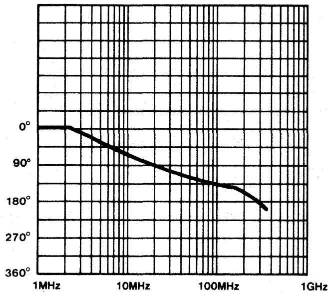
NTSC OUTPUT SIGNAL



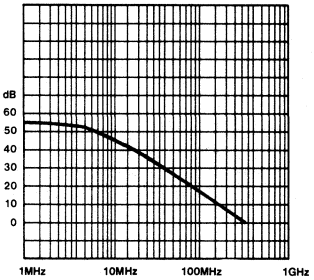
NOTE
Output of NE5539 20dB amplifier.
Z in = 75Ω's
Z out = 75Ω's

Figure 4

NE5539 OPEN LOOP PHASE

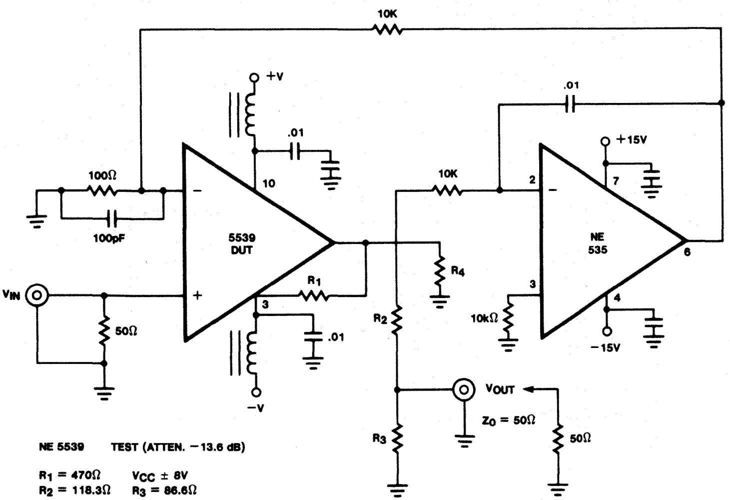


NE5539 OPEN LOOP GAIN



ULTRA HIGH FREQUENCY OPERATIONAL AMPLIFIER NE/SE5539

OPEN LOOP GAIN/PHASE TEST CIRCUIT



NE 5539 TEST (ATTEN. −13.6 dB)

R_1 = 470Ω V_{CC} ± 8V
R_2 = 118.3Ω R_3 = 86.6Ω
SE 5539 TEST (ATTEN −1.7 dB) (TERMINATED)
R_1 = 390Ω V_{CC} ± 6V
R_2 = 140Ω
R_3 = 75Ω R_4 = 470Ω

GENERAL PURPOSE OPERATIONAL AMPLIFIER μA741/μA741C/SA741C

DESCRIPTION

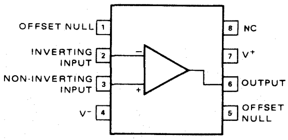
The μA741 is a high performance operational amplifier with high open loop gain, internal compensation, high common mode range and exceptional temperature stability. The μA741 is short-circuit protected and allows for nulling of offset voltage.

FEATURES

- **Internal frequency compensation**
- **Short circuit protection**
- **Excellent temperature stability**
- **High input voltage range**

PIN CONFIGURATION

D,FE,N PACKAGE



TOP VIEW

ORDER NUMBERS

μA741N μA741FE
μA741CN μA741CFE
SA741CN
μA741CD

ABSOLUTE MAXIMUM RATINGS

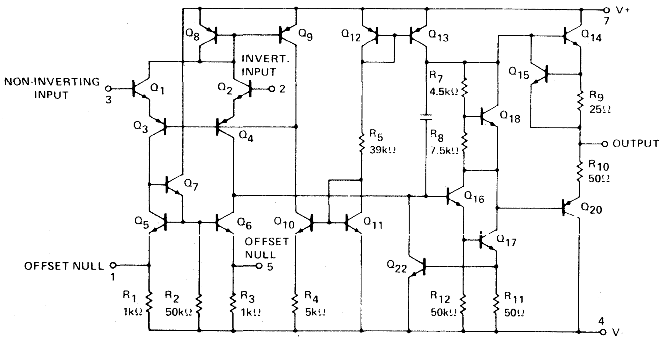
PARAMETER	RATING	UNIT
Supply voltage		
μA741C	±18	V
μA741	±22	V
Internal power dissipation		
N package	500	mW
FE package	1000	mW
Differential input voltage	±30	V
Input voltage[1]	±15	V
Output short-circuit duration	Continuous	
Operating temperature range		
μA741C	0 to +70	°C
SA741C	-40 to +85	°C
μA741	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 60sec)	300	°C

NOTE

1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

EQUIVALENT SCHEMATIC

μA741, μA741C, SA741C



GENERAL PURPOSE OPERATIONAL AMPLIFIER μA741/μA741C/SA741C

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = \pm15V$, unless otherwise specified.

PARAMETER		TEST CONDITIONS	μA741			μA741C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S = 10k\Omega$		1.0	5.0		2.0	6.0	mV
		$R_S = 10k\Omega$, over temp.		1.0	6.0			7.5	mV
I_{OS}	Offset current			20	200		20	200	nA
		Over temp.						300	nA
		$T_A = +125°C$		7.0	200				nA
		$T_A = -55°C$		20	500				nA
I_{BIAS}	Input bias current			80	500		80	500	nA
		Over temp.						800	nA
		$T_A = +125°C$		30	500				nA
		$T_A = -55°C$		300	1500				nA
V_{OUT}	Output voltage swing	$R_L = 10k\Omega$	±12	±14		±12	±14		V
		$R_L = 2k\Omega$, over temp.	±10	±13		±10	±13		V
A_{VOL}	Large signal voltage gain	$R_L = 2k\Omega$, $V_O = \pm10V$	50	200		20	200		V/mV
		$R_L = 2k\Omega$, $V_O = \pm10V$, over temp.	25			15			V/mV
	Offset voltage adjustment range			±30			±30		mV
PSRR	Supply voltage rejection ratio	$R_S \leq 10k\Omega$					10	150	μV/V
		$R_S \leq 10k\Omega$, over temp.		10	150				μV/V
CMRR	Common mode rejection ratio								dB
		Over temp.	70	90					dB
I_{CC}	Supply current			1.4	2.8		1.4	2.8	mA
		$T_A = +125°C$		1.5	2.5				mA
		$T_A = -55°C$		2.0	3.3				mA
V_{IN}	Input voltage range	(μA741, over temp.)	±12	±13		±12	±13		V
R_{IN}	Input resistance		0.3	2.0		0.3	2.0		MΩ
P_d	Power consumption			50	85		50	85	mW
		$T_A = +125°C$		45	75				mW
		$T_A = -55°C$		45	100				mW
R_{OUT}	Output resistance			75			75		Ω
I_{SC}	Output short-circuit current			25			25		mA

GENERAL PURPOSE OPERATIONAL AMPLIFIER μA741/μA741C/SA741C

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$, $V_S = \pm15V$, unless otherwise specified.

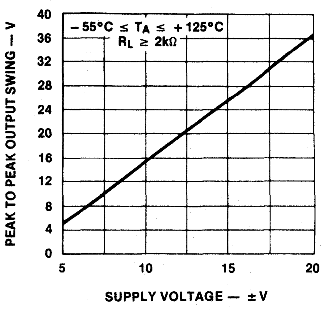
PARAMETER		TEST CONDITIONS	SA741C			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage	$R_S = 10k\Omega$		2.0	6.0	mV
		$R_S = 10k\Omega$, over temp.			7.5	mV
I_{OS}	Offset current			20	200	nA
		Over temp.			500	nA
I_{BIAS}	Input bias current			80	500	nA
		Over temp.			1500	nA
V_{OUT}	Output voltage swing	$R_L = 10k\Omega$	±12	±14		V
		$R_L = 2k\Omega$, over temp.	±10	±13		V
A_{VOL}	Large signal voltage gain	$R_L = 2k\Omega$, $V_O = \pm10V$	20	200		V/mV
		$R_L = 2k\Omega$, $V_O = \pm10V$, over temp.	15			V/mV
	Offset voltage adjustment range			±30		mV
PSRR	Supply voltage rejection ratio	$R_S \leq 10k\Omega$		10	150	µV/V
CMRR	Common mode rejection ratio					dB
I_{CC}	Supply current			1.4	2.8	mA
V_{IN}	Input voltage range	(μA741, over temp.)	±12	±13		V
	Input resistance		0.3	2.0		MΩ
P_d	Power consumption			50	85	mW
R_{OUT}	Output resistance			75		Ω
I_{SC}	Output short-circuit current			25		mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm15V$, unless otherwise specified.

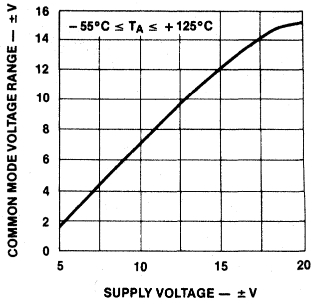
PARAMETER	TEST CONDITIONS	μA741, μA741C			UNIT
		Min	Typ	Max	
Parallel input resistance	Open loop, f = 20Hz				MΩ
Parallel input capacitance	Open loop, f = 20Hz		1.4		pF
Unity gain crossover frequency	Open loop		1.0		MHz
Transient response unity gain	$V_{IN} = 20mV$, $R_L = 2k\Omega$, $C_L \leq 100pf$				
Rise time			0.3		µs
Overshoot			5.0		%
Slew rate	$C \leq 100pf$, $R_L \geq 2k$, $V_{IN} = \pm10V$		0.5		V/µs

TYPICAL PERFORMANCE CHARACTERISTICS

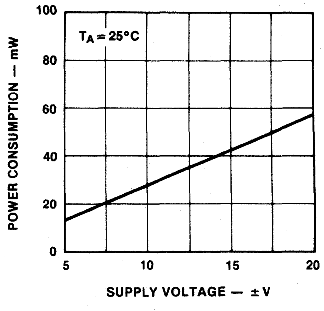
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

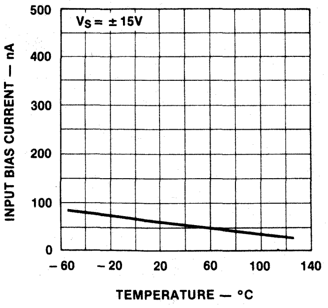


POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE

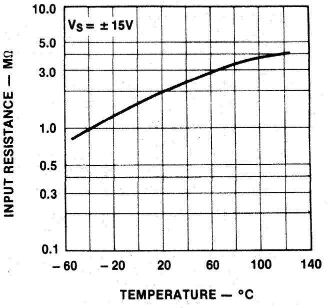


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

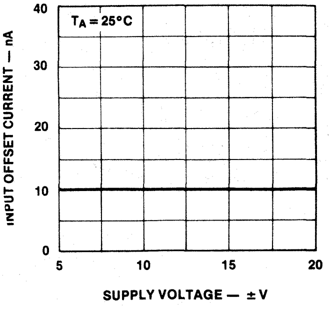
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



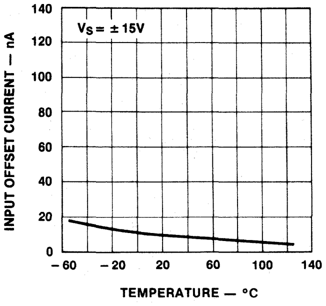
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



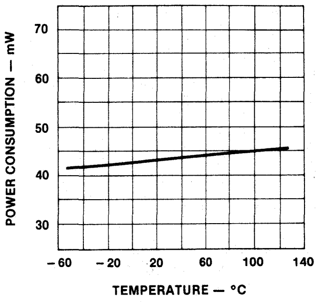
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



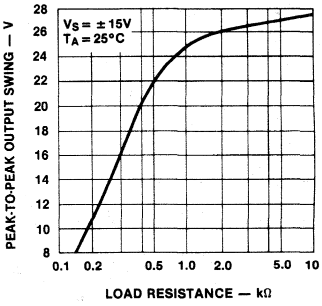
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



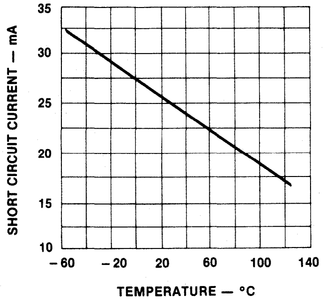
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



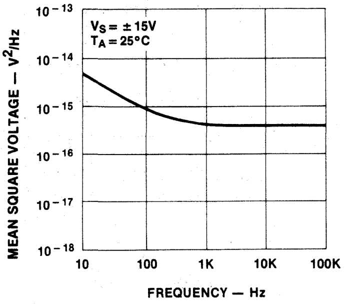
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



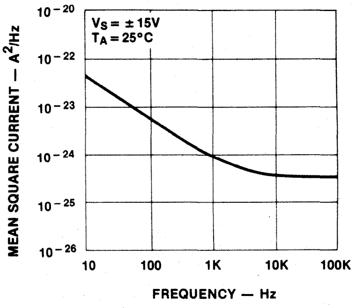
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY

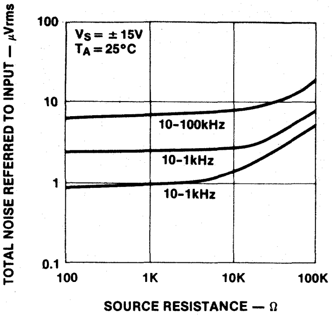


INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY

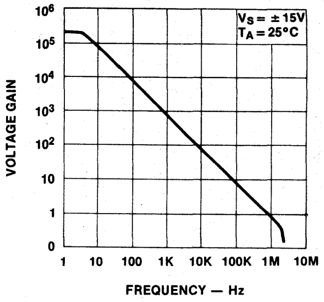


GENERAL PURPOSE OPERATIONAL AMPLIFIER μA741/μA741C/SA741C

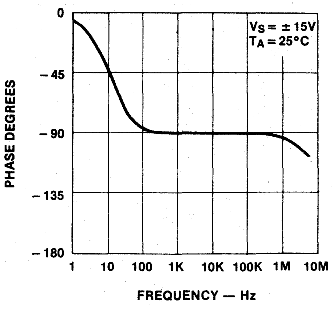
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)



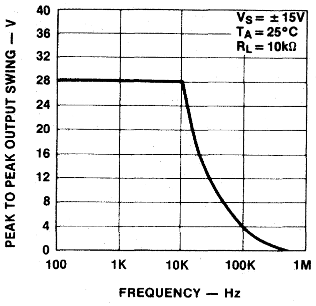
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



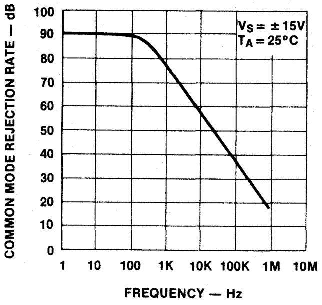
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



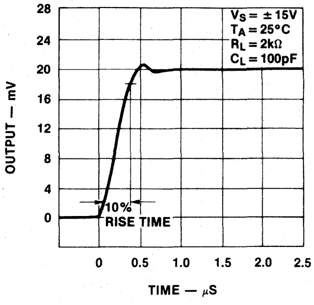
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



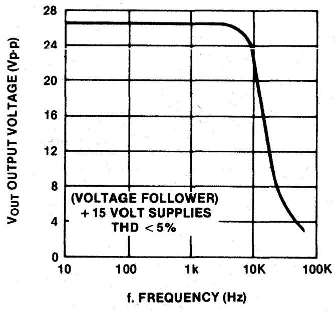
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



TRANSIENT RESPONSE



POWER BANDWIDTH (Large Signal Swing vs Frequency)

DUAL OPERATIONAL AMPLIFIER

μA747/747C/SA747C

DESCRIPTION

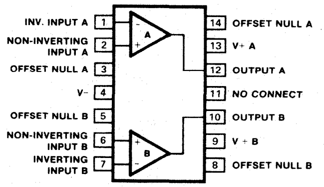
The 747 is a pair of high performance monolithic operational amplifiers constructed on a single silicon chip. High common mode voltage range and absence of "latch-up" make the 747 ideal for use as a voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications. The 747 is short-circuit protected and requires no external components for frequency compensation. The internal 6dB/octave roll-off insures stability in closed loop applications. For single amplifier performance, see μA741 data sheet.

FEATURES

- **No frequency compensation required**
- **Short-circuit protection**
- **Offset voltage null capability**
- **Large common-mode and differential voltage ranges**
- **Low power consumption**
- **No latch-up**

PIN CONFIGURATIONS

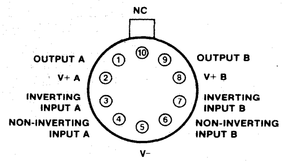
D,F,N PACKAGE



TOP VIEW

ORDER NUMBERS
μA747CN, μA747CF, μA747N,
μA747F, SA747CN, μA747C

H PACKAGE*



ORDER NUMBERS
μA747CH, μA747H

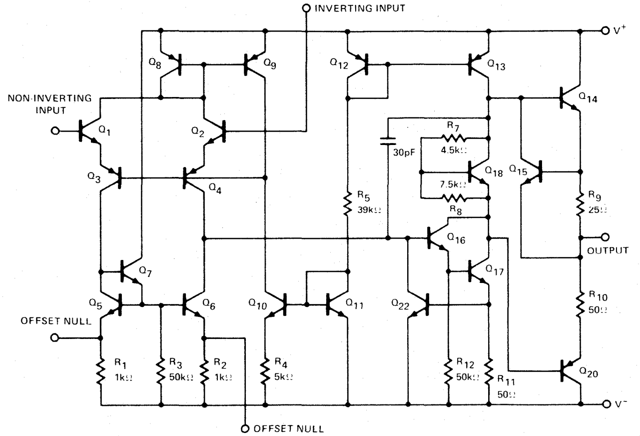
*Metal cans (H) not recommended for new designs

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
μA747	±22	V
μA747C	±18	V
SA747C	±18	V
Internal power dissipation		
H Package	500	mW
N,F Packages	670	mW
Differential input voltage	±30	V
Input voltage	±15	V
Voltage between offset null and V-	±0.5	V
Storage temperature range	-65 to +155	°C
Operating temperature range		
μA747	-55 to +125	°C
μA747C	0 to +70	°C
SA747C	-40 to +85	°C
Lead temperature (soldering, 60 sec)	300	°C
Output short-circuit duration	indefinite	

EQUIVALENT SCHEMATIC

EQUIVALENT CIRCUIT (EACH SIDE)



DUAL OPERATIONAL AMPLIFIER μA747/747C/SA747C

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = ±15V$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SA747C			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage	$R_S \leq 10k\Omega$		2.0	6.0	mV
		$R_S \leq 10k\Omega$, over temp		3.0	7.5	mV
I_{OS}	Offset current			20	200	nA
		Over temp			500	nA
I_{BIAS}	Input current				500	nA
		Over temp			1500	nA
V_{OUT}	Output voltage swing	$R_L \geq 2k\Omega$, over temp	±10	±13		V
		$R_L \geq 10k\Omega$, over temp	±12	±14		V
I_{CC}	Supply current			1.7	2.8	mA
		Over temp		2.0	3.3	mA
	Power consumption			50	85	mW
		Over temp		60	100	mW
	Input capacitance			1.4		pF
	Offset voltage adjustment range			±15		V
	Output resistance			75		Ω
	Channel separation			120		dB
PSRR	Supply voltage rejection ratio	$R_S \leq 10k\Omega$, over temp		30	150	μV/V
A_{VOL}	Large signal voltage gain (DC)	$R_L \geq 2k\Omega$ $V_{OUT} = \pm 10V$	25,000			V/V
CMRR		$R_S \leq 10K\Omega$, V_{CM} ±12V over temp	70			dB

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = ±15V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	μA747/μA747C/SA747C			UNIT
		Min	Typ	Max	
Transient response	$V_{IN} = 20mV$, $R_1 = 2k\Omega$, $C_1 < 100pf$				
Risetime	Unity gain CL ≤ 100pf		0.3		μs
Overshoot	Unity gain CL ≤ 100pf		5.0		%
Slew rate	RL > 2kΩ		0.5		V/μs

DUAL OPERATIONAL AMPLIFIER μA747/747C/SA747C

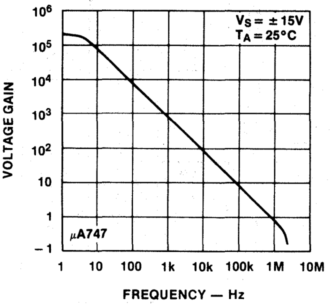
DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm15V$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	μA747			μA747C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S \leq 10k\Omega$		2.0	5.0		2.0	6.0	mV
		$R_S \leq 10k\Omega$, over temp		3.0	6.0		3.0	7.5	mV
I_{OS}	Offset current			20	200		20	200	nA
		$T_A = +125°C$		7.0	200				nA
		$T_A = -55°C$		85	500				nA
		Over temp					7.0	300	nA
I_{BIAS}	Input current			80	500		80	500	nA
		$T_A = 125°C$		30	500				nA
		$T_A = -55°C$		300	1500				nA
		Over temp					30	800	nA
V_{OUT}	Output voltage swing	$R_L \geq 2k\Omega$, over temp	±10	±13		±10	±13		V
		$R_L \geq 10k\Omega$, over temp	±12	±14		±12	±14		V
I_{CC}	Supply current each side			1.7	2.8		1.7	2.8	mA
		$T_A = 125°C$		1.5	2.5				mA
		$T_A = -55°C$		2.0	3.3				mA
		Over temp					2.0	3.3	mA
	Power consumption			50	85		50	85	mW
		$T_A = 125°C$		45	75				mW
		$T_A = -55°C$		60	100				mW
		Over temp					60	100	mW
	Input capacitance			1.4			1.4		pF
	Offset voltage adjustment range			±15			±15		V
	Output resistance			75			75		Ω
	Channel separation			120			120		dB
PSRR	Supply voltage rejection ratio	$R_S \leq 10k\Omega$, over temp		30	150		30	150	μV/V
A_{VOL}	Large signal voltage gain (DC)	$R_L \geq 2k\Omega$ $V_{OUT} = \pm10V$	50,000			25,000			V/V
		Over temp	25,000			15,000			V/V
CMRR		$R_S \leq 10K\Omega$, V_{CM} ±12V over temp	70			70			dB

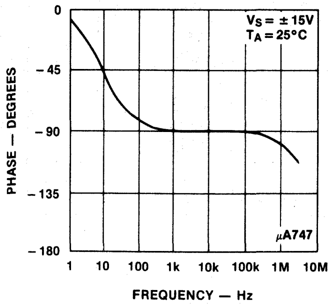
DUAL OPERATIONAL AMPLIFIER μA747/747C/SA747C

TYPICAL PERFORMANCE CHARACTERISTICS

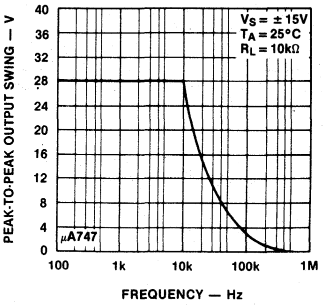
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



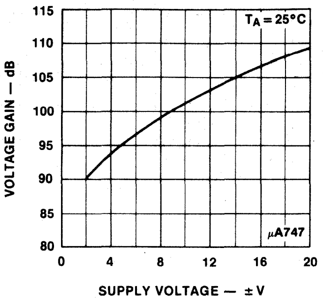
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



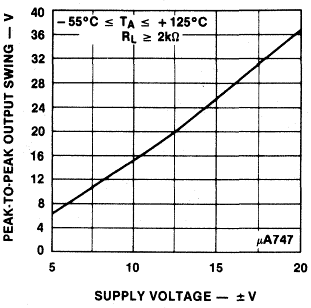
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



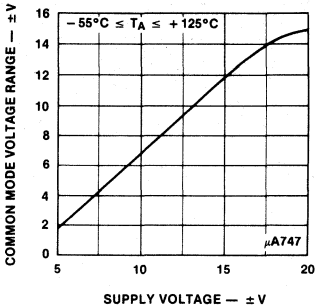
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



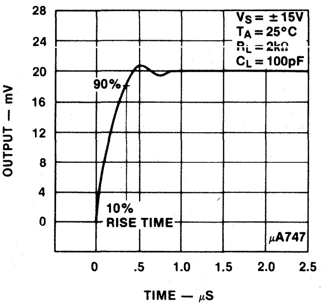
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



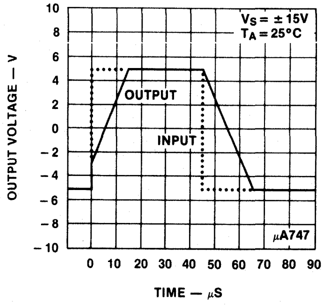
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



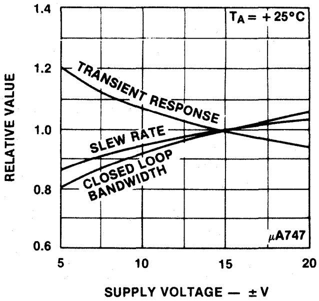
TRANSIENT RESPONSE



VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE

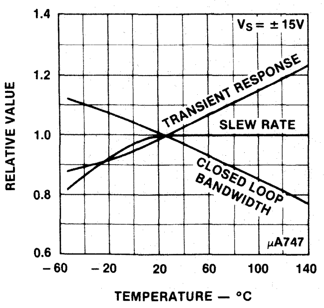


FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE

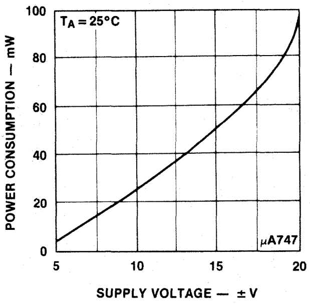


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

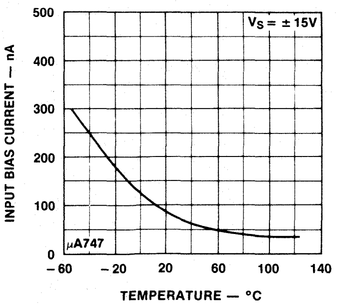
FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



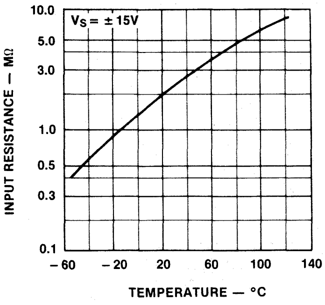
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



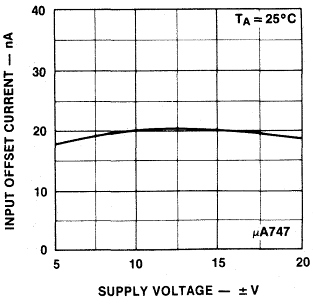
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



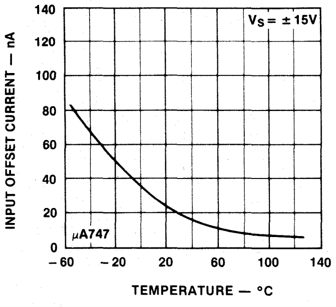
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



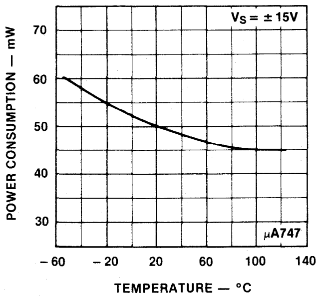
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



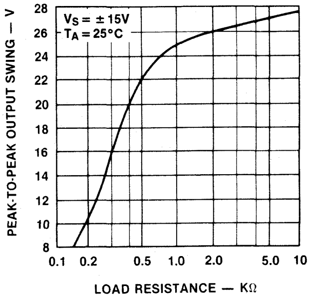
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



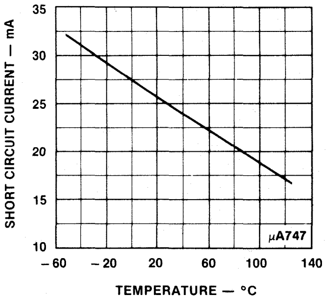
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

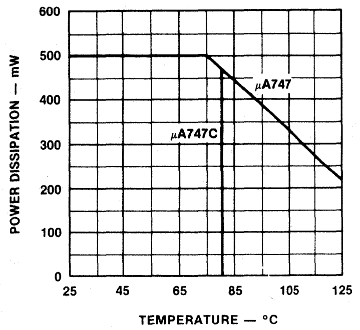


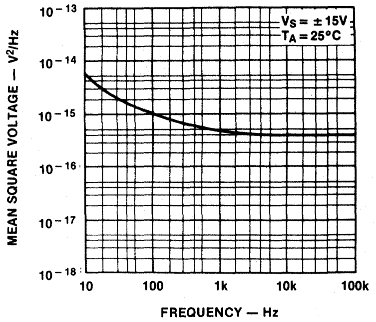
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

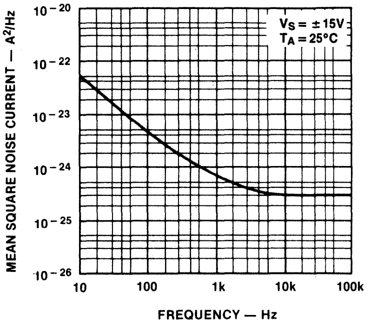


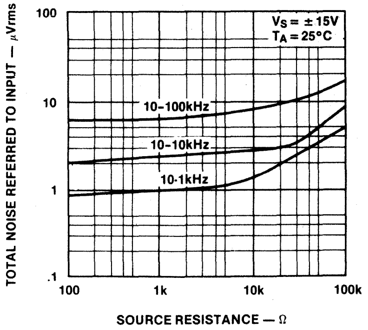
DUAL OPERATIONAL AMPLIFIER µA747/747C/SA747C

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

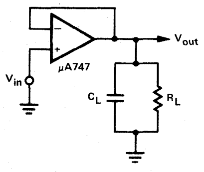

ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE

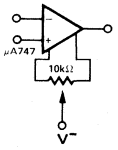

INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY


INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY


BROADBAND NOISE FOR VARIOUS BANDWIDTHS

TEST CIRCUITS


TRANSIENT RESPONSE TEST CIRCUIT


VOLTAGE OFFSET NULL CIRCUIT

GENERAL PURPOSE OPERATIONAL AMPLIFIER µA748/748C

DESCRIPTION

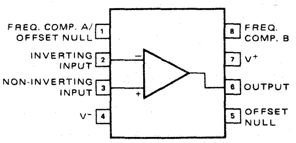
The 748 is a High Performance Operational Amplifier featuring high gain, short circuit immunity, offset voltage null capability, simplified compensation and excellent temperature stability.

FEATURES

- **Short circuit protection**
- **Offset voltage null capability**
- **Large common-mode and differential voltage ranges**
- **Low power consumption**
- **No latch-up**

PIN CONFIGURATION

D, N, FE PACKAGE



TOP VIEW

ORDER NUMBERS

µA748N	**µ748FE**
µA748CN	**µ748CFE**
µA748CD	

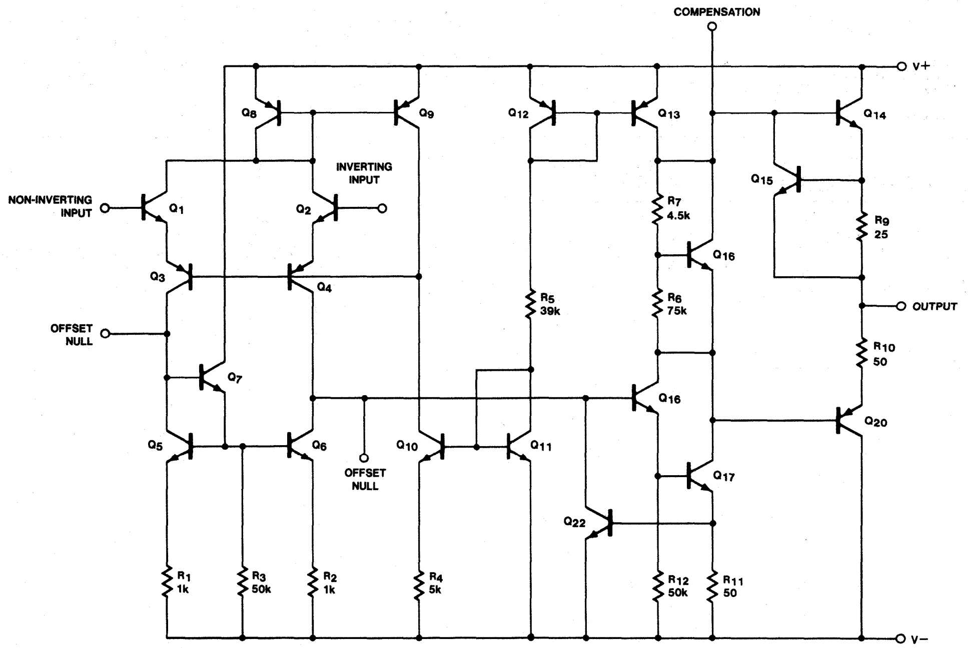
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
µA748	±22	V
µA748C	±18	V
Internal power dissipation[1]	500	mW
Differential output voltage	±30	V
Input voltage[2]	±15	V
Storage temperature range	-65 to +150	°C
Operating temperature range		
µA748	-55 to +125	°C
µA748C	0 to +70	°C
Lead temperature	300	°C
Output short circuit duration[3]	indefinite	

NOTES

1. Rating applies for case temperatures to +70°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +70°C ambient temperature.

EQUIVALENT CIRCUIT



NOTE

All resistors values are typical and in ohms.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	μA748			μA748C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S \leq 10k\Omega$, $T_A = 25°C$		1.0	5.0		2.0	6.0	mV
		Over temperature			6.0			7.5	mV
I_{OS}	Offset current			20	200		20	200	nA
		$25° \leq T_A \leq T_{max}$		7.0	200		9.0	300	nA
		$T_{min} \leq T_A \leq 25°C$		85	500		35	300	nA
I_{BIAS}	Input current			80	500		80	500	nA
		$25° \leq T_A \leq T_{max}$		30	500		40	800	nA
		$T_{min} \leq T_A \leq 25°C$		300	1500		130	800	nA
V_{CM}	Common mode voltage range	Over temperature	±12	±13		±12	±13		V

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	μA748			μA748C			UNIT
			Min	Typ	Max	Min	Typ	Max	
CMRR	Common mode rejection ratio	$R_S \leq \pm 10k\Omega$, over temperature	70	90		70	90		dB
R_{IN}	Input resistance		0.3	2.0		.30	2.0		MΩ
V_{OUT}	Output voltage swing	$R_L \geq 2k\Omega$, over temperature	±10	±13		±10	±13		V
		$R_L \geq 10k\Omega$, over temperature	±12	±14		±12	±14		V
I_{CC}	Supply current			1.7	2.83		1.7	2.83	mA
		$25° \leq T_A \leq T_{max}$		1.5	2.50		1.6	3.33	mA
		$T_{min} \leq T_A \leq 25°C$		2.0	3.33		1.8	3.33	mA
P_d	Power consumption	$T_A = 25°C$		50	85		50	85	mW
		$25° \leq T_A \leq T_{max}$		45	75		48	100	mW
		$T_{min} \leq T_A \leq 25°C$		60	100		54	100	mW
PSRR	Supply voltage rejection ratio	$R_S \leq 10k\Omega$, over temperature		30	150		30	150	μV/V
	Output resistance	$T_A = 25°C$		75			75		Ω
A_{VOL}	Large signal voltage gain	$R_L \geq 2k\Omega$ V_{OUT} ±10V ±15V	50	200		50	200		V/mV
		Over temperature	25			25			V/mV
	Input capacitance			1.4			1.4		pF
	Offset voltage adjustment range			±15			±15		mV

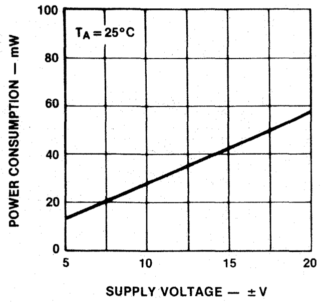
AC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	μA748			μA748C/SA748C			UNIT
		Min	Typ	Max	Min	Typ	Max	
Transient response (unity gain)	$V_{IN} = 20mV$, $R_L = 2k\Omega$							
	$C_L \leq 100pF$							
Rise time	$C_1 = 30pF$		0.3			0.3		μs
Overshoot			5.0			5.0		%
Slew rate	$R_L \geq 2k\Omega$ $C_1 = 30pF$		0.5			0.5		V/μs

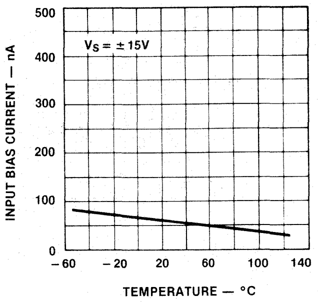
GENERAL PURPOSE OPERATIONAL AMPLIFIER μA748/748C

TYPICAL CHARACTERISTIC CURVES

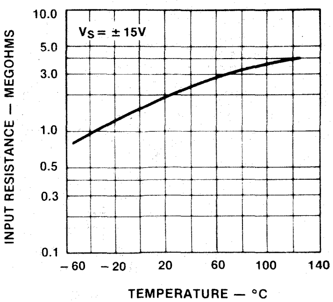
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



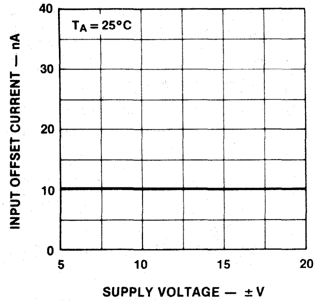
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



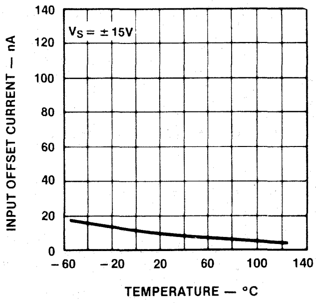
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



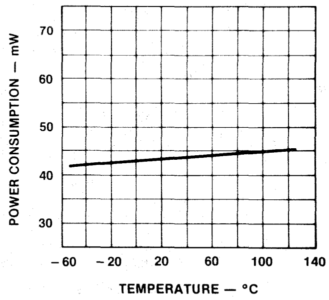
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



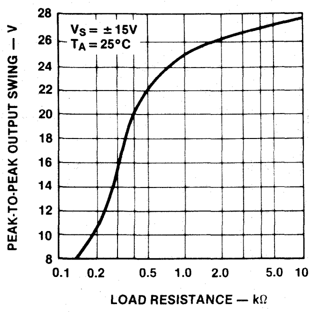
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



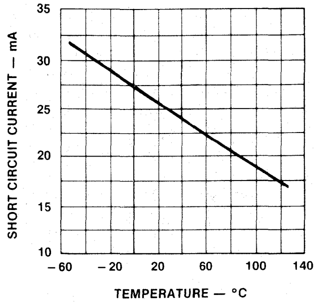
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



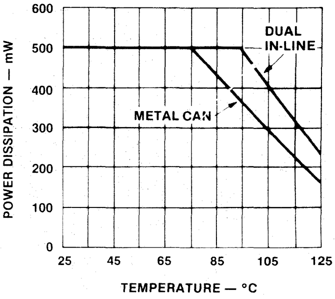
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

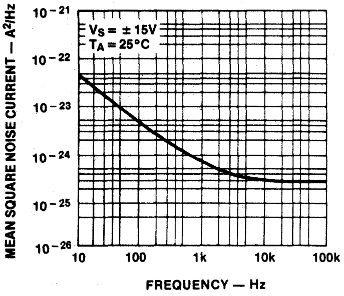


ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE

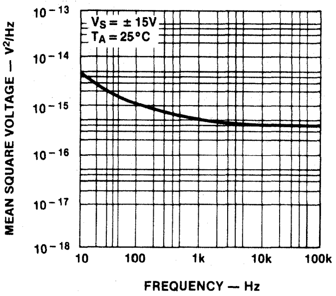


TYPICAL CHARACTERISTIC CURVES (Cont'd)

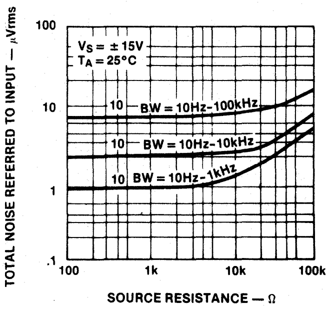
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



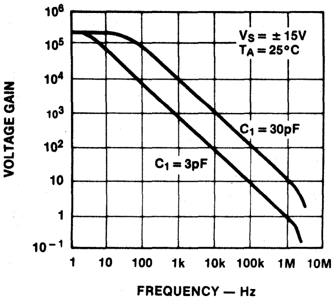
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



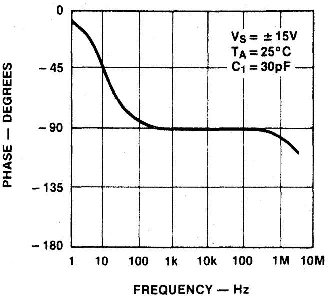
BROADBAND NOISE AS A FUNCTION OF SOURCE RESISTANCE



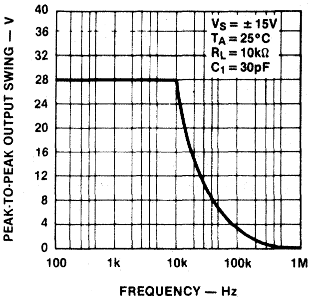
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



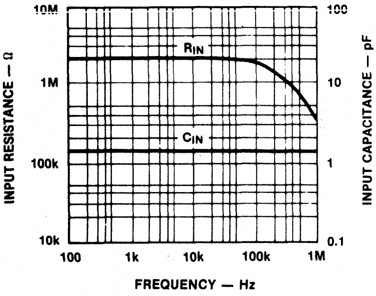
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



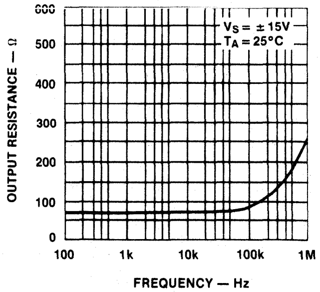
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



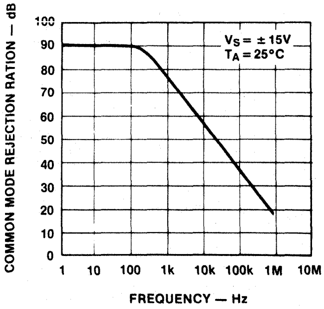
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY

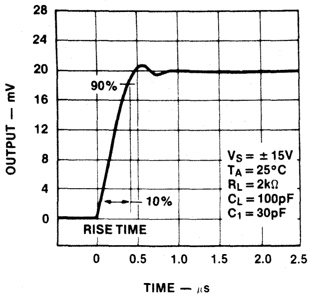


COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY

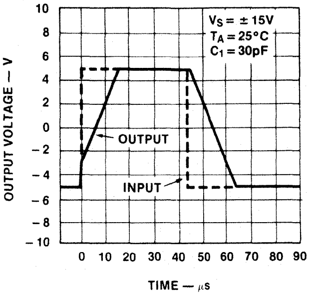


TYPICAL CHARACTERISTIC CURVES (Cont'd)

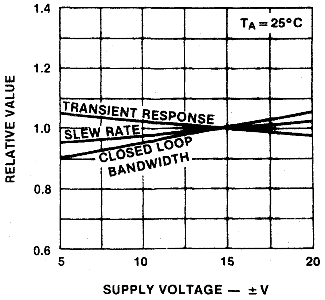
TRANSIENT RESPONSE



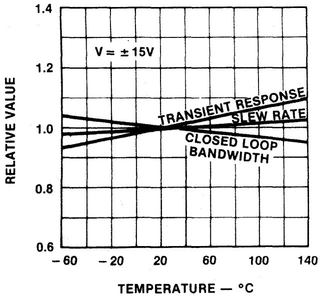
VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



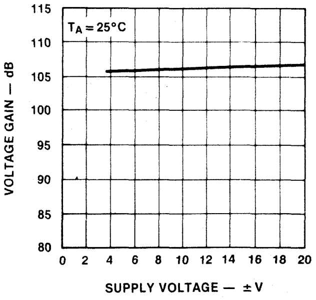
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



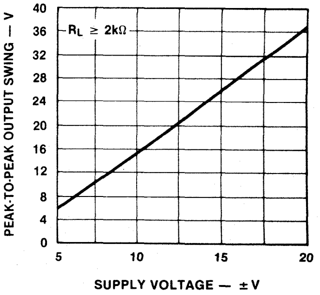
FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



Section 4
Video Amplifiers

INDEX

Section 4 — Video Amplifiers

VIDEO AMPLIFIER NE/SE592

DESCRIPTION

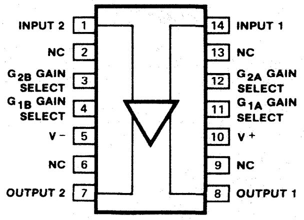
The SE/NE592 is a monolithic, two stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disc head amplifiers. The 592 is a pin-for-pin replacement for the μA733.

FEATURES

- **120MHz bandwidth**
- **Adjustable gains from 0 to 400**
- **Adjustable pass band**
- **No frequency compensation required**
- **Wave shaping with minimal external components**

PIN CONFIGURATION

D,F,N PACKAGE

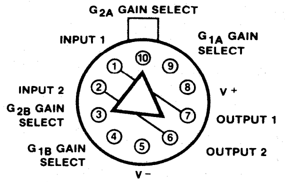


TOP VIEW

ORDER NUMBERS

NE592D NE592N
NE592F SE592F

H PACKAGE*



NOTE
Pin 5 connected to case.

ORDER NUMBERS

NE592H SE592H

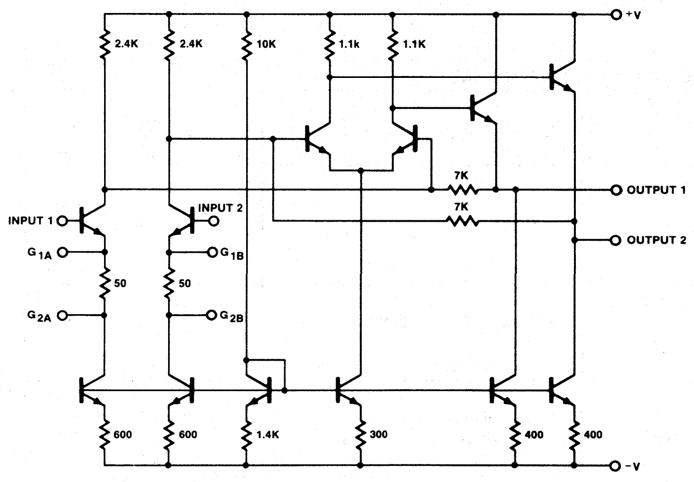
*Metal cans (H) not recommended for new designs.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25°C$ unless otherwise specified.

PARAMETER	RATING	UNIT
Supply voltage	±8	V
Differential input voltage	±5	V
Common mode		
Input voltage	±6	V
Output current	10	mA
Operating temperature range		
SE592K	-55 to +125	°C
NE592K	0 to +70	°C
Storage temperature range	-65 to +150	°C
Power dissipation	500	mW

EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS $T_A = +25°C$, $V_S = \pm 6V$, $V_{CM} = 0$ unless otherwise specified.

Recommended operating supply voltages $V_S = \pm 6.0V$

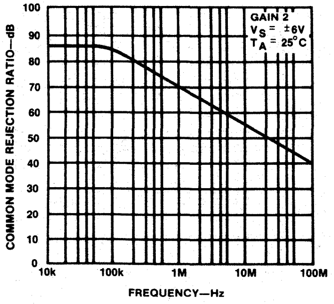
PARAMETER	TEST CONDITIONS	NE592			SE592			UNITS
		Min	Typ	Max	Min	Typ	Max	
Differential voltage gain								
Gain 1^{1}	$R_L = 2kΩ$, $V_{OUT} = 3V$ p-p	250	400	600	300	400	500	V/V
Gain 2^{2}		80	100	120	90	100	110	V/V
Bandwidth								
Gain 1^{1}			40			40		MHz
Gain 2^{2}			90			90		MHz
Rise Time								
Gain 1^{1}	$V_{OUT} = 1V$ p-p		10.5			10.5		ns
Gain 2^{2}			4.5	12		4.5	10	ns
Propagation delay								
Gain 1^{1}	$V_{OUT} = 1V$ p-p		7.5			7.5		ns
Gain 2^{2}			6.0	10		6.0	10	ns
Input resistance								
Gain 1^{1}			4.0			4.0		kΩ
Gain 2^{2}		10	30		20	30		kΩ
Input capacitance^{2}	Gain 2		2.0			2.0		pF
Input offset current			0.4	5.0		0.4	3.0	μA
Input bias current			9.0	30		9.0	20	μA
Input noise voltage	BW 1kHz to 10MHz		12			12		μVrms
Input voltage range				± 1.0			± 1.0	V
Common mode rejection ratio								
Gain 2	VCM ± 1V, F < 100kHz	60	86		60	86		dB
Gain 2	VCM ± 1V, F = 5MHz		60			60		dB
Supply voltage rejection ratio								
Gain 2	ΔVS = ± 0.5V	50	70		50	70		dB
Output offset voltage								
Gain 2^{2}	$R_L = \infty$		0.35	0.75		0.35	0.75	V
Output common mode voltage	$R_L = \infty$	2.4	2.9	3.4	2.4	2.9	3.4	V
Output voltage swing differential	$R_L = 2K$	3.0	4.0		3.0	4.0		
Output resistance			20			20		Ω
Power supply current	$R_L = \infty$		18	24		18	24	mA
THE FOLLOWING SPECS APPLY OVER TEMPERATURE		0°C ≤ T_A ≤ 70°C			− 55°C ≤ T_A ≤ 125°C			
Differential voltage gain								
Gain 1^{1}	$R_L = 2kΩ$, $V_{OUT} = 3V$ p-p	250		600	200		600	V/V
Gain 2^{2}		80		120	80		120	V/V
Input resistance								
Gain 2^{2}		8.0			8.0			kΩ
Input offset current				6.0			5.0	μA
Input bias current				40			40	μA
Input voltage range		± 1.0			± 1.0			V
Common mode rejection ratio								
Gain 2	VCM ± 1V, F < 100kHz	50			50			dB
Supply voltage rejection ratio								
Gain 2	ΔVS = ± 0.5V	50			50			dB
Output offset voltage								
Gain 2^{2}	$R_L = \infty$			0.75			0.75	V
Output voltage swing differential	$R_L = 2K$	2.5			2.5			V
Power supply current	$R_L = \infty$			27			27	mA

NOTES

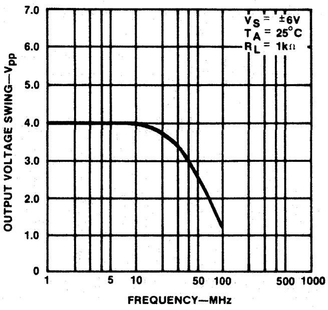
1. Gain select pins G_{1A} and G_{1B} connected together.
2. Gain select pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.

TYPICAL PERFORMANCE CHARACTERISTICS

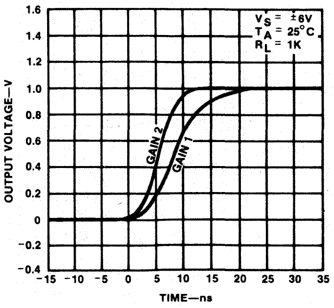
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



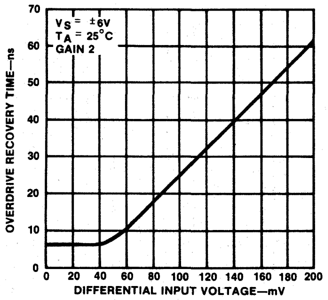
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



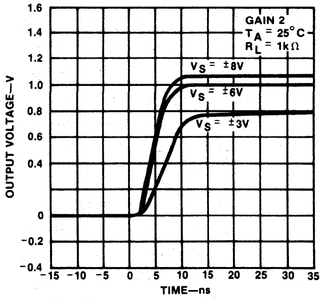
PULSE RESPONSE



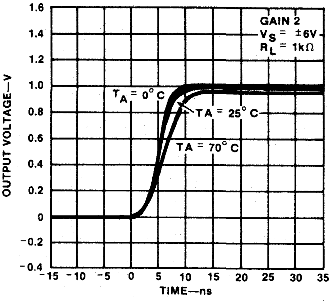
DIFFERENTIAL OVERDRIVE RECOVERY TIME



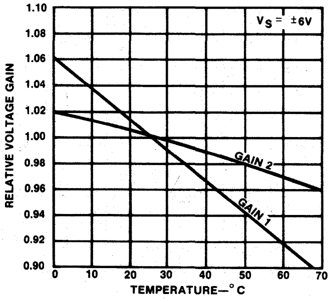
PULSE RESPONSE AS A FUNCTION OF SUPPLY VOLTAGE



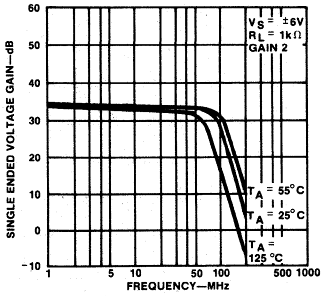
PULSE RESPONSE AS A FUNCTION OF TEMPERATURE



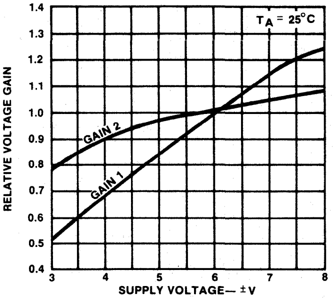
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



GAIN vs FREQUENCY AS A FUNCTION OF TEMPERATURE

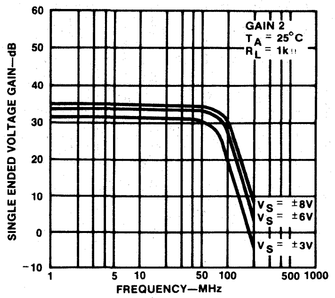


VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

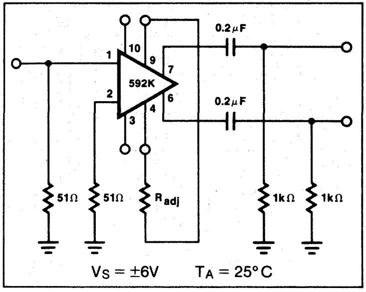


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

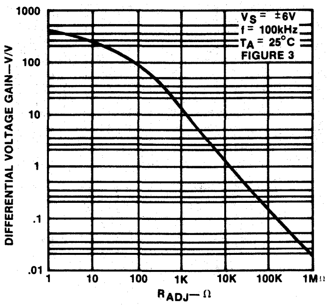
GAIN vs FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



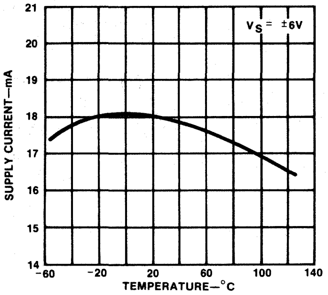
VOLTAGE GAIN ADJUST CIRCUIT



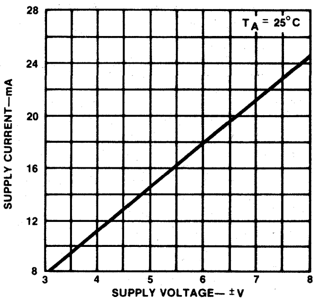
VOLTAGE GAIN AS A FUNCTION OF RADJ (FIGURE 3)



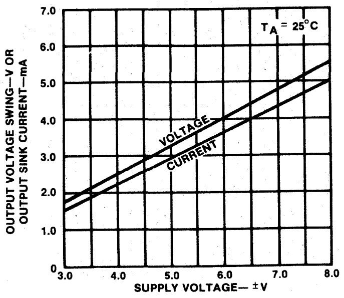
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



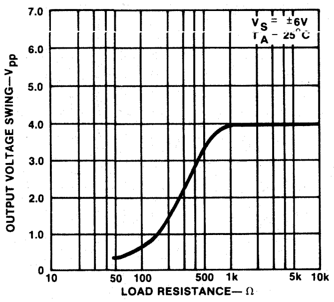
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



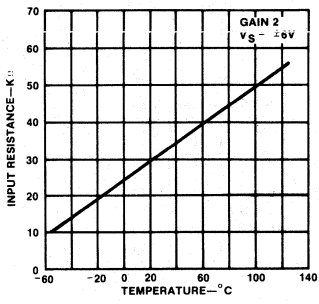
OUTPUT VOLTAGE AND CURRENT SWING AS A FUNCTION OF SUPPLY VOLTAGE



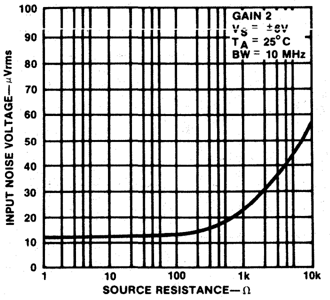
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



INPUT RESISTANCE AS A FUNCTION OF TEMPERATURE



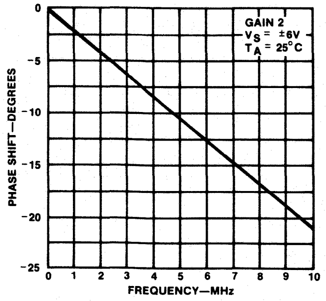
INPUT NOISE VOLTAGE AS A FUNCTION OF SOURCE RESISTANCE



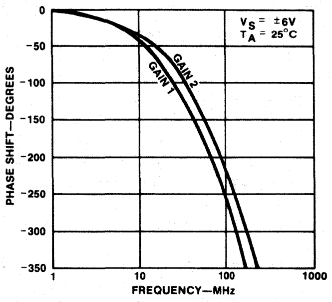
VIDEO AMPLIFIER NE/SE592

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

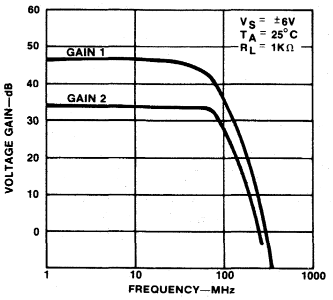
PHASE SHIFT AS A FUNCTION OF FREQUENCY



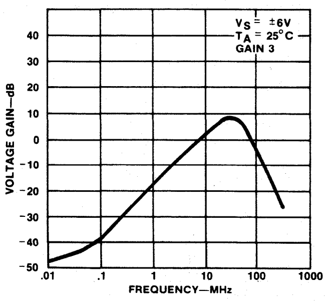
PHASE SHIFT AS A FUNCTION OF FREQUENCY



VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

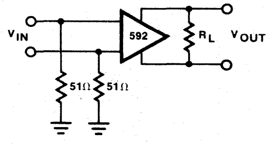


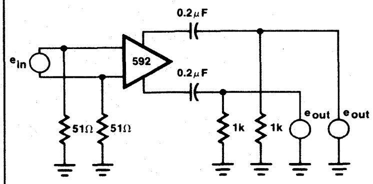
VOLTAGE GAIN AS A FUNCTION OF FREQUENCY (ALL GAIN SELECT PINS OPEN)



TEST CIRCUITS

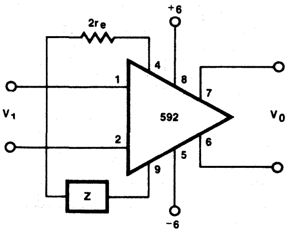
T_A = 25°C unless otherwise specified





TYPICAL APPLICATIONS

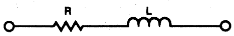
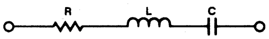
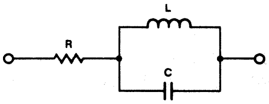
FILTER NETWORKS



$$\frac{V_0\,(s)}{V_1\,(s)} \cong \frac{1.4 \times 10^4}{Z(s) + 2r_e}$$

$$\cong \frac{1.4 \times 10^4}{Z(s) + 32}$$

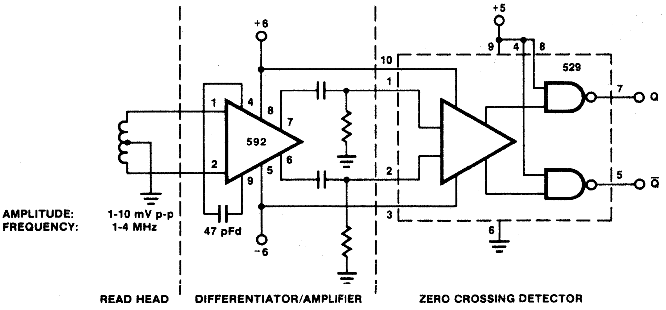
BASIC CONFIGURATION

Z NETWORK	FILTER TYPE	V_0 (s) TRANSFER V_1 (s) FUNCTION
	LOW PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
	HIGH PASS	$\frac{1.4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$
	BAND PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/L\ s + 1/LC}\right]$
	BAND REJECT	$\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

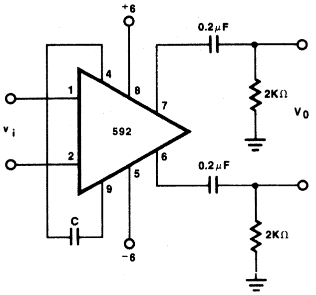
NOTE

In the networks above, the R value used is assumed to include $2r_e$, or approximately 32Ω.

DISC/TAPE PHASE MODULATED READBACK SYSTEMS



DIFFERENTIATION WITH HIGH COMMON MODE NOISE REJECTION



FOR FREQUENCY $F_1 << 1/2\,\pi\,(32)\,C$

$V_0 \cong 1.4 \times 10^4 C \frac{dVi}{dT}$

DIFFERENTIAL VIDEO AMPLIFIER

μA733/733C

DESCRIPTION

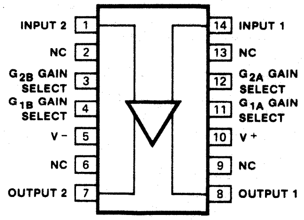
The 733 is a monolithic differential input, differential output, wideband video amplifier. It offers fixed gains of 10,100 or 400 without external components, and adjustable gains from 10 to 400 by the use of an external resistor. No external frequency compensation components are required for any gain option. Gain stability, wide bandwidth and low phase distortion are obtained through use of the classic series-shunt feedback from the emitter follower outputs to the inputs of the second stage. The emitter follower outputs provide low output impedance, and enable the device to drive capacitive loads. The 733 is intended for use as a high performance video and pulse amplifier in communications, magnetic memories, display and video recorder systems.

FEATURES

- **120MHz bandwidth**
- **250kΩ input resistance**
- **Selectable gains of 10,100 and 400**
- **No frequency compensation required**
- **Mil std 883A,B,C available**

PIN CONFIGURATION

F,N PACKAGE

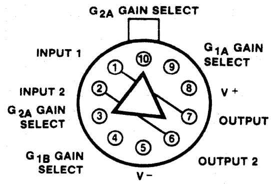


TOP VIEW

ORDER NUMBERS

μA733F	μA733CN
μA733N	μA733CF

H PACKAGE*



NOTE
Pin 5 connected to case.

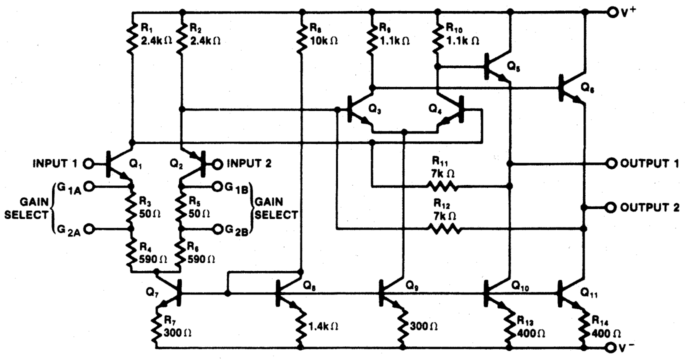
ORDER NUMBER
μA733H

*Metal cans (H) not recommended for new designs.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Differential input Voltage	±5	V
Common mode input Voltage	±6	V
V_{CC}	±8	V
Ouput current	10	mA
Junction temperature	+150	°C
Storage temperature range	-65 to +150	°C
Operation temperature range		
μA733C	0 to +75	°C
μA733	-55 to +125	°C
P_D Power dissipation		
K package	500	mW
N, F package	670	mW

CIRCUIT SCHEMATIC



DIFFERENTIAL VIDEO AMPLIFIER μA733/733C

DC ELECTRICAL CHARACTERISTICS

T_A = +25°C, V_S = ±V, VCM = 0 unless otherwise specified.
Recommended operating supply voltages V_S = ±6.0V.

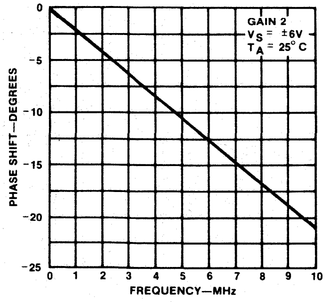
PARAMETER	TEST CONDITIONS	μA733C			μA733			UNITS
		Min	Typ	Max	Min	Typ	Max	
Differential voltage gain								
Gain 1[1]		250	400	600	300	400	500	V/V
Gain 2[2]	R_I = 2kΩ, V_{OUT} = 3Vp-p	80	100	120	90	100	110	V/V
Gain 3[3]		8.0	10	12	9.0	10	11	V/V
Bandwidth								
Gain 1[1]			40			40		MHz
Gain 2[2]			90			90		MHz
Gain 3[3]			120			120		MHz
Rise time								
Gain 1[1]			10.5			10.5		ns
Gain 2[2]	V_{OUT} = 1Vp-p		4.5	12		4.5	10	ns
Gain 3[3]			2.5			2.5		ns
Propagation delay								
Gain 1[1]			7.5			7.5		ns
Gain 2[2]	V_{OUT} = 1Vp-p		6.0	10		6.0	10	ns
Gain 3[3]			3.6			3.6		ns
Input resistance								
Gain 1[1]			4.0			4.0		kΩ
Gain 2[2]		10	30		20	30		kΩ
Gain 3[3]			250			250		kΩ
Input capacitance[2]	Gain 2		2.0			2.0		pF
Input offset current			0.4	5.0		0.4	3.0	μA
Input bias current			9.0	30		9.0	20	μA
Input noise voltage	BW = 1kHz to 10MHz		12			12		μVrms
Input voltage range		±1.0			±1.0			V
Common mode								
Rejection ratio								
Gain 2	VCM = ±V,f ≤ 100kHz	60	86		60	86		dB
Gain 2	VCM = ±1V,F = 5MHz		60			60		dB
Supply voltage								
Rejection ratio								
Gain 2	ΔV_S = ±0.5V	50	70		50	70		dB
Output offset voltage								
Gain 1[1]	R_L = ∞		0.6	1.5		0.6	1.5	V
Gain 2 and 3[2,3]			0.35	1.5		0.35	1.0	V
Output common mode voltage	R_L= ∞	2.4	2.9	3.4	2.4	2.9	3.4	V
Output voltage swing, differential	R_L = 2k	3.0	4.0		3.0	4.0		
Output sink current		2.5	3.6		2.5	3.6		mA
Output resistance			20			20		Ω
Power supply current	R_L ± ∞		18	24		18	24	mA

NOTES

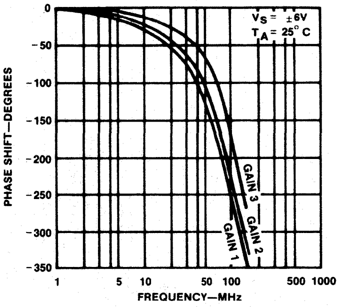
1. Gain select pins G_{1A} and G_{1B} connected together.
2. Gain select pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.

TYPICAL PERFORMANCE CHARACTERISTICS

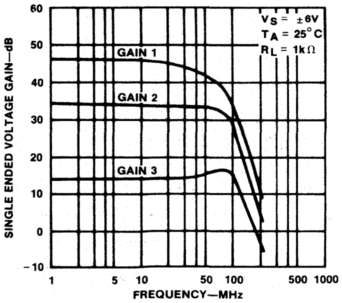
PHASE SHIFT AS A FUNCTION OF FREQUENCY



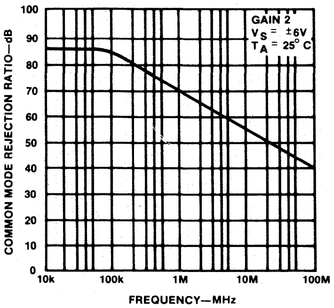
PHASE SHIFT AS A FUNCTION OF FREQUENCY



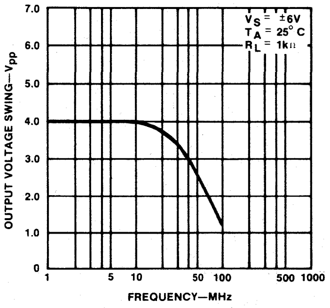
VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



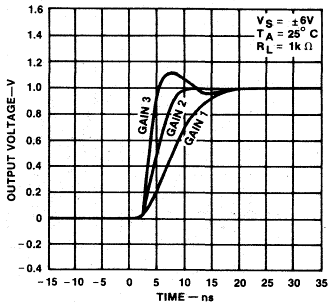
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



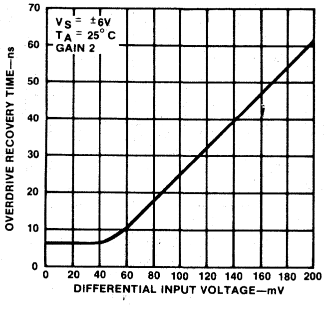
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



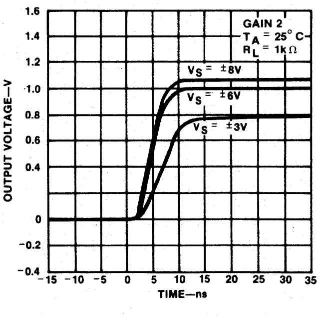
PULSE RESPONSE



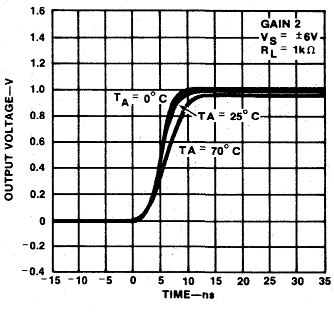
DIFFERENTIAL OVERDRIVE RECOVERY TIME



PULSE RESPONSE AS A FUNCTION OF SUPPLY VOLTAGE



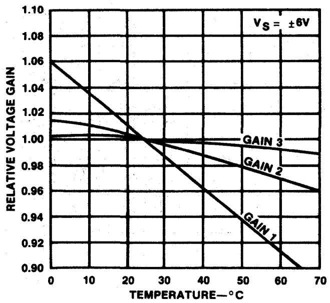
PULSE RESPONSE AS A FUNCTION OF TEMPERATURE



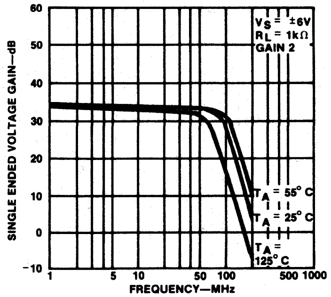
DIFFERENTIAL VIDEO AMPLIFIER μA733/733C

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

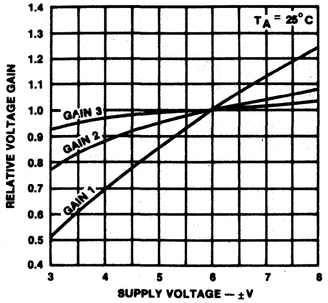
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



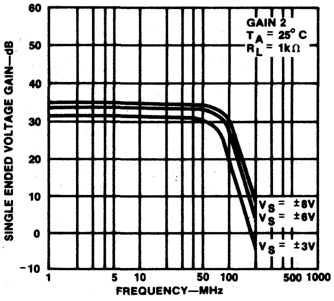
GAIN vs FREQUENCY AS A FUNCTION OF TEMPERATURE



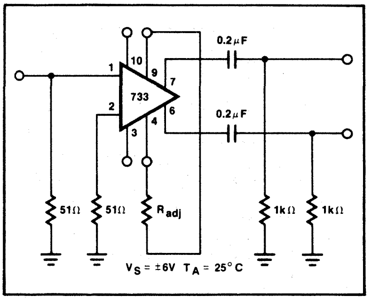
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



GAIN vs FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE

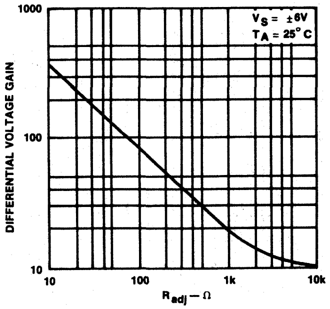


VOLTAGE GAIN ADJUST CIRCUIT

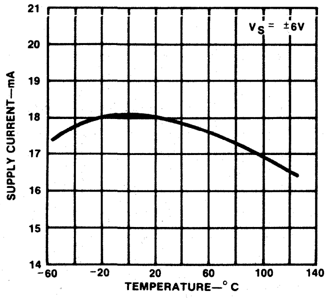


(Pin numbers apply to K Package)

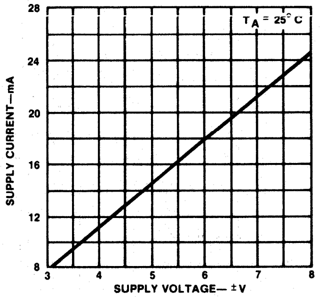
VOLTAGE GAIN AS A FUNCTION OF RADJ (FIGURE 3)



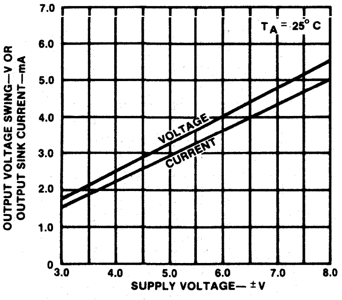
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

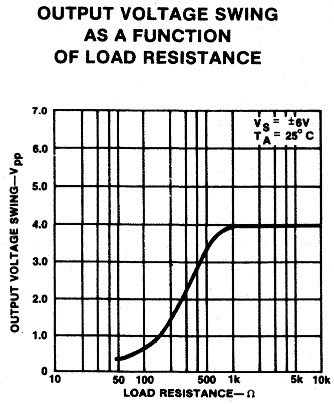


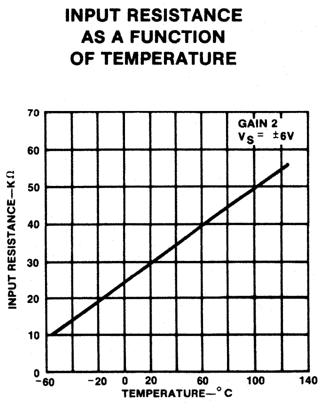
OUTPUT VOLTAGE AND CURRENT SWING AS A FUNCTION OF SUPPLY VOLTAGE

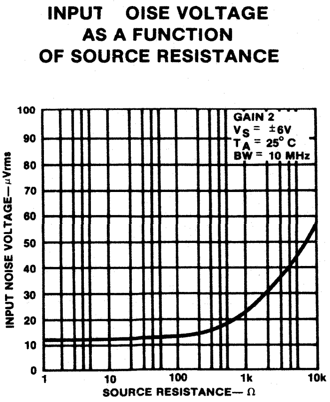


DIFFERENTIAL VIDEO AMPLIFIER μA733/733C

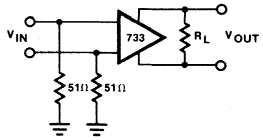
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

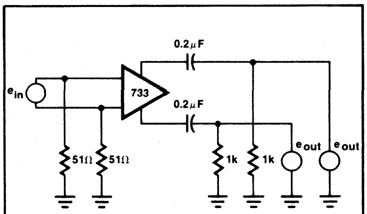

OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE


INPUT RESISTANCE AS A FUNCTION OF TEMPERATURE


INPUT OISE VOLTAGE AS A FUNCTION OF SOURCE RESISTANCE

TEST CIRCUITS T_A = 25°C unless otherwise specified.





Section 5
Timers

INDEX

Section 5 — Timers

TIMER NE/SE555/SE555C

DESCRIPTION

The 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA.

FEATURES

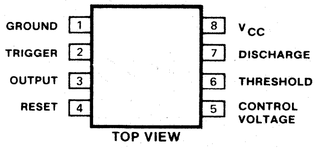
- **Turn off time less than 2μs**
- **Maximum operating frequency greater than 500kHz**
- **Timing from microseconds to hours**
- **Operates in both astable and monostable modes**
- **High output current**
- **Adjustable duty cycle**
- **TTL compatible**
- **Temperature stability of 0.005% per °C**

APPLICATIONS

- **Precision timing**
- **Pulse generation**
- **Sequential timing**
- **Time delay generation**
- **Pulse width modulation**
- **Pulse position modulation**
- **Missing pulse detector**

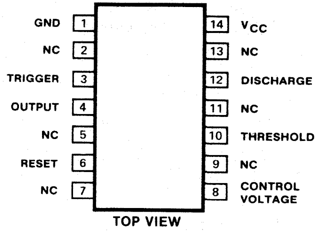
PIN CONFIGURATIONS

D, N, FE PACKAGE



ORDER NUMBERS
NE/SE555N,FE NE555D
SE555CN,CFE

F PACKAGE

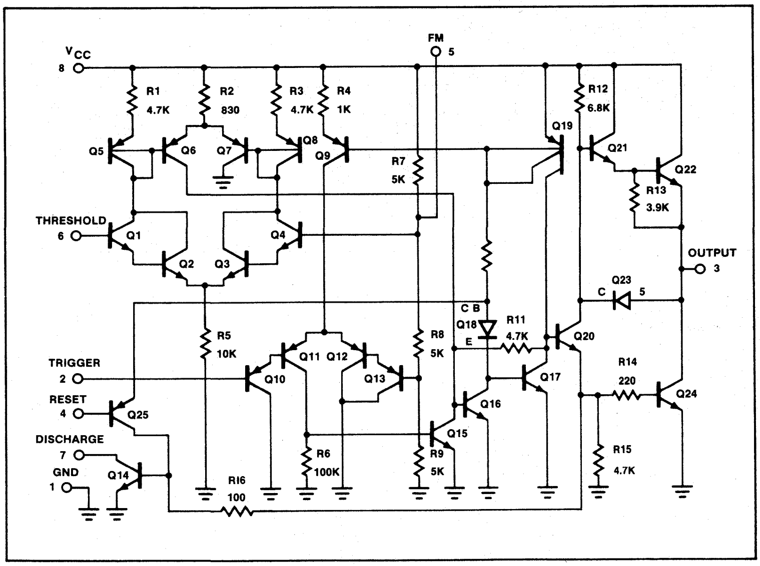


ORDER NUMBERS
NE/SE555F SE555CF

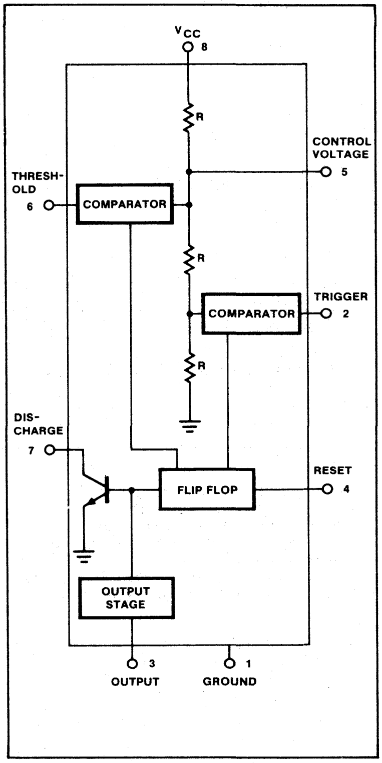
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
SE555	+18	V
NE555, SE555C,	+16	V
Power dissipation	600	mW
Operating temperature range		
NE555	0 to +70	°C
SE555, SE555C	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	300	°C

EQUIVALENT SCHEMATIC



BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = +5V to +15 unless otherwise specified.

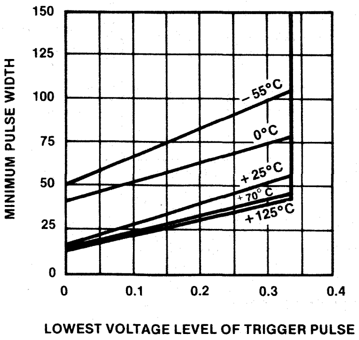
PARAMETER	TEST CONDITIONS	SE555			NE555/SE555C			UNIT
		Min	Typ	Max	Min	Typ	Max	
Supply voltage		4.5		18	4.5		16	V
Supply current (low state)[1]	V_{CC} = 5V $R_L = \infty$		3	5		3	6	mA
	V_{CC} = 15V $R_L = \infty$		10	12		10	15	mA
Timing error (monostable)	R_A = 2KΩ to 100KΩ							
Initial accuracy[2]	C = 0.1μF		0.5	2.0		1.0	3.0	%
Drift with temperature			30	100		50		ppm/°C
Drift with supply voltage			0.05	0.2		0.1	0.5	%/V
Timing error (astable)	R_A, R_B = 1kΩ to 100kΩ							
Initial accuracy[2]	C = 0.1μF		1.5			2.25		%
Drift with temperature	V_{CC} = 15V		90			150		ppm/°C
Drift with supply voltage			0.15			0.3		%/V
Control voltage level	V_{CC} = 15V	9.6	10.0	10.4	9.0	10.0	11.0	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4.0	V
Threshold voltage	V_{CC} = 15V	9.4	10.0	10.6	8.8	10.0	11.2	V
	V_{CC} = 5V	2.7	3.33	4.0	2.4	3.33	4.2	V
Threshold current[3]			0.1	0.25		0.1	0.25	μA
Trigger voltage	V_{CC} = 15V	4.8	5.0	5.2	4.5	5.0	5.6	V
	V_{CC} = 5V	1.45	1.67	1.9	1.1	1.67	2.2	V
Trigger current	V_{TRIG} = 0V		0.5	0.9		0.5	2.0	μA
Reset voltage[4]		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset current			0.1	0.4		0.1	0.4	mA
Reset current	V_{RESET} = 0V		0.4	1.0		0.4	1.5	mA
Output voltage (low)	V_{CC} = 15V							
	I_{SINK} = 10mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100mA		2.0	2.2		2.0	2.5	V
	I_{SINK} = 200mA		2.5			2.5		V
	V_{CC} = 5V							
	I_{SINK} = 8mA		0.1	0.25		0.3	0.4	V
	I_{SINK} = 5mA		0.05	0.2		0.25	0.35	V
Output voltage (high)	V_{CC} = 15V							
	I_{SOURCE} = 200mA		12.5			12.5		V
	I_{SOURCE} = 100mA	13.0	13.3		12.75	13.3		V
	V_{CC} = 5V							
	I_{SOURCE} = 100mA	3.0	3.3		2.75	3.3		V
Turn off time[5]	V_{RESET} = V_{CC}		0.5	2.0		0.5		μs
Rise time of output			100	200		100	300	ns
Fall time of output			100	200		100	300	ns
Discharge leakage current			20	100		20	100	na

NOTES

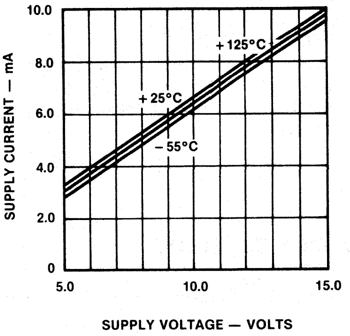
1. Supply current when output high typically 1mA less.
2. Tested at V_{CC} = 5V and V_{CC} = 15V.
3. This will determine the maximum value of $R_A + R_B$, for 15V operation, the max total R = 10 megohm, and for 5V operation, the max total R = 3.4 megohm.
4. Specified with trigger input high.
5. Time measured from a positive going input pulse from 0 to 0.8 x V_{CC} into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

TYPICAL PERFORMANCE CHARACTERISTICS

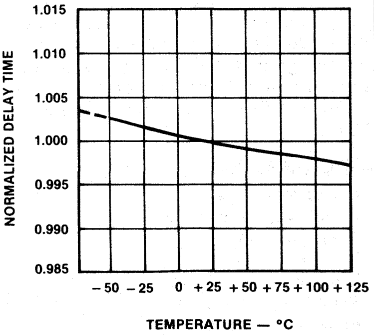
MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



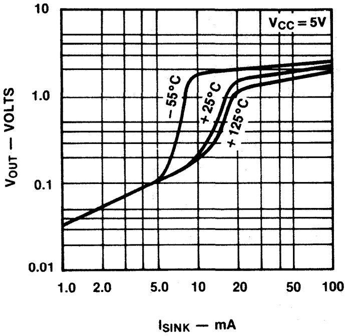
SUPPLY CURRENT vs SUPPLY VOLTAGE



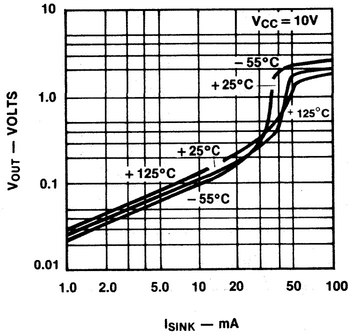
DELAY TIME vs TEMPERATURE



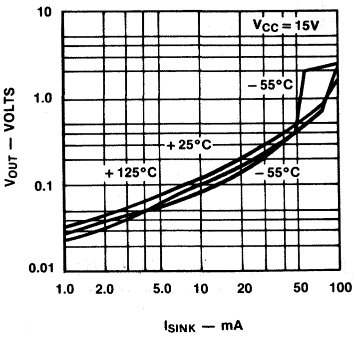
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



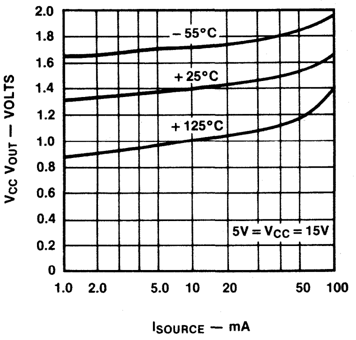
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



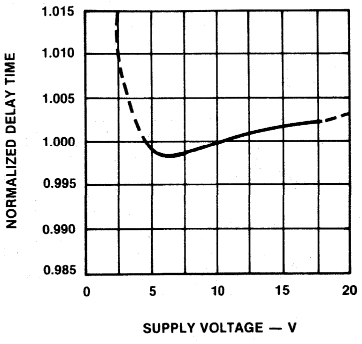
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



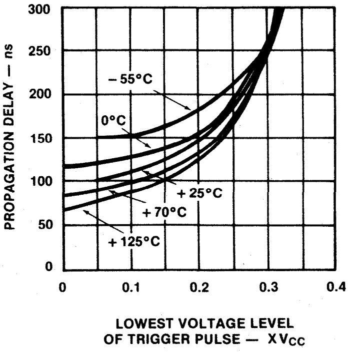
HIGH OUTPUT VOLTAGE DROP vs OUTPUT SOURCE CURRENT



DELAY TIME vs SUPPLY VOLTAGE



PROPAGATION DELAY vs VOLTAGE LEVEL OF TRIGGER PULSE



DUAL TIMER

NE/SA/SE556

DESCRIPTION

The 556 Dual Monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. The 556 is a dual 555. Timing is provided by an external resistor and capacitor for each timing function. The two timers operate independently of each other sharing only V_{CC} and ground. The circuits may be triggered and reset on falling waveforms. The output structures may sink or source 200mA.

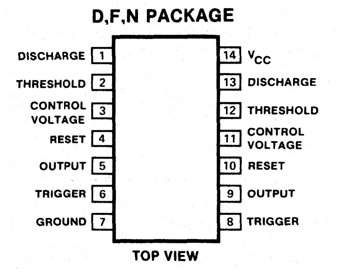
APPLICATIONS

- **Precision timing**
- **Sequential timing**
- **Pulse shaping**
- **Pulse generator**
- **Missing pulse detector**
- **Tone burst generator**
- **Pulse width modulation**
- **Time delay generator**
- **Frequency division**
- **Industrial controls**
- **Pulse position modulation**
- **Appliance timing**
- **Traffic light control**
- **Touch tone encoder**

FEATURES

- **Timing from microseconds to hours**
- **Replaces two 555 timers**
- **Operates in both astable and monostable modes**
- **High output current**
- **Adjustable duty cycle**
- **TTL compatible**
- **Temperature stability of 0.005% per °C**
- **SE566 MIL STD 883A, B, C available, N38510 (JAN planned, 38510 processing available).**

PIN CONFIGURATION

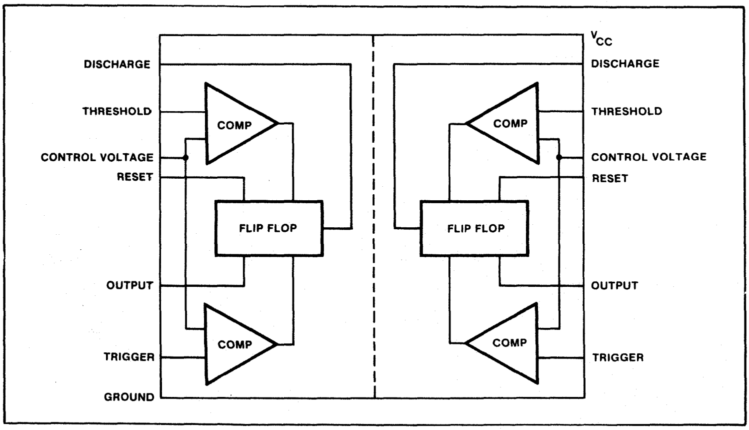


ORDER NUMBERS

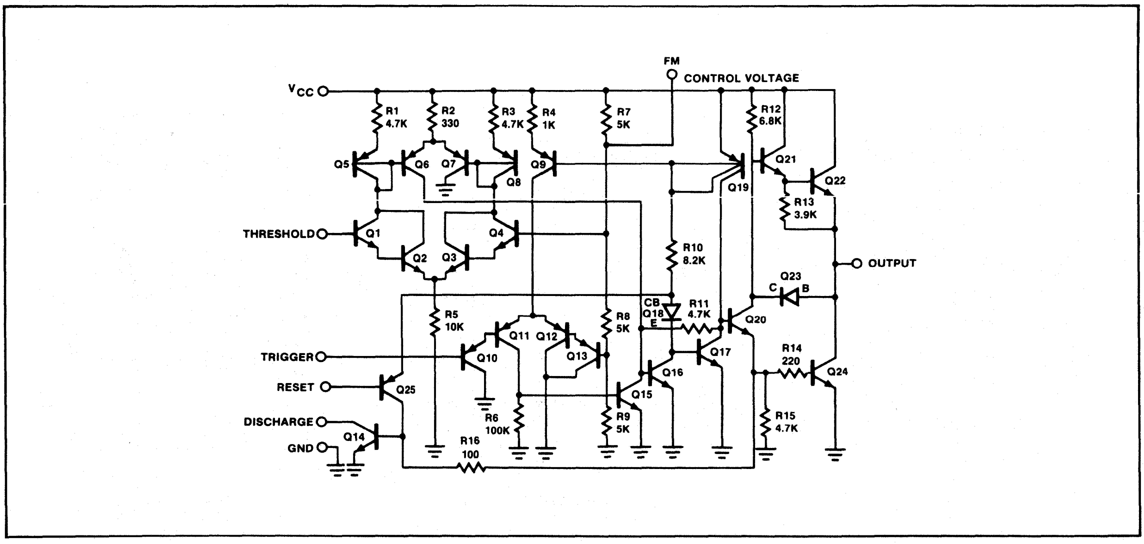
NE/SE556F,N NE556D

SA556N SE556CN

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC (Shown for one circuit only)



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
NE/SA556, SE556C	+16	V
SE556	+18	V
Power dissipation	600	mW
Operating temperature range		
NE556	0 to +70	°C
SA556	-40 to +85	°C
SE556, SE556C	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (Soldering, 60 sec)	+300	°C

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +5V to +15V unless otherwise specified.

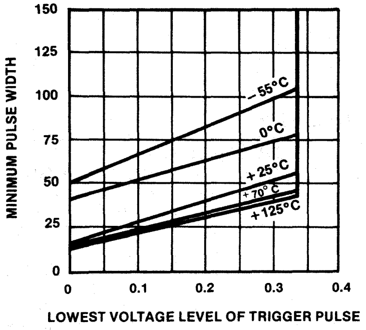
PARAMETER	TEST CONDITIONS	SE556			NE/SA556/SE556C			UNITS
		Min	Typ	Max	Min	Typ	Max	
Supply voltage		4.5		18	4.5		16	V
Supply current (low state)[1]	V_{CC} = 5V R_L = ∞		6	10		6	12	mA
	V_{CC} = 15V R_L = ∞		20	24		20	30	mA
Timing error (monostable)	R_A = 2kΩ to 100kΩ							
Initial accuracy[2]	C = 0.1μF		0.5	1.5		0.75	3.0	%
Drift with temperature			30	100		50		ppm/°C
Drift with supply voltage			0.05	0.2		0.1	0.5	%/V
Timing error (astable)	R_A, R_B = 1kΩ to 100kΩ							
Initial accuracy[2]	C = 0.1μF		1.5			2.25		%
Drift with temperature	V_{CC} = 15V		90			150		ppm/°C
Drift with supply voltage			0.15			0.3		%/V
Control voltage level	V_{CC} = 15V	9.6	10.0	10.4	9.0	10.0	11.0	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4.0	V
Threshold voltage	V_{CC} = 15V	9.4	10.0	10.6	8.8	10.0	11.2	V
	V_{CC} = 5V	2.7	3.33	4.0	2.4	3.33	4.2	V
Threshold current[3]			30	250		30	250	nA
Trigger voltage	V_{CC} = 15V	4.8	5.0	5.2	4.5	5.0	5.6	V
	V_{CC} = 5V	1.45	1.67	1.9	1.1	1.67	2.2	V
Trigger current	V_{TRIG} = 0V		0.5	0.9		0.5	2.0	μA
Reset voltage[5]		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset current			0.1	0.4		0.1	0.6	mA
Reset current	V_{RESET} = 0V		0.4	1.0		0.4	1.5	mA
Output voltage (low)	V_{CC} = 15V							
	I_{SINK} = 10mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100mA		2.0	2.25		2.0	3.2	V
	I_{SINK} = 200mA		2.5			2.5		V
	V_{CC} = 5V							
	I_{SINK} = 8mA		0.1	0.2		0.25	0.3	V
	I_{SINK} = 5mA		0.05	0.15		0.15	0.25	V
Output voltage (high)	V_{CC} = 15V							
	I_{SOURCE} = 200mA		12.5			12.5		V
	I_{SOURCE} = 100mA	13.0	13.3		12.75	13.3		V
	V_{CC} = 5V							
	I_{SOURCE} = 100mA	3.0	3.3		2.75	3.3		V
Rise time of output			100	200		100	300	ns
Fall time of output			100	200		100	300	ns
Discharge leakage current			20	100		20	100	nA
Matching characteristics[4]								
Initial accuracy[2]			0.5	1.0		1.0	2.0	%
Drift with temperature			10			10		ppm/°C
Drift with supply voltage			0.1	0.2		0.2	0.5	%/V

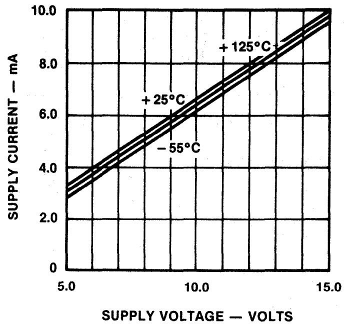
NOTES See following page

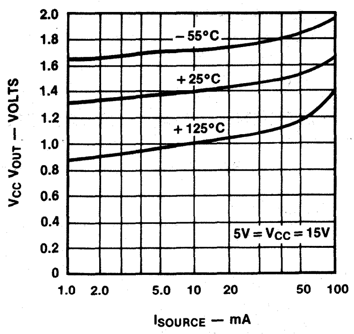
NOTES

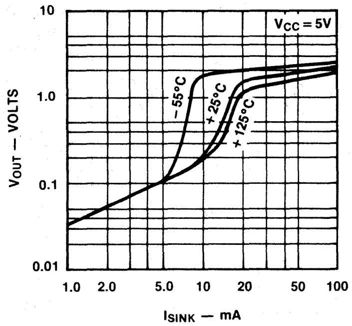
1. Supply current when output is high is typically 1.0mA less.
2. Tested at V_{CC} = 5V and V_{CC} = 15V.
3. This will determine the maximum value of $R_A + R_B$. For 15V operation, the maximum total R = 10 meg-ohms, and for 5V operation, the max. total R = 3.4 meg-ohms.
4. Matching charactristics refer to the difference between performance characteristics for each timer section in the monostable mode.
5. Specified with trigger input high.

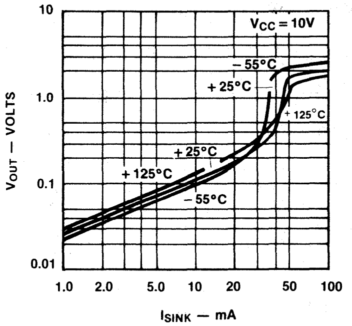
TYPICAL PERFORMANCE CHARACTERISTICS

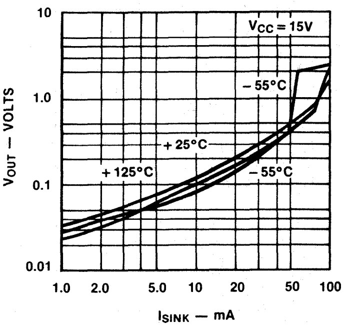

MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING

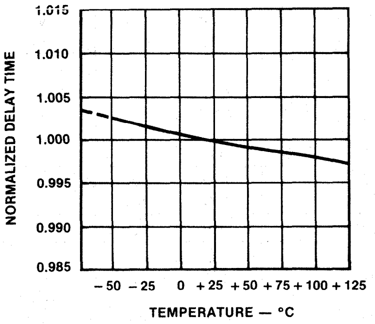

SUPPLY CURRENT vs SUPPLY VOLTAGE

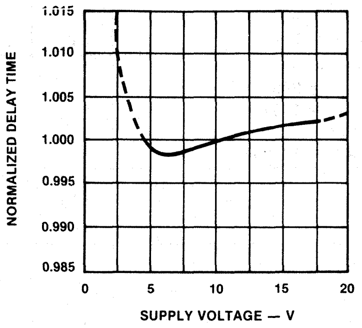

HIGH OUTPUT VOLTAGE DROP vs OUTPUT SOURCE CURRENT

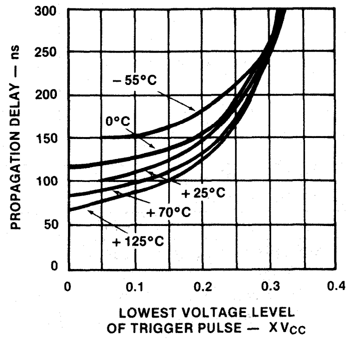

LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT


LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT


LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT


DELAY TIME vs TEMPERATURE


DELAY TIME vs SUPPLY VOLTAGE


PROPAGATION DELAY vs VOLTAGE LEVEL OF TRIGGER PULSE

DUAL TIMER NE/SA/SE556-1/SE556-1C

DESCRIPTION

The 556-1 Dual Monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. The 556-1 is a dual 555. Timing is provided by an external resistor and capacitor for each timing function. The two timers operate independently of each other sharing only V_{CC} and ground. The circuits may be triggered and reset on falling waveforms. The output structures may sink or source 200mA.

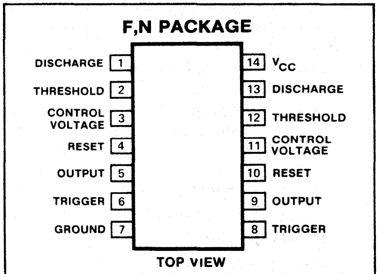
APPLICATIONS

- **Precision timing**
- **Sequential timing**
- **Pulse shaping**
- **Pulse generator**
- **Missing pulse detector**
- **Tone burst generator**
- **Pulse width modulation**
- **Time delay generator**
- **Frequency division**
- **Industrial controls**
- **Pulse position modulation**
- **Appliance timing**
- **Traffic light control**
- **Touch tone encoder**

FEATURES

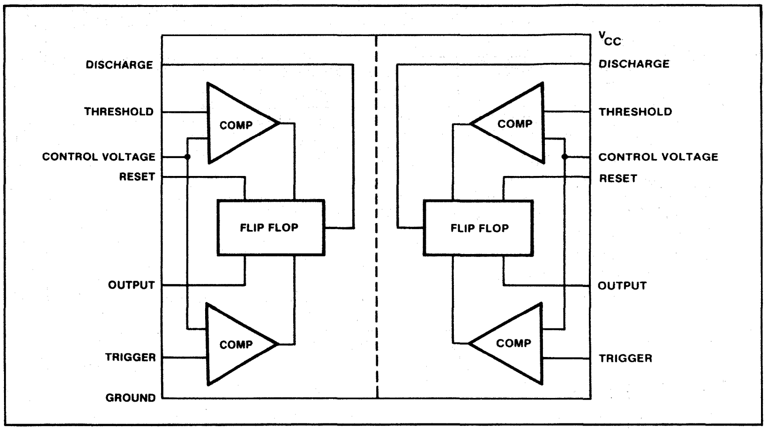
- **Turn off time less than 2μS**
- **Maximum operating frequency greater than 500kHz**
- **Timing from microseconds to hours**
- **Replaces two 555 timers**
- **Operates in both astable and monostable modes**
- **High output current**
- **Adjustable duty cycle**
- **TTL compatible**
- **Temperature stability of 0.005% per °C**

PIN CONFIGURATION

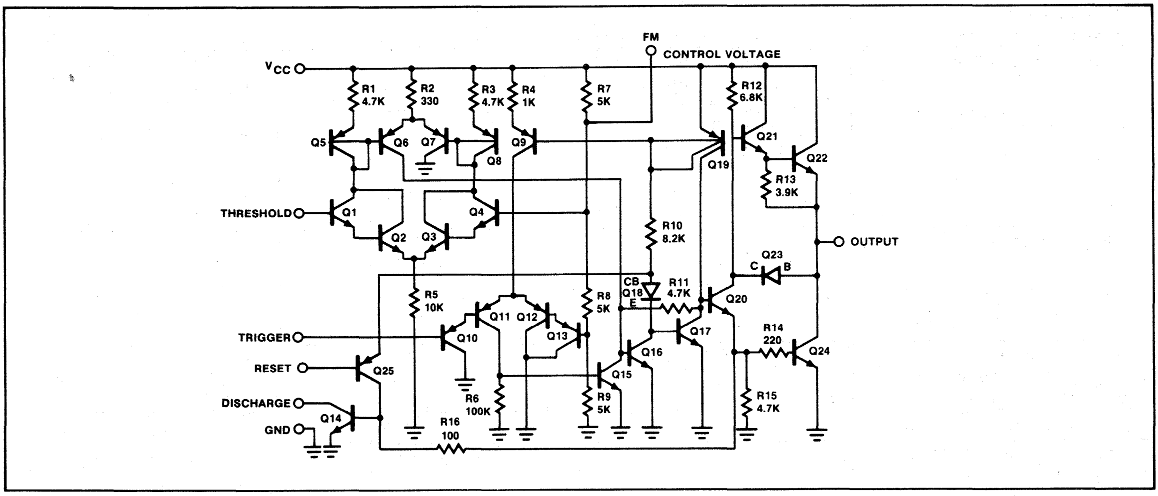


ORDER NUMBERS
NE/SA/SE556-1F,N SE556-1CF,CN

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC (Shown for one circuit only)



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
NE/SA556-1, SE556-1C	+16	V
SE556-1	+18	V
Power dissipation	1.20	W
Operating temperature range		
NE/SA556-1	0 to +70	°C
SA556-1	-40 to +85	°C
SE556-1, SE556-1C	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60 sec)	+300	°C

ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, V_{CC} = +5V to +15V unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE556-1			NE556-1/SE556-1C			UNITS
		Min	Typ	Max	Min	Typ	Max	
Supply voltage		4.5		18	4.5		16	V
Supply current (low state)[1]	V_{CC} = 5V $R_L = \infty$		6	10		6	12	mA
	V_{CC} = 15V $R_L = \infty$		20	24		20	30	mA
Timing error (monostable)	R_A = 2kΩ to 100kΩ							
Initial accuracy[2]	C = 0.1μF		0.5	1.5		0.75	3.0	%
Drift with temperature			30	100		50		ppm/°C
Drift with supply voltage			0.05	0.2		0.1	0.5	%/V
Timing error (astable)	R_A, R_B = 1kΩ to 100kΩ							
Initial accuracy[2]	C = 0.1μF		1.5			2.25		%
Drift with temperature	V_{CC} = 15V		90			150		ppm/°C
Drift with supply voltage			0.15			0.3		%/V
Control voltage level	V_{CC} = 15V	9.6	10.0	10.4	9.0	10.0	11.0	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4 0	V
Threshold voltage	V_{CC} = 15V	9.4	10.0	10.6	8.8	10.0	11.2	V
	V_{CC} = 5V	2.7	3.33	4.0	2.4	3.33	4.2	V
Threshold current[3]			30	250		30	250	nA
Trigger voltage	V_{CC} = 15V	4.8	5.0	5.2	4.5	5.0	5.6	V
	V_{CC} = 5V	1.45	1.67	1.9	1.1	1.67	2.2	V
Trigger current	V_{TRIG} = 0V		0.5	0.9		0.5	2.0	μA
Reset voltage[5]		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset current			0.1	0.4		0.1	0.6	mA
Reset current	V_{RESET} = 0V		0.4	1.0		0.4	1.5	mA
Output voltage (low)	V_{CC} = 15V							
	I_{SINK} = 10mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100mA		0.8	1.2		2.0	2.5	V
	I_{SINK} = 200mA		2.5			2.5		V
	V_{CC} = 5V							
	I_{SINK} = 8mA		0.1	0.2		0.25	0.3	V
	I_{SINK} = 5mA		0.05	0.15		0.15	0.25	V
Output voltage (high)	V_{CC} = 15V							
	I_{SOURCE} = 200mA		12.5			12.5		V
	I_{SOURCE} = 100mA	13.0	13.3		12.75	13.3		V
	V_{CC} = 5V							
	I_{SOURCE} = 100mA	3.0	3.3		2.75	3.3		V
Turn off time[6]	V_{RESET} = V_{CC}		0.5	2.0		0.5		μs
Rise time of output			100	200		100	300	ns
Fall time of output			100	200		100	300	ns
Discharge leakage current			20	100		20	100	nA
Matching characteristics[4]								
Initial accuracy[2]			0.5	1.0		1.0	2.0	%
Drift with temperature			±10			±10		ppm/°C
Drift with supply voltage			0.1	0.2		0.2	0.5	%/V

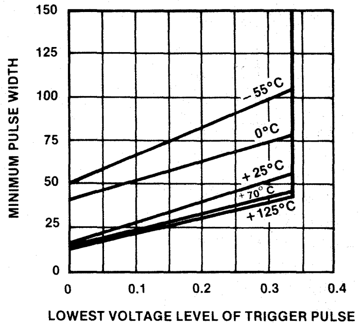
NOTES
See following page

NOTES

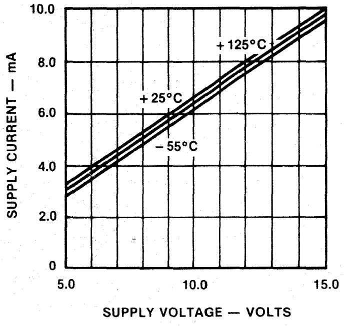
1. Supply current when output is high is typically 1.0mA less.
2. Tested at V_{CC} = 5V and V_{CC} = 15V.
3. This will determine the maximum value of $R_A + R_B$. For 15V operation, the maximum total R = 10 megohms, and for 5V operation, the max. total R = 3.4 megohms.
4. Matching characteristics refer to the difference between performance characteristics for each timer section in the monostable mode.
5. Specified with trigger input high.
6. Time measured from a positive going input pulse from 0 to 0.8 V_{CC} into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

TYPICAL CHARACTERISTICS

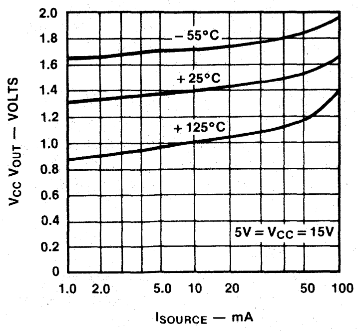
MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



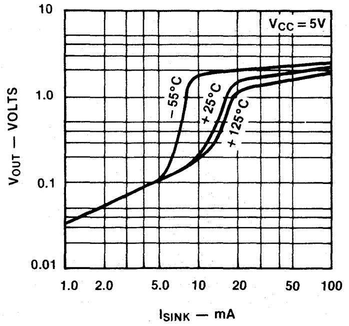
SUPPLY CURRENT vs SUPPLY VOLTAGE



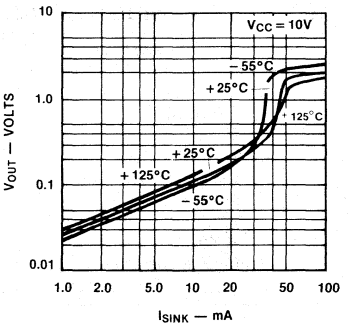
HIGH OUTPUT VOLTAGE DROP vs OUTPUT SOURCE CURRENT



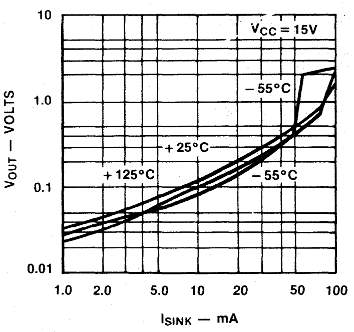
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



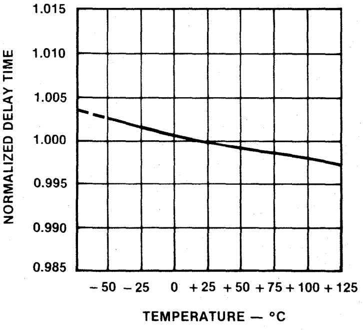
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



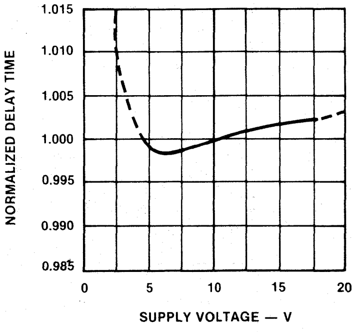
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



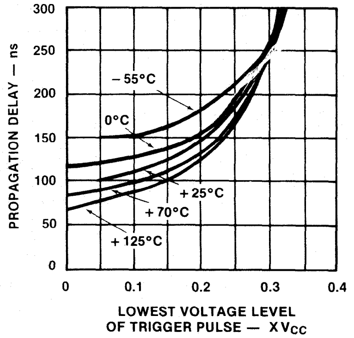
DELAY TIME vs TEMPERATURE



DELAY TIME vs SUPPLY VOLTAGE



PROPAGATION DELAY vs VOLTAGE LEVEL OF TRIGGER PULSE



QUAD TIMER NE/SA/SE558

DESCRIPTION

The 558 Quad Timers are monolithic timing devices which can be used to produce four entirely independent timing functions. The 558 output sinks current. These highly stable, general purpose controllers can be used in a monostable mode to produce accurate time delays, from microseconds to hours. In the time delay mode of operation, the time is precisely controlled by one external resistor and one capacitor. A stable operation can be achieved by using two of the four timer sections.

The four timing sections in the 558 are edge triggered; therefore, when connected in tandem for sequential timing applications, no coupling capacitors are required. Output current capability of 100mA is provided in both devices.

FEATURES

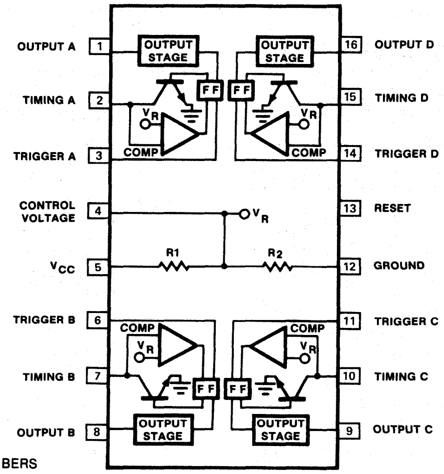
- **100mA output current per section**
- **Edge triggered (no coupling capacitor)**
- **Output independent of trigger conditions**
- **Wide supply voltage range 4.5V to 18V**
- **Timer intervals from microseconds to hours**
- **Time period equals RC**
- **Military qualifications pending**

APPLICATIONS

- **Sequential timing**
- **Time delay generation**
- **Precision timing**
- **Industrial controls**
- **Quad one-shot**

PIN CONFIGURATION

F,N PACKAGE



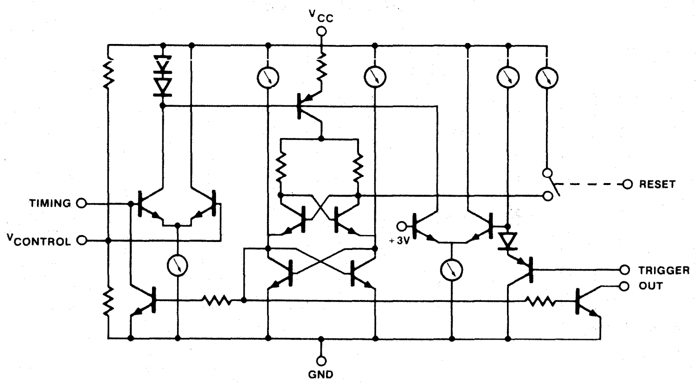
ORDER NUMBERS
NE/SA/SE558F NE/SA/SE558N

TOP VIEW

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
NE/SA558	+16	V
SE558	+18	V
Power dissipation	1.25	W
Operating temperature range		
NE558	0 to +70	°C
SA558	-40 to +85	°C
SE558	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	+300	°C

558 EQUIVALENT CIRCUIT



QUAD TIMER

NE/SA/SE558

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = +5V$ to $+15V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE558			NE/SA558			UNIT
		Min	Typ	Max	Min	Typ	Max	
Supply voltage		4.5		18	4.5		16	V
Supply current	V_{CC} = Reset = 15V		21	32		27	36	mA
Timing accuracy (T = RC)	R = 2kΩ to 100kΩ C = 1μF							
Initial accuracy			1.0	3		2		%
Drift with temperature			150			150		ppm/°C
Drift with supply voltage			0.1			0.1		%/V
Trigger voltage[1]	V_{CC} = 15V	0.8	1.5	2.4	0.8	1.5	2.4	V
Trigger current	Trigger = 0V		5	30		5	100	μA
Reset voltage[2]		0.8	1.5	2.4	0.8	1.5	2.4	V
Reset current	Reset		50	300		50		μA
Threshold voltage			0.63			0.63		xV_{CC}
Threshold leakage			15			15		nA
Output voltage[3]	I_L = 10mA		0.1	0.2		0.1	0.4	V
	I_L = 100mA		0.7	1.5		1.0	2.0	V
Output leakage			10			10		nA
Propagation delay			1.0			1.0		μs
Risetime of output	I_L = 100mA		100			100		ns
Falltime of output	I_L = 100mA		100			100		ns

NOTES

1. The trigger functions only on the falling edge of the trigger pulse only after previously being high. After reset the trigger must be brought high and then low to implement triggering.
2. For reset below 0.8 volts, outputs set low and trigger inhibited. For reset above 2.4 volts, trigger enabled.
3. The 558 output structure is open collector which requires a pull up resistor to V_{CC} to sink current. The output is normally low sinking current.

Section 6
Power Controllers

INDEX

Section 6 — Power Controllers

VOLTAGE REGULATOR—SYMBOLS AND DEFINITIONS

T_A

Ambient temperature range. Range of the surrounding environment of the operating device.

T_J

Junction Temperature. The maximum temperature of the device. 150°C is standard for silicon devices.

T_{STG}

Storage temperature range. Temperature range that the device can be stored in a non-operating condition.

T_{SOLD}

Soldering Temperature. The temperature which can be applied to the lead frame of the device for short periods of time (normally specified for a duration of 10 sec).

Truth Tables

0 is logic level low
1 is logic level high
X - don't care condition - has no effect under circuit conditions listed.

Absolute Maximum Rating

Operating safe zones exceeding these limits could cause permanent damage to the device and are not meant to imply that devices can operate at these limits.

Power Dissipation

The power that the device can safely handle at 25°C. The dissipation must be derated as indicated for the individual package type.

Package Type Designation

See full package designations in Appendix.

V_{CC} ($-V_{CC}$)

Supply Voltage. The range of power supply voltage over which the device will operate safely.

Line Regulation

Sometimes referred to as "static regulation". This term refers to the changes in the output as the input is varied slowly from its rated minimum value to its rated maximum value (from 105 VAC_{RMS} to 125 VAC_{RMS}). Measured in mv/V.

Load Regulation

Sometimes referred to as "dynamic regulation". This term refers to the changes in the output when load conditions are suddenly changed (from no load to full load). Measured in mv/V.

Thermal Regulation

Referred to as changes due to ambient variations or thermal drift. Also referred to as temperature coefficient, measured in ppm/°C or mv/°C.

Transient Response

The ability of a regulator to respond to rapid changes in line variations, load variations, or intermittent transient input conditions. (Transient Response is often referred to as "recovery time"). Measured in milliseconds (ms).

Voltage Limiting

The ability of the regulator to "shut down" in the event that the internal reference sources fail to function properly. Measured in Volts.

Current Limiting

The ability of the amplified segment to limit the output current of the device when safe operating limits are exceeded. Measured in amperes (pre-determined).

Thermal Shutdown

The ability of the regulator to shut itself down when the maximum die temperature is exceeded. Measured in degrees Celsius (C).

Power Dissipation

The ability of the regulator to tolerate excessively high levels of input power while maintaining its operation within the safe operating area of its active devices. Measured in watts.

Efficiency

Regarding a regulator, the ratio of the total power input to the usable power output. Expressed as a percentage. (For example, if a regulator has a 50 watt input and a 40 watt output, its efficiency is 80 percent).

EMI/RFI

("Electromagnetic Interference/Radio Frequency Interference") regarding regulators, magnetic field disturbance and radio frequency interference signals generated especially by SMPS devices. Measurement is generally unspecified.

Safe Operating Area Restriction (SOAR)

Limits the output current of the amplifier to maintain safe (no thermal runaway) operating conditions. (Accomplished through internal sensor amplifiers).

NOTE
Refer to Section 4 of Analog Applications Manual for an in-depth explanation of Voltage Regulators

SWITCHED-MODE POWER SUPPLY CONTROL CIRCUIT NE/SE5560

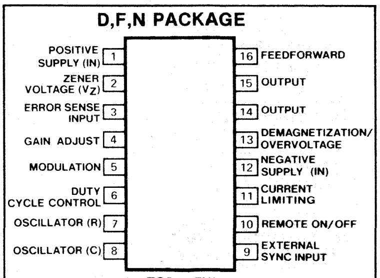
DESCRIPTION

The NE/SE5560 is a control circuit for use in switched mode power supplies. This single monolithic chip incorporates all the control and housekeeping (protection) functions required in switched mode power supplies, including an internal temperature compensated reference source, internal Zener reference, sawtooth generator, pulse width modulator, output stage and various protection circuits.

FEATURES

- **Stabilized power supply**
- **Temperature compensated reference source**
- **Sawtooth generator**
- **Pulse width modulator**
- **Remote on/off switching**
- **Current limiting**
- **Low supply voltage protection**
- **Loop fault protection**
- **Demagnetization/overvoltage protection**
- **Maximum duty cycle adjustment**
- **Feed forward control**
- **External synchronization**

PIN CONFIGURATION



TOP VIEW

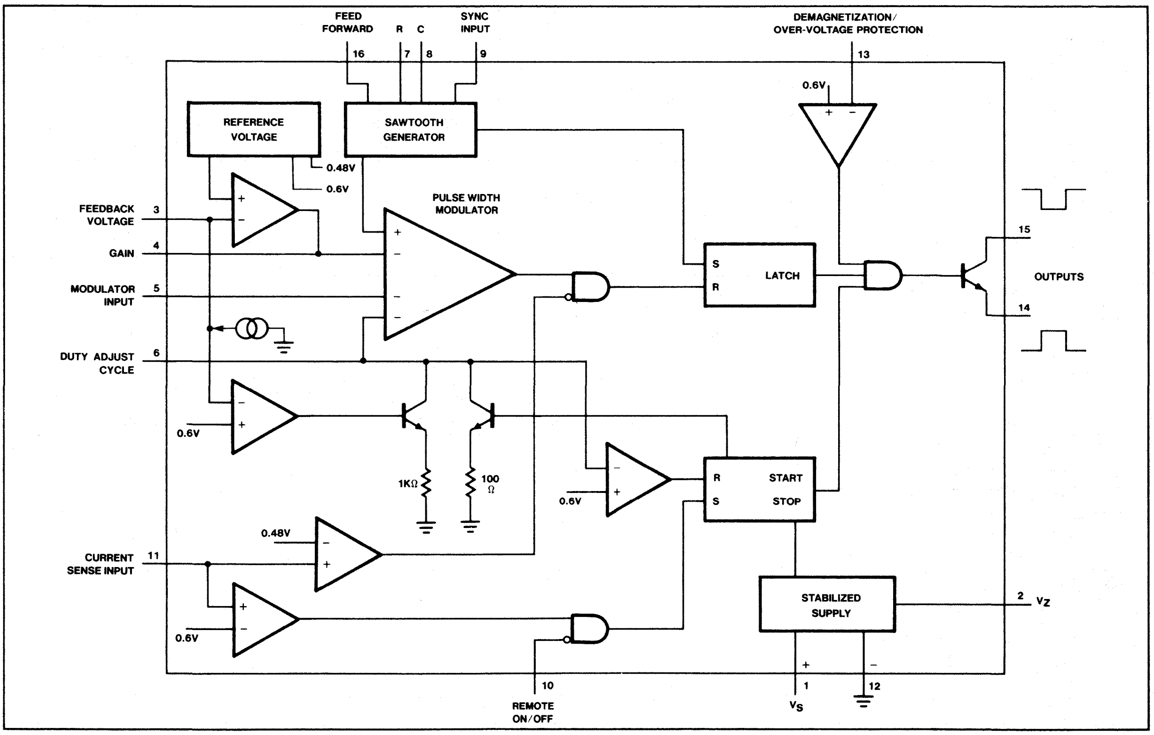
ORDER NUMBERS

NE5560N SE5560F
NE5560D SE5560N
NE5560F

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply		
Voltage sourced	+18	V
Current sourced	30	mA
Output transistor		
Output current	40	mA
Collector voltage (Pin 15)	+18	V
Max. emitter voltage (Pin 14)	+5	V
Operating temperature (ambient)		
SE5560	−55 to +125	°C
NE5560	0 to 70	°C
Storage temperature range	−65 to +150	°C

BLOCK DIAGRAM



SWITCHED-MODE POWER SUPPLY CONTROL CIRCUIT NE/SE5560

DC ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V_{CC} = 12V$ unless otherwise specified)

PARAMETER	TEST CONDITIONS	SE5560			NE5560			UNIT
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Sections	Over temp.	3.65		3.85	3.53		4.00	V
Internal reference voltage (V_{ref})	25°C	3.69	3.76	3.81	3.57	3.76	3.95	V
Internal Zener reference (V_Z)	$I_L = 7mA$	7.8	8.4	9.0	7.8	8.4	9.0	V
Oscillator Section								
Frequency range	Over temp.	50		100k	50		100k	Hz
Modulator								
Modulator input current	Voltage at Pin 5 = 1V over temp.		0.2	20		0.2	20	μA
Housekeeping Function								
*Pin 6, input current	Over temp.		0.2	20		0.2	20	μA
*Pin 6, duty cycle limit control	(for 50% maximum duty cycle) 15kHz to 50kHz/41% of V_Z	40	50	60	40	50	60	% of duty cycle
*Pin 1, low supply voltage protection thresholds		V_Z+ 0.2	V_Z+ 7V	V_Z+ 1.7V	V_Z+ 0.2	V_Z+ 7V	V_Z+ 1.7V	V
*Pin 3, feedback loop protection trip threshold		470	600	720	470	600	720	mV
*Pin 3, pull up current	Over temp.		−15	−35		−15	−35	μA
*Pin 13, demagnetization/over voltage protection trip on threshold		470	600	720	470	600	720	mA
*Pin 13, input current	25°C		0.6	10		0.6	10	μA
	Over temp.			20			20	μA
Pin 16, feed forward duty cycle² control	Voltage at Pin 16 = $2V_Z$		0.4			0.4		original duty cycle
*Pin 16, feed forward input current	25°C		0.2	5		0.2	5	μA
	Over temp.			10			10	μA
External Synchronization								
Pin 9 off		0		0.8	0		0.8	V
on		2		V_Z	2		V_Z	V
sink current	Voltage at Pin 9 = 0V, 25°C		−65	−100		−65	−125	μA
	Over temp.			−125			−125	μA
Remote								
*Pin 10 off		0	0.8		0	0.8		V
on		2	V_Z		2	V_Z		V
sink current	25°C		−85	−100		−85	−125	μA
	Over temp.			−125			−125	μA
Current Limiting								
*Pin 11, I_{IN}	Voltage at Pin 11 = 250mV, 25°C		−2	−10		−2	−10	μA
	Over temp.			−20			–	
Trip Levels:								
Shut down, slow start		0.560	0.600	0.700	0.560	0.600	0.700	V
Current limit		0.400	0.48	0.500	0.400	0.48	0.500	V
Error Amplifier								
Output voltage swing (maximum)		6.2			6.2			V
Output voltage swing (minimum)				0.7		0.7		V
Open loop gain			60			60		dB
Feedback resistor		10k		10k				Ω
Small signal bandwidth			3			3		MHz
Output Stage								
V_{CE}(SAT) $I_C = 40mA$				0.5		0.5		V
Output Current (Pin 15)		40			40			mA
Max emitter voltage (Pin 14)		5	6		5	6		V

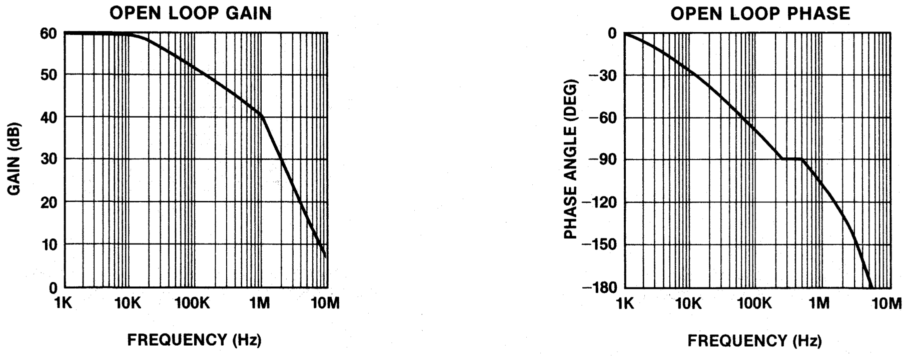
SWITCHED-MODE POWER SUPPLY CONTROL CIRCUIT NE/SE5560

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	TEST CONDITIONS	SE5560			NE5560			UNIT
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Voltage/Current								
I_{CC}	$I_Z = 0$, voltage fed, $V_{CC} = 12V$, 25°C			10			10	mA
	Over temp.			15			15	mA
V_{CC}	$I_{CC} = 10mA$, current feed	20		23	19		24	V
V_{CC}	$I_{CC} = 30mA$, current feed	20		30	20		30	V
Temperature coefficient of V_{ref}			+75			+75		ppm/°C
Temperature coefficient of V_Z			+150			+150		ppm/°C
Initial accuracy	R = 5kΩ		5			5		%
Duty cycle range[1]	fo = 20kHz	0		98	0		98	%
Single pulse inhibit delay	Inhibit delay time for 20% overdrive at 40mA I_{OUT}		0.7	0.8		0.7	0.8	μs

TYPICAL PERFORMANCE CHARACTERISTICS

ERROR AMPLIFIER



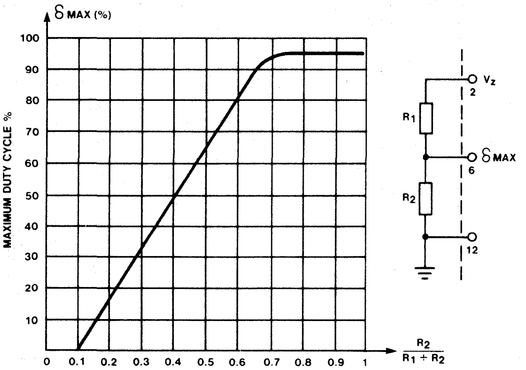
OPEN LOOP GAIN

OPEN LOOP PHASE

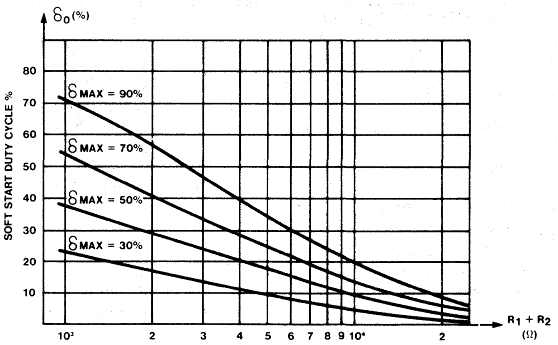
SWITCHED-MODE POWER SUPPLY CONTROL CIRCUIT NE/SE5560

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

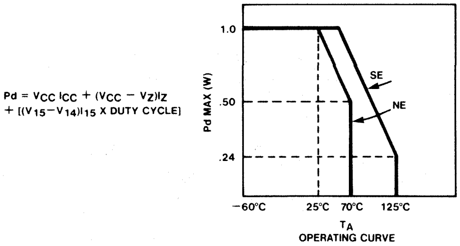
GRAPH FOR DETERMINING δ MAX



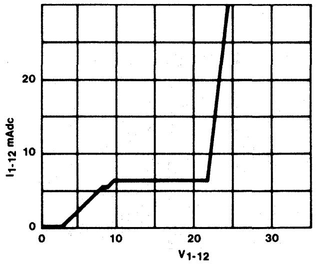
SOFT-START MIN DUTY CYCLE vs $R_1 + R_2$



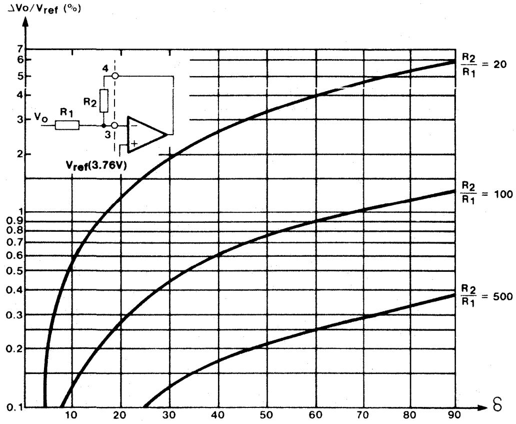
POWER DERATING CURVE



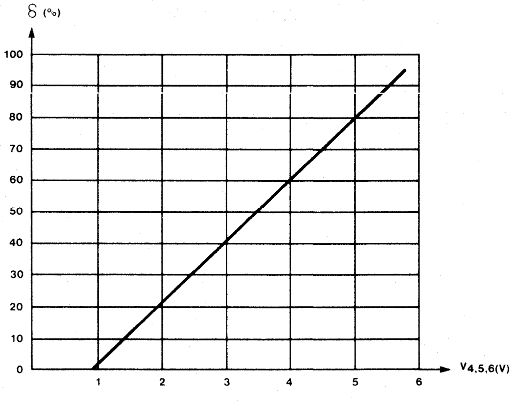
NE5560 VOLTAGE/CURRENT FED SUPPLY CHARACTERISTICS



REGULATION vs ERROR AMP CLOSED LOOP GAIN



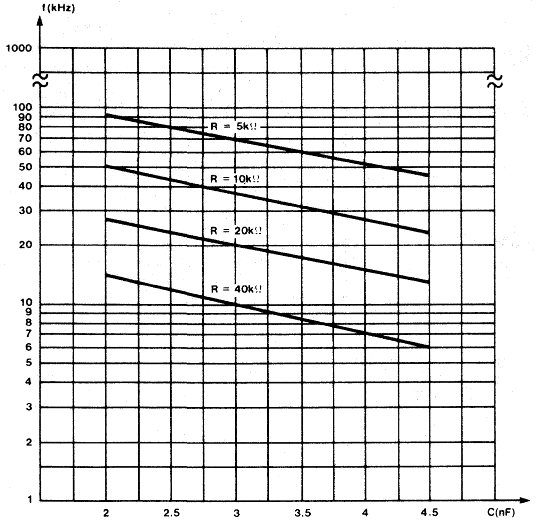
TRANSFER CURVE OF PULSE WIDTH MODULATOR DUTY CYCLE vs INPUT VOLTAGE



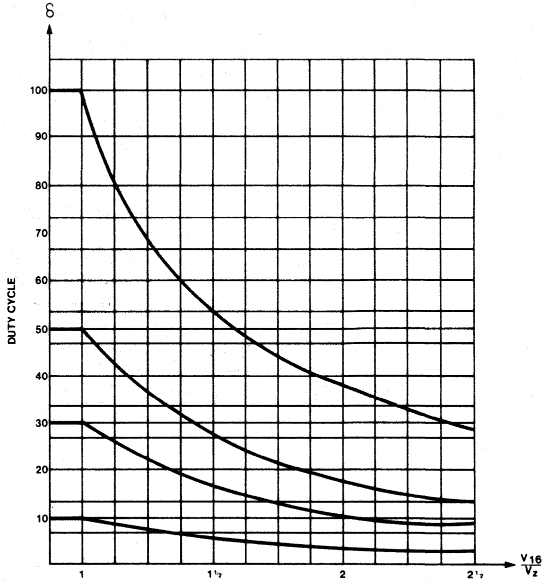
SWITCHED-MODE POWER SUPPLY CONTROL CIRCUIT NE/SE5560

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

TYPICAL FREQUENCY PLOT vs R_T AND C_T



DUTY CYCLE SENSITIVITY TO FEED FORWARD VOLTAGE (PIN 16)



DESCRIPTION of the NE5560 BLOCK DIAGRAM

The following functions are incorporated:

- A temperature compensated reference source.
- An error amplifier with pin 3 as input. The output is connected to pin 4 so that the gain is adjustable with external resistors.
- A sawtooth generator with a TTL-compatible synchronization input (pins 7,8,9).
- A pulse-width modulator with a duty-cycle range from 0 to 95%.

The PWM has two additional inputs:

Pin 6 can be used for a precise setting of δ max.

Pin 5 gives a direct access to the modulator, allowing for real constant current operation:

- A gate at the output of the PWM provides a simple dynamic current limit.
- A latch that is set by the flyback of the sawtooth and reset by the output pulse of the above-mentioned gate prohibits double pulsing.
- Another latch functions as a start-stop circuit; it provides a fast switch-off and a slow start.
- A current protection circuit that operates via the start-stop circuit. This is a combined function with the current limit circuit, therefore pin 11 has two trip-on levels; the lower one for cycle-by-cycle current limiting, the upper one for current protection by means of switch-off and slow-start.
- A TTL-compatible remote on/off input at pin 10, also operating via the start-stop circuit.
- An inhibit input at pin 13. The output pulse can be inhibited immediately.
- An output gate that is commanded by the latches and the inhibit circuit.
- An output transistor of which both the collector (pin 15) and the emitter (pin 14) are externally available. This allows for normal or inverse output pulses.
- A power supply that can be either voltage or current driven (pins 1 and 12). The internally generated stabilized output voltage V_Z is connected to pin 2.
- A special function is the so-called feed-forward at pin 16. The amplitude of the sawtooth generator is modulated in such a way that the duty cycle becomes inversely proportional to the voltage on this pin: $\delta \sim C/V16$.
- Loop fault protection circuits assure that the duty-cycle is reduced to zero or a low value for open or short-circuited feedback loops.

Stabilized Power Supply (Pins 1, 2, 12)

The power supply of the NE5560 is of the well known series regulation type and provides a stablized output voltage of typically 8.5 volts.

This voltage V_Z is also present at pin 2 and can be used for precise setting of δ max. and to supply external circuitry. Its maximum current capability is 5mA.

The circuit can be fed directly from a DC voltage source between 10.5V and 18V or can be current driven via a limiting resistor. In the latter case, internal pinch-off resistors will limit the maximum supply voltage; typical 23V for 10mA and maximum 30V for 30mA.

The low supply voltage protection is active when V(1–12) is below 10.5V and inhibits the output pulse.

When the supply voltage surpasses the 10.5V level, the IC starts delivering output pulses via the slow-start function.

The current consumption at 12V is less than 10mA, provided that no current is drawn from V_Z and $R(7-12) \geqslant 20k\Omega$.

SWITCHED MODE POWER SUPPLY CONTROLLER NE/SE5561

DESCRIPTION

The NE5561/SE5561 is a control circuit for use in switched mode power supplies. It contains an internal temperature compensated supply, PWM, sawtooth oscillator, over-current sense latch, and output stage. The device is intended for low cost SMPS applications where extensive housekeeping functions are not required.

FEATURES

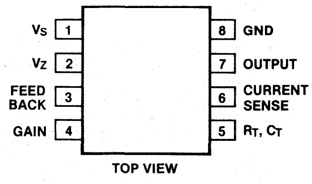
- **Micro-miniature (D) package**
- **Pulse-width modulator**
- **Current limiting (cycle by cycle)**
- **Sawtooth generator**
- **Stabilized power supply**
- **Double pulse protection**
- **Internal temperature compensated reference**

APPLICATIONS

- **Switch mode power supplies**
- **D/C motor controller inverter**
- **DC/DC converter**

PIN CONFIGURATION

D, FE, N PACKAGES

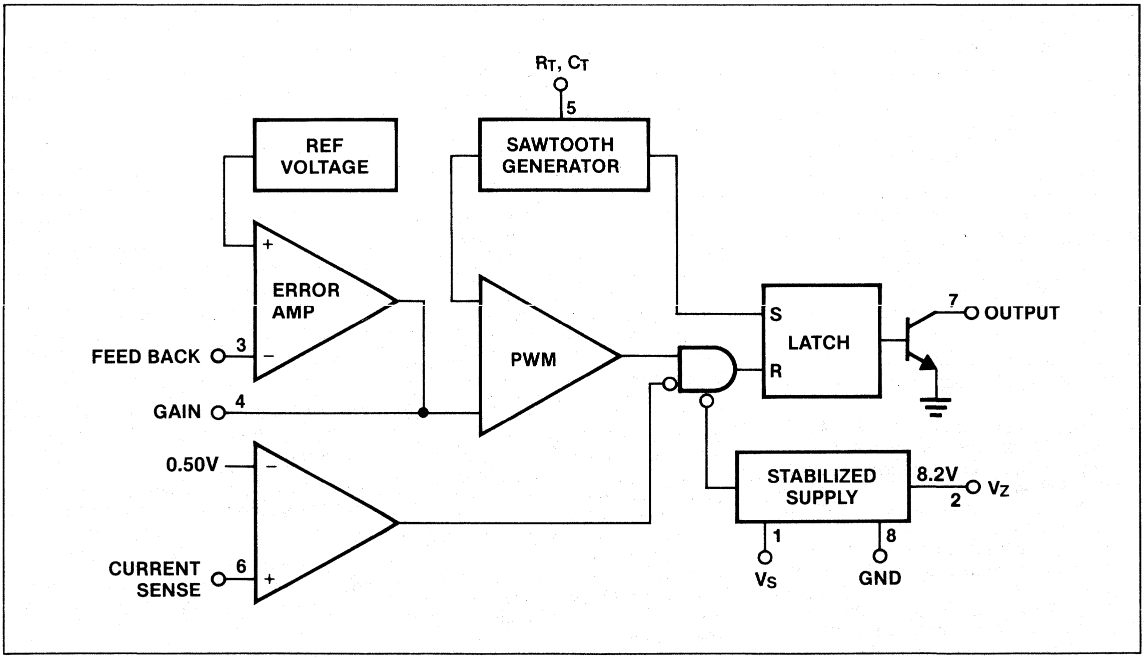


ORDER NUMBERS
NE5561D, NE5561FE, NE5561N,
SE5561FE, SE5561N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage, V_S	18	V
Output Current	40	mA
Output duty cycle	98	%
Max total power dissipation	0.75	W
Operating temperature range		
NE5561	0 to 70	°C
SE5561	−55 to +125	°C

BLOCK DIAGRAM



SWITCHED MODE POWER SUPPLY CONTROLLER NE/SE5561

DC ELECTRICAL CHARACTERISTICS $V_S = 12V$, $T_A = 25°C$ unless otherwise specified

SYMBOL AND PARAMETER	TEST CONDITIONS		SE5561			NE5561			UNIT
			Min	Typ	Max	Min	Typ	Max	
OSCILLATOR SECTION: Frequency range	Over temp		50		100k	50		100k	Hz
Initial accuracy				12			12		%
Duty cycle range	$f_o = 20kHz$		0		98	0		98	%
REFERENCE SECTION: V_{REF}, Internal ref voltage		Over temp	3.65		3.88	3.55		3.98	V
		$T_A = 25°C$	3.69	3.75	3.84	3.57	3.75	3.96	V
V_Z, internal zener ref	$I_L = 7mA$		7.8	8.2	8.8	7.8	8.2	8.8	V
Temp coefficient of V_{REF}				100			100		ppm/°C
Temp coefficient of V_Z				– 175			– 175		ppm/°C
CURRENT LIMITING (I_{IN})	Pin 6 = 250mV	$T_A = 25°C$		– 2	– 10		– 2	– 10	μA
		Over temp			– 20			– 20	μA
Single pulse inhibit delay	Inhibit delay time for 20% overdrive at	$I_{OUT} = 40mA$		0.7	0.8		0.7	0.8	μs
		$I_{OUT} = 20mA$		0.88	1.10		0.88	1.10	μs
Current limit trip level			.400	.500	.600	.400	.500	.600	V
ERROR AMPLIFIER: Open loop gain				60			60		dB
Feedback resistor			10k			10k			Ω
Small signal bandwidth				3			3		MHz
Output voltage swing (pos)			6.2			6.2			V
Output voltage swing (neg)					0.7			0.7	V
OUTPUT STAGE: Output current		Over temp	20			20			mA
V_{ce} Sat	$I_C = 20mA$	Over temp			0.4			0.4	V
SUPPLY VOLTAGE/CURRENT: I_S	$I_Z = 0$, voltage fed	$T_A = 25°C$			10.0			10.0	mA
		Over temp			13.0			13.0	mA
V_S	$I_S = 10mA$, current fed		20.0	21.0	22.0	19.0	21.0	24.0	V

REGULATION VS ERROR AMP CLOSED LOOP GAIN

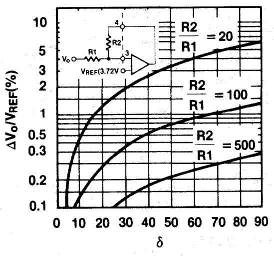


Figure 1

TRANSFER CURVE OF PULSE-WIDTH MODULATOR DUTY CYCLE VS INPUT VOLTAGE

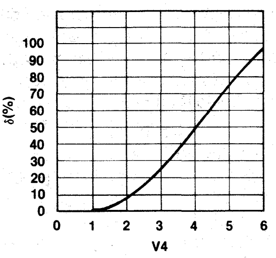


Figure 2

POWER DERATING CURVE

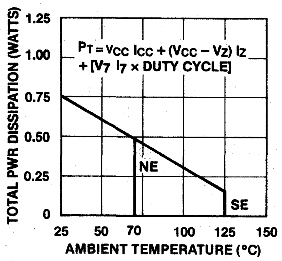


Figure 3

TYPICAL FREQUENCY PLOT VS R_T AND C_T

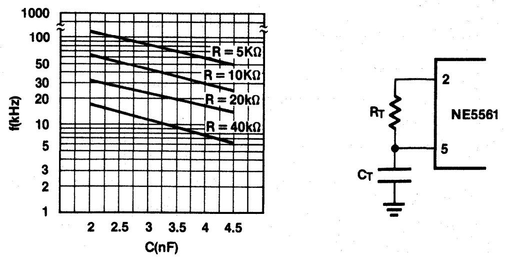


Figure 4

MAXIMUM DUTY CYCLE VS BASE VOLTAGE ON Q1

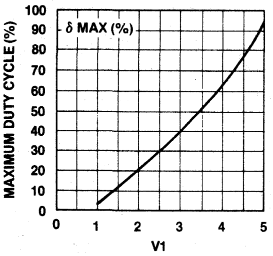
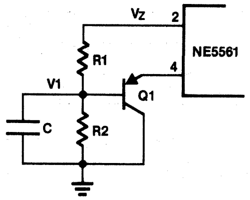


Figure 5a

START-UP CIRCUIT



$$\delta \max = f \left[\frac{R2}{R1 + R2} V_Z + V_{BE\ Q1} \right]$$

Figure 5b

SLOW START VOLTAGE

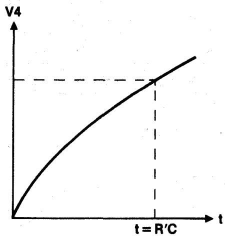


Figure 5c

NE5561 Start-Up

The start-up, or initial turn on, of this device requires some degree of external protective duty cycle limiting to prevent the duty cycle from initially going to the extreme maximum ($\delta > 90\%$). Either over-current limit or slow start circuitry must be employed to limit duty cycle to a safe value during start-up. Both may be used if desired.

To implement slow-start, the circuit of Figure 5b can be used. The divider R1 and R2 sets a voltage, buffered by Q1, such that the output of the error amplifier is clamped to a maximum output voltage, (Figure 5a) thereby limiting the maximum duty cycle. The addition of capacitor C will cause this voltage to ramp up slowly when power is applied, causing the duty cycle to ramp up simultaneously.

Over-current limit may be used also. To limit duty cycle in this mode, the switch current is monitored at pin 6 and the output of the 5561 is disabled on a cycle by cycle basis when current reaches the programmed limit. With current limit control of slow-start, the duty cycle is limited to that value just allowing maximum switch current to flow. (Approximately 0.50V measured at pin 6.)

5V, 0.5A Buck Regulator Operates from 15V

The converter design shows how simple it is to derive a TTL supply from a system supply of 15V (see Figure 6). The NE5561 drives a 2N4920 PNP transistor directly to provide switching current to the inductor. Overall line regulation is excellent and covers a range of 12V to 18V with minimal change (< 10 mV) in the output operating at full load.

As with all NE5561 circuits, the auxiliary slow start and δ_{max} circuit is required, as evidenced by Q1. The δ_{max} limit may be calculated by using the relationship (Figure 5a, b).

$$\frac{R2}{R1 + R2} (8.2V) = V_{\delta(max)}.$$

The maximum duty cycle is then determined from the pulse-width modulator transfer graph (see Figure 5a), and R1, R2 are defined from the desired conditions.

NE5561 Boost Converter with Output Variable (18V to 30V, 0.2A)

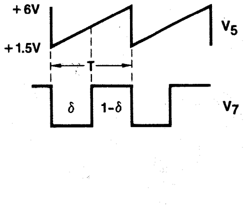
The circuit shown uses the NE5561 SMPS controller in a non-isolated boost converter operating from a 15V line. The addition of three transistors and one diode is necessary to complete the design (see Figure 7).

Operation is as follows. Q1 is a combination slow start and max duty cycle limit transistor. When power is first applied to the circuit, C7 in a discharged state begins to charge toward the divider voltage, V_δ. This $V_\delta + V_{BE}$ controls the voltage on pin 4, the error amp output, causing the duty cycle to be limited initially to δ_0, then to gradually approach its normal operating range, δ. The base divider is fed from V_Z, which is nominally 8.2V.

Output regulation starts at the error amplifier, with gain set by R2 (adj) and R5 combination. The error amp is stable for closed loop gain in excess of 40 dB (X100), for which the regulation will be approximately 1%. C4 is added to the output to insure stability at gain below 40 dB. C4 creates a dominant pole at approximately 1 kHz, descending at 6 dB per octave to unity near 1 MHz. Input to the error amplifier is referenced to 3.76V and must reach this reference level for the output of the NE5561 to be active. Output voltage is then the quantity. (D_R) 3.7V

If R2 ratio is, for instance, 10:1, the output will be ≃ 37V. If the ratio is 5:1, the output will be ≃ 18.5V, etc.

Output to Q2 base is a square wave of variable duty cycle as determined by load demand. The internal transistor is open collector and must have a pull-up resistance, in this application the base circuit of Q2. The duty cycle δ is a fraction between 0 and 1. The actual on-time is proportional then to $\delta \bullet T$, where T is the period of the free-running frequency of the sawtooth generator internal the NE5561. Frequency is set by the RC combination, R7 • C5 with charging current supplied from V_Z (8.2V). The stabilizing effect of the internal zener supply gives a constant frequency. The sawtooth waveform is related to duty cycle as shown below.



(V₇ NOT TO SCALE)

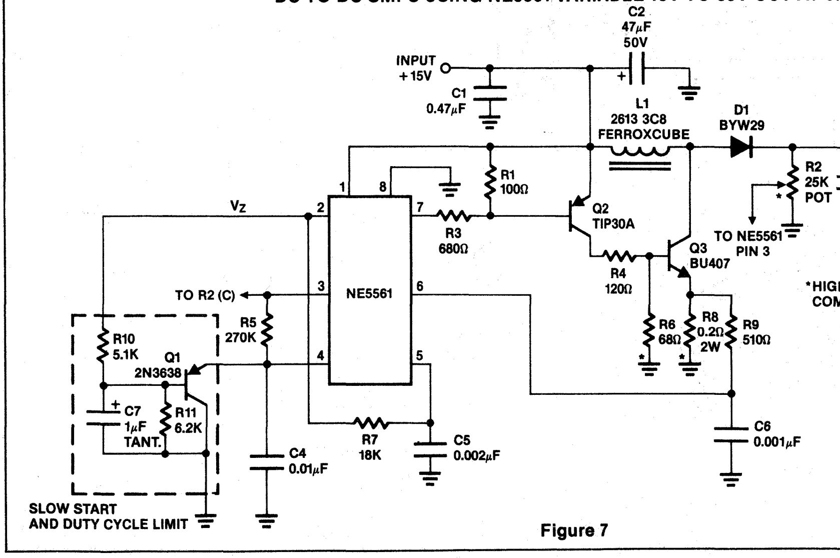
Q3 is switched on during the saturated portion of the output waveform from pin 7 of the NE5561, termed δ, and is switched off during the remainder of the cycle $(1-\delta)$.

The sawtooth frequency is set at approximately 22 kHz in this example. The NE5561 is capable of operation to 100 kHz, however.

Pin 6 of the NE5561 operates an over-current protective feature which resets the output on pin 7 if the instantaneous pin 6 voltage exceeds 0.50V. In this case, R8 determines the peak current of Q3 emitter circuit prior to shutdown. The operation of the over-current circuit is on a pulse to pulse basis, returning to normal as soon as the pin 6 voltage falls below 0.50V. As is noted, a small degree of filtering is needed to eliminate short switching transient, allowing only the primary current waveform to be sensed.

Switching circuit operation proceeds as follows. Q3 turns on, causing magnetization current to begin increasing in L1, the switching inductor. After initial start up, C3 is charged to the output, thus with Q3 on, Diode D1 is reverse biased and does not conduct during the duty cycle, δ. C3, the output capacitor, sustains the full load current during this part of the cycle. When Q3 turns off, the magnetic field energy previously stored in L1 is discharged through

DC TO DC SMPS USING NE5561 VARIABLE 18V TO 30V OUT AT 0.2A



C5 is the timing capacitor (0.03μF for 22 kHz)

L1 is Ferroxcube 2613-3C8 with 14 turns of #18 enameled wire (0.14 mH)

$$\delta f_{max} = f\left[\frac{R11}{R10 + R11}(V_Z) + V_{BE}\right]$$

Figure 7

D1 now forward biased. The output capacitor is incrementally charged, restoring its depleted voltage. The ripple voltage is a function of the size of C3 and its internal resistance. For minimum ripple, a low ESR (Equivalent Series Resistance) capacitor must be used, since previously mentioned peak load current flows in C3.

Single Transistor 100V, 250 mA Buck Converter

With a single 15V zener diode to limit package dissipation, the NE5561 controller may be operated directly from the rectified AC line. The following example shows the simplicity of such a converter which is capable of a nominal 100V output (see Figure 9). A base drive transformer is used to gain high voltage isolation between the NE5561 and the switching transistor, and to provide adequate base drive. A low power PNP transistor is used in an auxilliary slow start and duty cycle limiting circuit to prevent over-excitation (Q1).

Operation is as follows. Drive from the NE5561 output is fed to the primary of T1, base drive transformer, with a pulse-width modulated signal causing Q2 (BU407) to switch current to inductor, L1. As the current builds up, energy is stored in L1, coincident with the saturation period (δ) of the NE5561 output stage. During this period, current also flows through L1 to C_O and the load. When Q2 cuts off, the choke field collapses and D1 conducts as the load is sustained by the inductor-stored energy.

V_{OUT} is sampled by the divider R7 and R8, rising until the junction of the divider is forced to 3.75V. Load variations are thus translated to duty cycle variations to maintain constant voltage at the output. The measured efficiency at 0.5A load is in excess of 72%. Line regulation is good from approximately 93V to 120V.

The base current waveform driving Q2 is shown in Figure 8. This indicates that the BU407 base current rises initially to 60 mA to obtain fast turn-on, then settles to about 40 mA for the remainder of the duty cycle, δ. Reverse biasing of the emitter-base junction occurs to enhance turn-off.

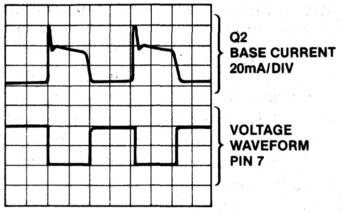
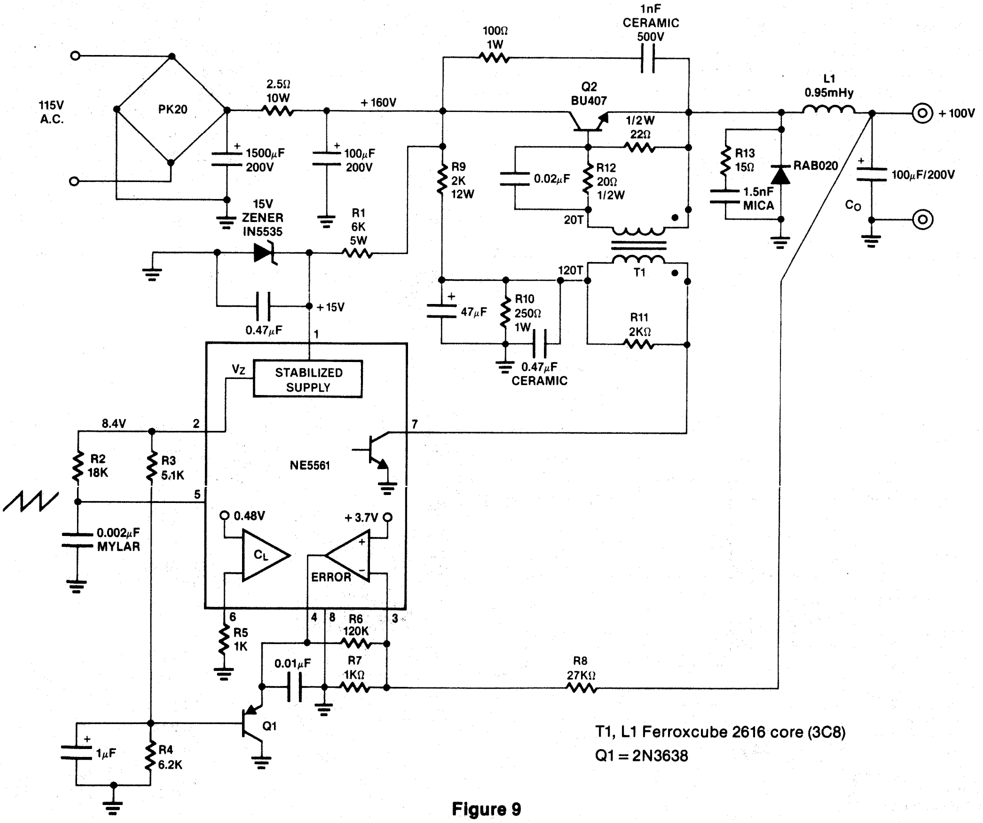


Figure 8

NE5561 100V/0.25A SWITCH MODE CONVERTER



T1, L1 Ferroxcube 2616 core (3C8)

Q1 = 2N3638

Figure 9

Snubber networks are necessary, as shown across Q2 and commutation diode, D1, to prevent component failure during fast switching. It is critical that these networks be placed physically adjacent to the respective components they protect, and that low inductance capacitors and resistors be used as snubbers (ceramic or dura mica caps and carbon resistors).

The base drive transformer is constructed using a Ferroxcube 2616-3C8 core, with primary of 120 turns of #26 wire, and 20 turns of #26 on secondary. The primary is wound in a simple solenoidal manner, first on the bobbin, followed by a layer of mylar tape to provide voltage isolation. Next, the secondary winding is added. Primary inductance measures 45 mH with a leakage inductance of 120 μH. It is important to have sufficient primary inductance to prevent excessive droop in base drive current. Also, leakage reactance must be kept reasonably low to minimize ringing.

DC Motor Drive with Fixed Speed Control

The circuit shown in Figure 10b incorporates a simple switch mode approach to DC motor control, which is efficient and free of the dissipation problems inherent in linear drives. The NE5561 provides pulse proportional drive and speed control based on DC tachometer feedback. A simple switching circuit consisting of one transistor (2N4920 PNP) and a commutation diode is used to deliver programmed pulse energy to the motor.

A frequency of approximately 20 kHz is used to eliminate audio noise present in some switching drives. The DC tach in this example delivers 2.7V/1000 RPM. Its output is such that negative feedback occurs when this voltage is applied to the error amplifier of the NE5561, pin 3, through a suitable divider. Note that the voltage to pin 3 must be 3.75V in order to obtain servo lock. Thus, the divider from the tach output must be appropriate to maintain the proper ratio for speed control to occur.

As shown in the waveform photo (Figure 10a), duty cycle varies directly with load torque demand. No load current is ≈ 0.3A and full load is 0.6A. Current and voltage waveforms at 0.6A are shown in Figure 10. If desired, torque limiting may be set by feeding a derivative of motor return current back to pin 6 of the NE5561.

Operating range is 12V to 18V input for a tach output nominal variation of less than 20 mV, and approximately 4.35V for the divider values shown. The motor is a Globe 100A 565 rated at 12V DC.

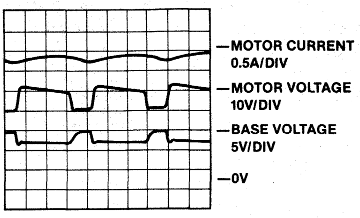


Figure 10a

NE5561 PULSE-WIDTH MODULATED MOTOR DRIVE (CONSTANT SPEED)

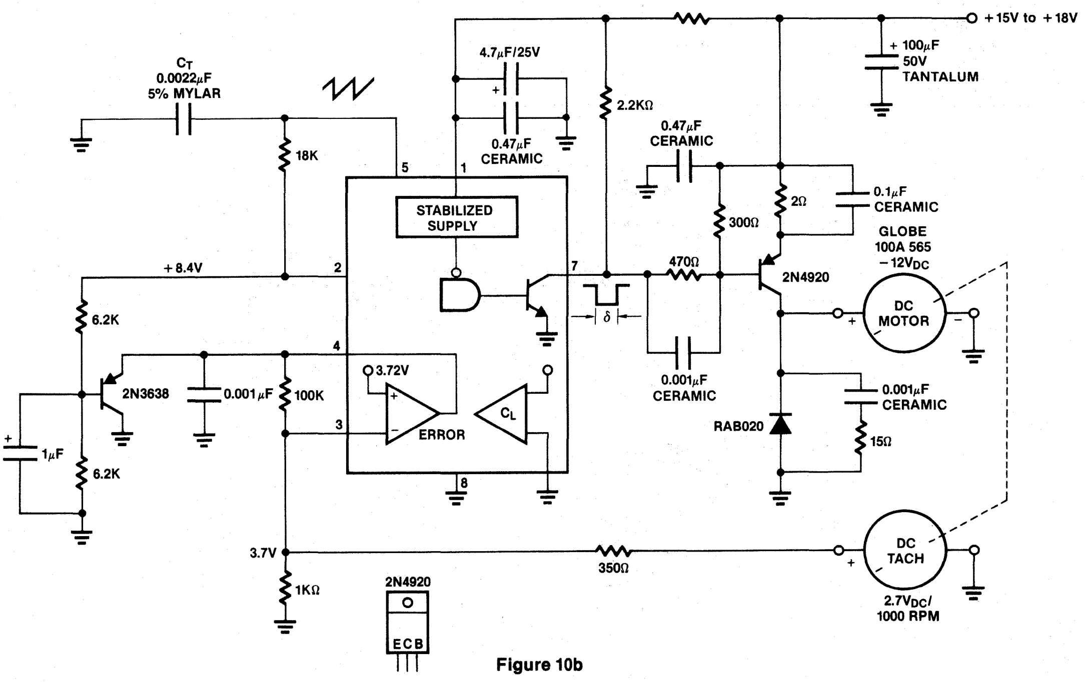


Figure 10b

REGULATING PULSE WIDTH MODULATOR SG1524/SG2524/SG3524

DESCRIPTION

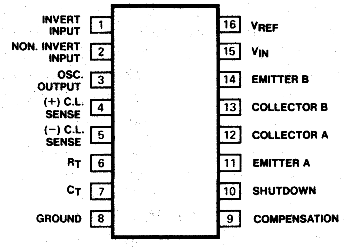
This monolithic integrated circuit contains all the control circuitry for a regulating power supply inverter or switching regulator. Included in a 16-pin dual-in-line package is the voltage reference, error-amplifier, oscillator, pulse width modulator, pulse steering flip-flop, dual alternating output switches and current limiting and shut-down circuitry. This device can be used for switching regulators of either polarity, transformer coupled DC to DC converters, transformerless voltage doublers and polarity converters, as well as other power control applications. The SG1524 is specified for operation over the full military temperature range of −55°C to +125°C, while the SG2524 and SG3524 are designed for commercial applications of 0°C to +70°C.

FEATURES

- **Complete PWM power control circuitry**
- **Single ended or push-pull outputs**
- **Line and load regulation of 0.2%**
- **1% maximum temperature variation**
- **Total supply current is less than 10mA**
- **Operation beyond 100kHz**

PIN CONFIGURATION

D,F,N PACKAGE



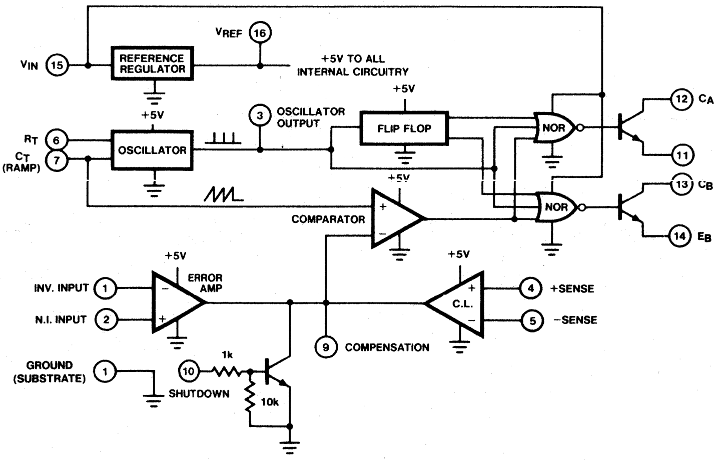
TOP VIEW

ORDER NUMBERS
SG1524F, SG2524F, SG2524N
SG3524F, SG3524N, SG3524D

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Input voltage	40	V
Output current (each output)	100	mA
Reference output current	50	mA
Oscillator charging current	5	mA
Power dissipation		
Package limitation	1000	mW
Derate above 25°C	8	mW / °C
Operating temperature range		
SG1524	−55 to +125	°C
SG2524 / SG3524	0 to +70	°C
Storage temperature range	−65 to +150	°C

BLOCK DIAGRAM



REGULATING PULSE WIDTH MODULATOR SG1524/SG2524/SG3524

DC ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for $T_A = -55°C$ to $+125°C$ for the SG1524 and 0°C to +70°C for the SG2524 and SG3524, V_{IN} = 20V, and f = 20kHz)

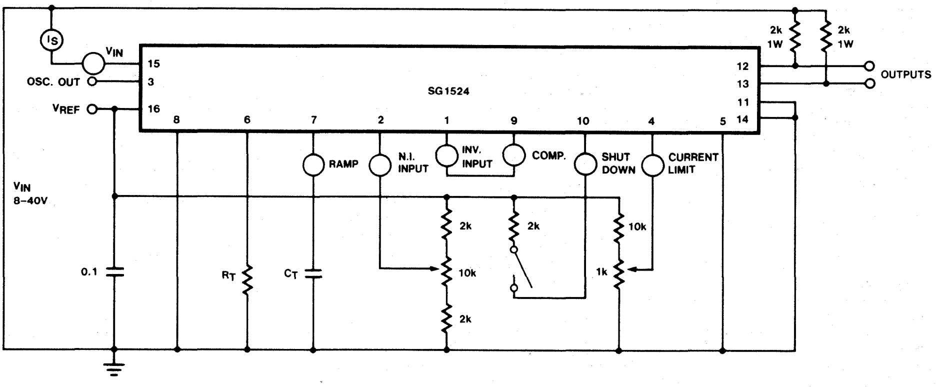
PARAMETER	TEST CONDITIONS	SG1524 SG2524			SG3524			UNIT
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Output voltage		4.8	5.0	5.2	4.6	5.0	5.4	V
Line regulation	V_{IN} = 8 to 40V		10	20		10	30	mV
Load regulation	I_L = 0 to 20mA		20	50		20	50	mV
Ripple rejection	f = 120Hz, T_A = 25°C		66			66		dB
Short circuit current limit	V_{REF} = 0, T_A = 25°C		100			100		mA
Temperature stability	Over operating temperature range		0.3	1		0.3	1	%
Long term stability	T_A = 25°C		20			20		mV/kHr
OSCILLATOR SECTION								
Maximum frequency	C_T = .001 mfd, R_T = 2kΩ		300			300		kHz
Initial accuracy	R_T and C_T constant		5			5		%
Voltage stability	V_{IN} = 8 to 40V, T_A = 25°C			1			1	%
Temperature stability	Over operating temperature range						2	%
Output amplitude	Pin 3, T_A = 25°C		3.5			3.5		V_P
Output pulse width	C_T = .01 mfd, T_A = 25°C		0.5			0.5		μs
ERROR AMPLIFIER SECTION								
Input offset voltage	V_{CM} = 2.5V		0.5	5		2	10	mV
Input bias current	V_{CM} = 2.5V		2	20		2	10	μA
Open loop voltage gain		72	80		60	80		dB
Common mode voltage	T_A = 25°C	1.8		3.4	1.8		3.4	V
Common mode rejection ratio	T_A = 25°C		70			70		dB
Small signal bandwidth	A_V = 0dB, T_A = 25°C		3			3		MHz
Output voltage	T_A = 25°C	0.5		3.8	0.5		3.8	V
COMPARATOR SECTION								
Duty cycle	% each output "ON"	0		45	0		45	%
Input threshold	Zero duty cycle		1			1		V
Input threshold	Maximum duty cycle		3.5			3.5		V
Input bias current			1			1		μA
CURRENT LIMITING SECTION								
Sense voltage	Pin 9 = 2V with error amplifier set for maximum out, T_A = 25°C	190	200	210	180	200	220	mV
Sense voltage T.C.			0.2			0.2		mV/°C
Common mode voltage		−1		+1	−1		+1	V
OUTPUT SECTION (each output)								
Collector-emitter voltage (breakdown)		40			40			V
Collector-leakage current	V_{CE} = 40V		0.1	50		0.1	50	μA
Saturation voltage	I_C = 50mA		1	2		1	2	V
Emitter output voltage	V_{IN} = 20V	17	18		17	18		V

DC ELECTRICAL CHARACTERISTICS (Cont'd)

(Unless otherwise stated, these specifications apply for $T_A = -55°C$ to $+125°C$ for the SG1524 and 0°C to +70°C for the SG2524 and SG3524, V_{IN} = 20V, and f = 20kHz)

PARAMETER	TEST CONDITIONS	SG1524 SG2524			SG3524			UNIT
		Min	Typ	Max	Min	Typ	Max	
Rise time	R_C = 2K ohm, T_A = 25°C		0.2			0.2		μs
Fall time	R_C = 2K ohm, T_A = 25°C		0.1			0.1		μs
TOTAL STANDBY CURRENT (excluding oscillator charging current, error and current limit dividers, and with outputs open)	V_{IN} = 40V		8	10		8	10	mA

OPEN LOOP TEST CIRCUIT



APPLICATIONS

Voltage Reference

An internal series regulator provides a nominal 5 volt output which is used both to generate a reference voltage and is the regulated source for all the internal timing and controlling circuitry. This regulator may be bypassed for operation from a fixed 5 volt supply by connecting pins 15 and 16 together to the input voltage. In this configuration, the maximum input voltage is 6.0 volts.

This reference regulator may be used as a 5 volt source for other circuitry. It will provide up to 50mA of current itself and can easily be expanded to higher currents with an external PNP as shown in Figure 1.

TYPICAL APPLICATION

EXPANDED REFERENCE CURRENT CAPABILITY

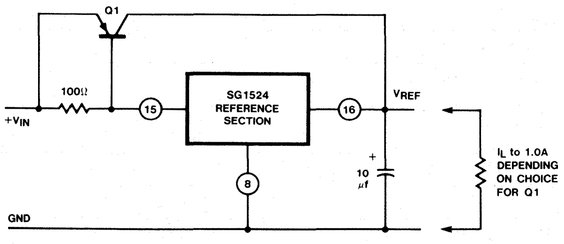


Figure 1

REGULATING PULSE WIDTH MODULATOR SG1524/SG2524/SG3524

OUTPUT STAGE DEAD TIME AS A FUNCTION OF THE TIMING CAPACITOR VALUE

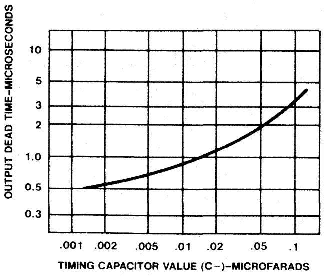


Figure 2

OSCILLATOR PERIOD AS A FUNCTION OF R_T AND C_T

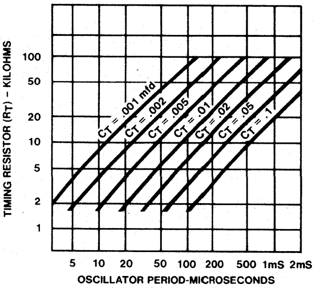


Figure 3

AMPLIFIES OPEN-LOOP GAIN AS A FUNCTION OF FREQUENCY AND LOADING ON PIN 9

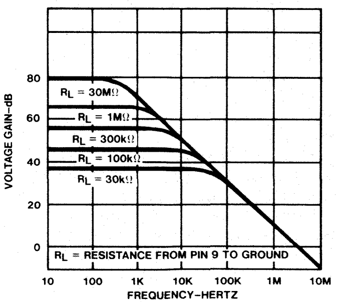


Figure 4

Oscillator

The oscillator in the SG1524 uses an external resistor (R_T) to establish a constant charging current into an external capacitor (C_T). While this uses more current than a series connected RC, it provides a linear ramp voltage on the capacitor which is also used as a reference for the comparator. The charging current is equal to 3.6V ÷ R_T and should be kept within the range of approximately 30μA to 2mA, i.e., 1.8K$<R_T<$100K.

The range of values for C_T also has limits as the discharge time of C_T determines the pulse width of the oscillator output pulse. This pulse is used (among other things) as a blanking pulse to both outputs to insure that there is no possibility of having both outputs on simultaneously during transitions. This output dead time relationship is shown in Figure 2. A pulse width below approximately 0.5 microseconds may allow false triggering of one output by removing the blanking pulse prior to the flip-flops reaching a stable state. If small values of C_T must be used, the pulse width may still be expanded by adding a shunt capacitance ($\approx$100pF) to ground at the oscillator output. (Note: Although the oscillator output is a convenient oscilloscope sync input, the cable and input capacitance may increase the blanking pulse width slightly.) Obviously, the upper limit to the pulse width is determined by the maximum duty cycle acceptable. Practical values of C_T fall between .001 and 0.1 microfarad.

The oscillator period is approximately t = R_TC_T where t is in microseconds when R_T = ohms and C_T = microfarads. The use of Figure 3 will allow selection of R_T and C_T for a wide range of operating frequencies. Note that for series regulator applications, the two outputs can be connected in parallel for an effective 0-90% duty cycle and the frequency of the oscillator is the frequency of the output. For push-pull applications, the outputs are separated and the flip-flop divides the frequency such that each outputs duty cycle is 0-45% and the overall frequency is one-half that of the oscillator.

External Synchronization

If it is desired to synchronize the SG1524 to an external clock, a pulse of $\approx$+3 volts may be applied to the oscillator output terminal with R_TC_T set slightly greater than the clock period. The same considerations of pulse width apply. The impedance to ground at this point is approximately 2K ohms.

If two or more SG1524's must be synchronized together, one must be designated as master with its R_TC_T set for the correct period. The slaves should each have an R_TC_T set for approximately 10% longer period than the master with the added requirement that C_T (slave) = one-half C_T (master). Then connecting Pin 3 on all units together will insure that the master output pulse—which occurs first and has a wider pulse width—will reset the slave units.

Error Amplifier

This circuit is a simple differential-input, transconductance amplifier. The output is the compensation terminal, pin 9, which is a high impedance node ($R_L \approx 5M\Omega$). The gain is

$$A_V = gmR_L = \frac{8\,I_C\,R_L}{2kT} \approx .002\,R_L$$

and can easily be reduced from a nominal of 10,000 by an external shunt resistance from pin 9 to ground, as shown in Figure 4.

In addition to DC gain control, the compensation terminal is also the place for AC phase compensation. The frequency response curves of Figure 4 show the uncompensated amplifier with a single pole at approximately 200Hz and a unity gain cross-over at 5MHz.

Typically, most output filter designs will introduce one or more additional poles at a significantly lower frequency. Therefore, the best stabilizing network is a series R-C combination between pin 9 and ground which introduces a zero to cancel one of the output filter poles. A good starting point is 50kΩ plus .001 microfarad.

One final point on the compensation terminal is that this is also a convenient place to insert any programming signal which is to override the error amplifier. Internal shutdown and current limit circuits are connected here, but any other circuit which can sink 200μA can pull this point to ground thus shutting off both outputs.

While feedback is normally applied around the entire regulator, the error amplifier can be used with conventional operational amplifier feedback and is stable in either the inverting or non-inverting mode. Regardless of the connections, however, input common-mode limits must be observed or output signal inversions may result. For conventional regulator applications, the 5 volt reference voltage must be divided down as shown in Figure 5. The error amplifier may also be used in fixed duty cycle applications by using the unity gain configuration shown in the open loop test circuit.

Current Limiting

The current limiting circuitry of the SG1524 is shown in Figure 6.

By matching the base-emitter voltages of Q1 and Q2, and assuming negligible voltage drop across R_1,

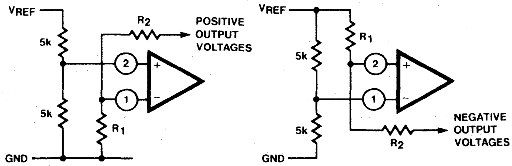
$$\text{Threshold} = V_{BE}(Q1) + I_1R_2 - V_{BE}(Q2)$$
$$= I_1R_2 \approx 200\text{mV}$$

Although this circuit provides a relatively small threshold with a negligible temperature coefficient, there are some limitations to its use, the most important of which is the ± 1 volt common mode range which requires sensing in the ground line. Another factor to consider is that the frequency compensation provided by R_1C_1 and Q1 provides a roll-off pole at approximately 300Hz.

Since the gain of this circuit is relatively low, there is a transition region as the current limit amplifier takes over pulse width control from the error amplifier. For testing purposes, threshold is defined as the input voltage to get 25% duty cycle with the error amplifier signaling maximum duty cycle.

In addition to constant current limiting, pins 4 and 5 may also be used in transformer-coupled circuits to sense primary current and shorten an output pulse, should transformer saturation occur. (Refer to Figure 11). Another application is to ground pin 5 and use pin 4 as an additional shutdown terminal: i.e., the output will be off with pin 4 open and on when it is grounded. Finally, foldback current limiting can be provided with the network of Figure 7. This circuit can reduce the short-circuit current (I_{SC}) to approximately one-third the maximum available output current (I_{MAX}).

ERROR AMPLIFIER BIASING CIRCUITS



$$V_O = \frac{2.5V\ (R + R_2)}{R_1} \qquad \frac{R_1\ R_2}{R_2 + R_2} = 2.5k\Omega$$

Note change in input connections for opposite polarity outputs.

Figure 5

CURRENT LIMITING CIRCUITRY OF THE SG 1524

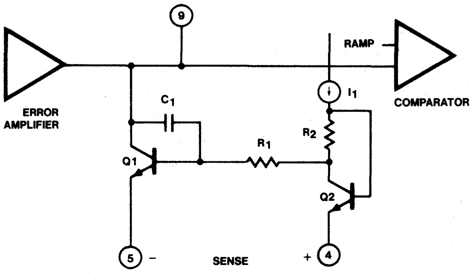
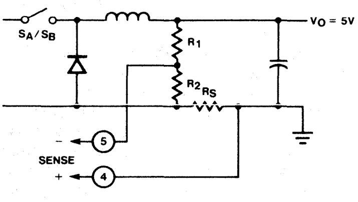


Figure 6

FOLDBACK CURRENT LIMITING



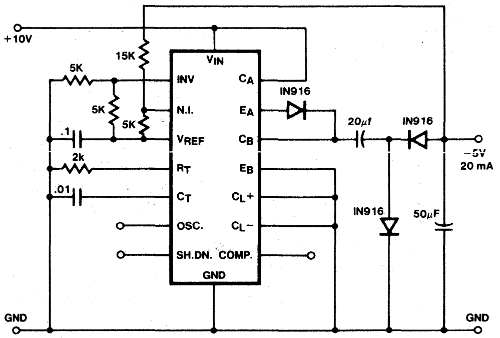
$$I_{MAX} = \frac{1}{R_S}\left(V_{TH} + \frac{V_O\ R_2}{R_1 + R_2}\right)$$

$$I_{SC} = \frac{V_{TH}}{R_S} \quad \text{WHERE}$$

$$V_{TH} = 200\ \text{mV}$$

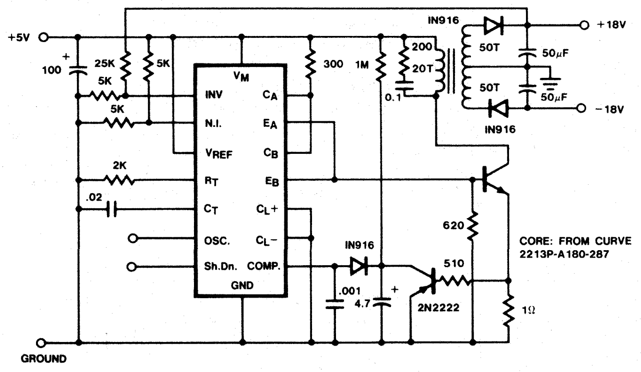
Foldback current limiting can be used to reduce power dissipation under shorted output conditions.

Figure 7



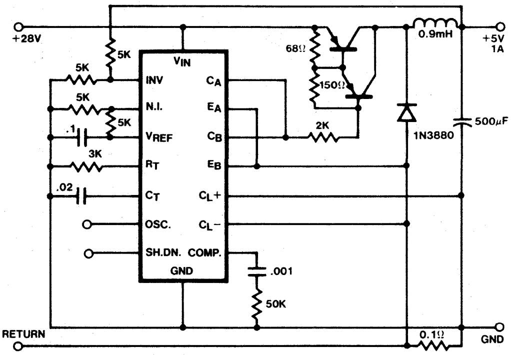
The capacitor-diode output circuit is used here as a polarity converter to generate a −5 volt supply from +15 volts. This circuit is useful for an output current of up to 20mA with no additional boost transistors required. Since the output transistors are current limited, no additional protection is necessary. Also, the lack of an inductor allows the circuit to be stabilized with only the output capacitor.

Figure 8



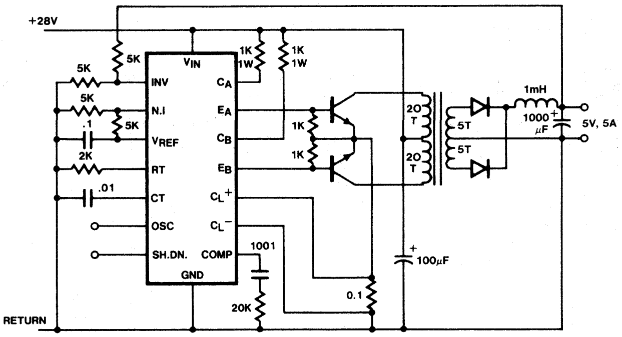
Another low-current supply is the flyback converter used here to generate ± 15 volts at 20mA from a +5 volt regulated line. The reference generator in the SG1524 is unused with the input voltage providing the reference. Current limiting in a flyback converter is difficult and is accomplished here by sensing current in the primary line and resetting a soft-start circuit.

Figure 9



In this conventional single-ended regulator circuit, the two outputs of the SG1524 are connected in parallel for effective .0-90% duty-cycle modulation. The use of an output inductor requires an R-C phase compensation network for loop stability.

Figure 10



Push-pull outputs are used in this transformer-coupled DC-DC regulating converter. Note that the oscillator must be set at twice the desired output frequency as the SG1524's internal flip-flop divides the frequency by 2 as it switches the P.W.M. signal from one output to the other. Current limiting is done here in the primary so that the pulse width will be reduced should transformer saturation occur.

Figure 11

PRECISION VOLTAGE REGULATOR

μA723/723C/SA723C

DESCRIPTION

The μA723/SA723C is a Monolithic Precision Voltage Regulator capable of operation in positive or negative supplies as a series, shunt, switching or floating regulator. The 723 contains a temperature compensated reference amplifier, error amplifier, series pass transistor, and current limiter, with access to remote shutdown.

FEATURES

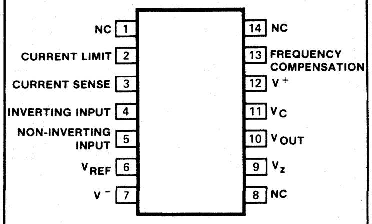
- **Positive or negative supply operation**
- **Series, shunt, switching or floating operation**
- **.01% line and load regulation**
- **Output voltage adjustable from 2 to 37 volts**
- **Output current to 150mA without external pass transistor**
- **μA723 MIL STD 88 3A, B, C available**

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Pulse voltage from V+ to V- (50 ms)	50	V
Continous voltage from V+ to V-	40	V
Input-output voltage differential	40	V
Maximum output current	150	mA
Current from V_{REF}	15	mA
Current from V_Z	25	mA
Internal power dissipation[1]	800	mw
Operating temperature range		
μA723	-55 to +125	°C
μA723C	0 to 70	°C
SA723C	-40 to +85	°C
Storage temperature range	-65 to +150	°C
Lead temperature	300	°C

PIN CONFIGURATIONS

D,F,N PACKAGE

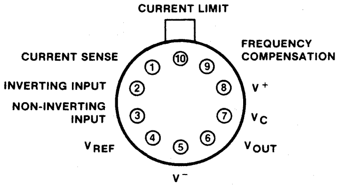


TOP VIEW

ORDER NUMBERS

μA723F,N μA723CF,CN
SA723CN μA723CD

H PACKAGE*

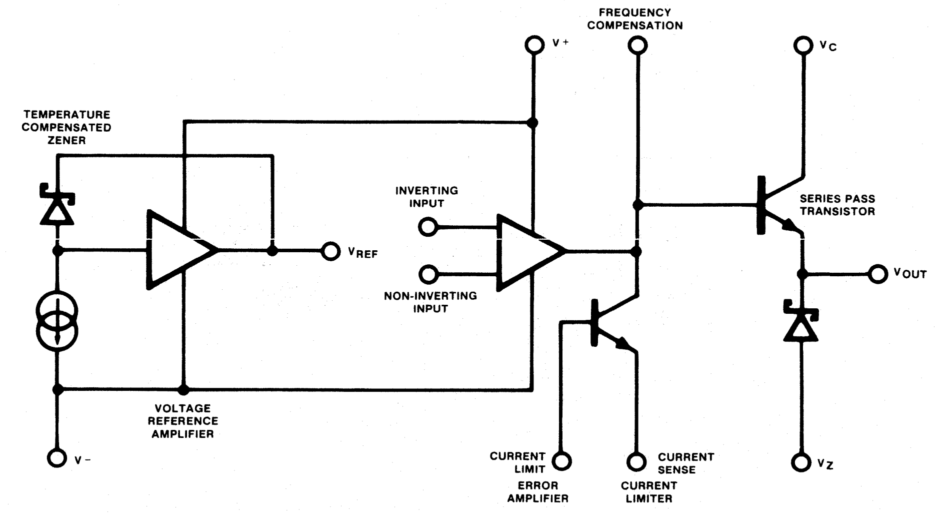


ORDER NUMBERS

μA723H μA723CH

*Metal cans (H) not recommended for new designs

EQUIVALENT CIRCUIT



PRECISION VOLTAGE REGULATOR μA723/723C/SA723C

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.[1]

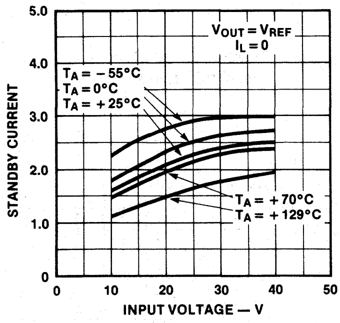
PARAMETER	TEST CONDITIONS	μA723			μA723C/SA723C			UNIT
		Min	Typ	Max	Min	Typ	Max	
Line regulation[2]	V_{IN} = 12V to V_{IN} = 15V		0.01	0.1		0.01	0.1	%V_{OUT}
	V_{IN} = 12V to V_{IN} = 40V		0.02	0.2		0.1	0.5	%V_{OUT}
Load regulation[2]	I_L = 1mA to I_L = 50mA		0.03	0.15		0.03	0.2	%V_{OUT}
	f = 50Hz to 10kHz, C_{REF} = 0		74			74		dB
	f = 50Hz to 10kHz, C_{REF} = 5μF		86			86		dB
Short circuit current limit	R_{SC} = 10Ω, V_{OUT} = 0		65			65		mA
Reference voltage		6.95	7.15	7.35	6.80	7.15	7.50	V
Output noise voltage	BW = 100Hz to 10kHz, C_{REF} = 0		20			20		μVrms
	BW = 100Hz to 10kHz, C_{REF} = 5μF		2.5			2.5		μVrms
Long term stability			0.1			0.1	0.1	%/1000hrs.
Standby current drain	I_L = 0, V_{IN} = 30V		2.3	3.5		2.3	4.0	mA
Input voltage range		9.5		40	9.5		40	V
Output voltage range		2.0		37	2.0		37	V
Input-output voltage differential		3.0		38	3.0		38	V
The following specifications apply over the operating temperature ranges								
Line regulation				0.3			0.3	%V_{OUT}
Load regulation				0.6			0.6	%V_{OUT}
Average temperature coefficient of output voltage	V_{IN} = 12V to V_{IN} = 15V I_L = 1mA to I_L = 50mA		0.002	0.015		0.003	0.015	%/°C

NOTES

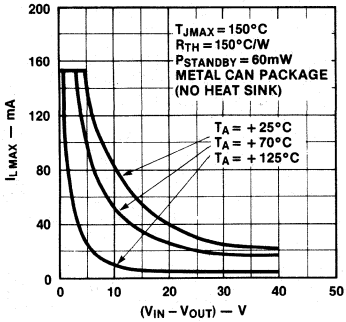
1. $V_{IN} = V+ = V_C = 12V$, $V- = 0V$, $V_{OUT} = 5V$, $I_L = 1mA$, $R_{SC} = 0$, $C_1 = 100pF$, $C_{REF} = 0$ and divider impedance as seen by error amplifier ≤ 10kΩ when connected as shown in Figure 3.
2. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

TYPICAL PERFORMANCE CHARACTERISTICS

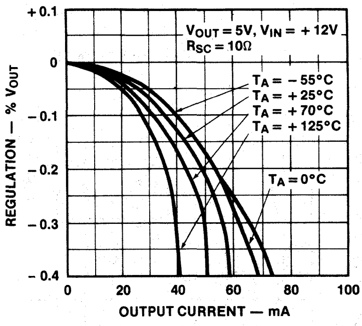
STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE



MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING

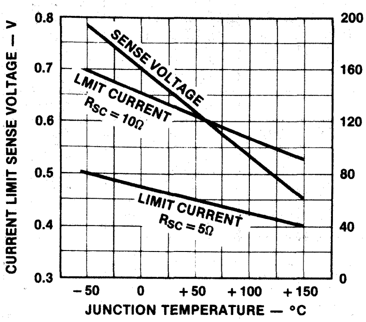


PRECISION VOLTAGE REGULATOR

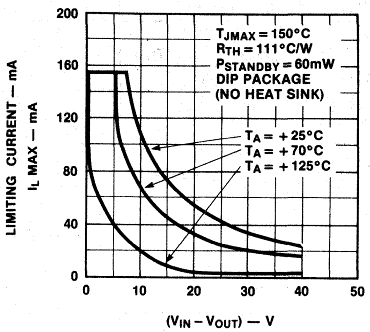
μA723/723C/SA723C

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

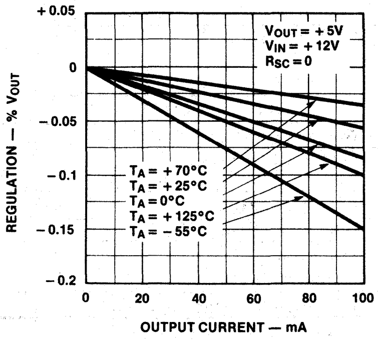
CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE



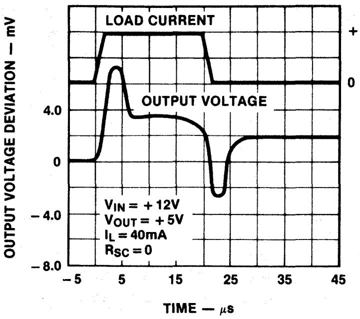
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



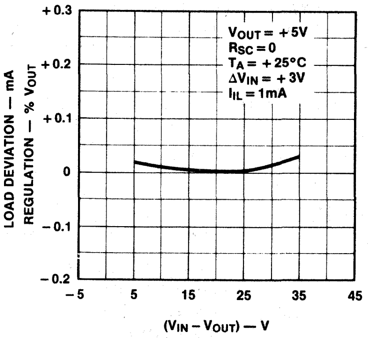
LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING



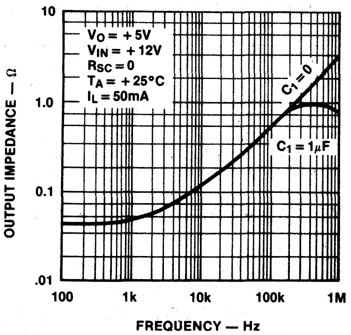
LOAD TRANSIENT RESPONSE



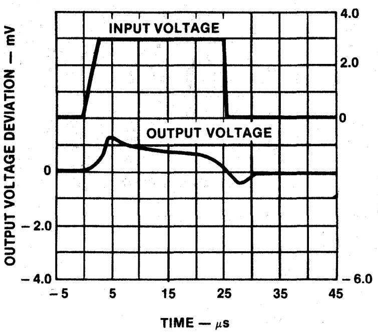
LINE REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



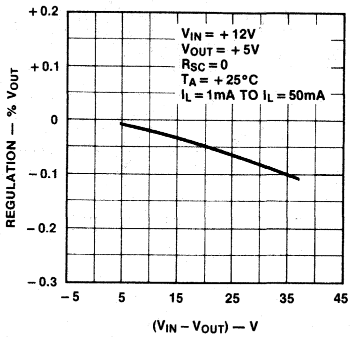
OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY



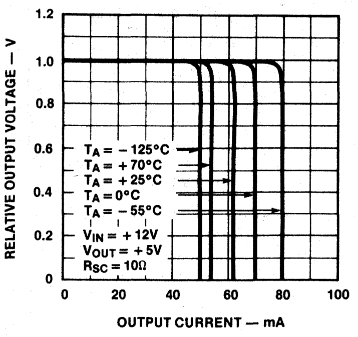
LINE TRANSIENT RESPONSE



LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

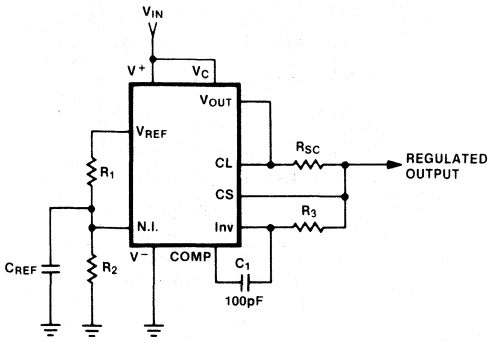


CURRENT LIMITING CHARACTERISTICS



TYPICAL APPLICATIONS

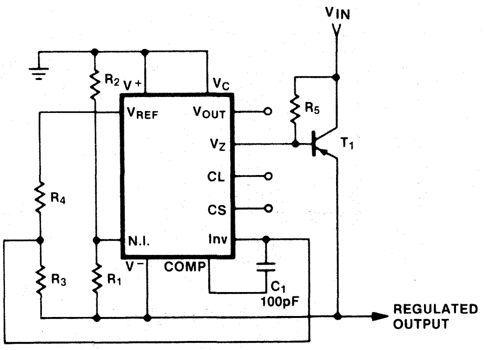
LOW VOLTAGE REGULATOR (V_{OUT} = 2 TO 7 VOLTS)



$$V_{OUT} = \left[V_{REF} \times \frac{R_2}{R_1 + R_2}\right]$$

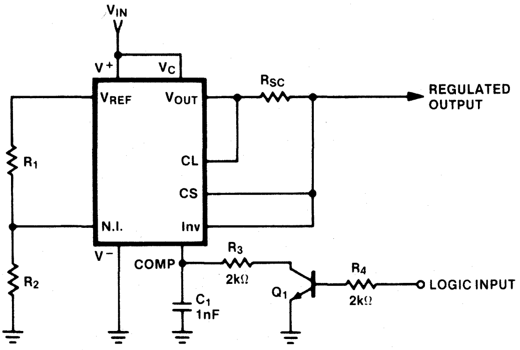
$R_3 = \frac{R_1 R_2}{R_1 + R_2}$ for minimum temperature drift

NEGATIVE VOLTAGE REGULATOR



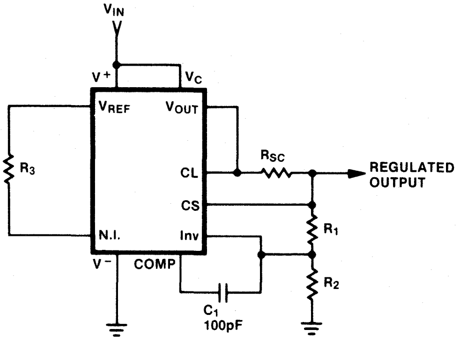
$$V_{OUT} = \left[\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1}\right];\ R_3 = R_4$$

REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING (V_{OUT} = 2 TO 7 VOLTS)



$$V_{OUT} = \left[V_{REF} \times \frac{R_2}{R_1 + R_2}\right]$$

HIGH VOLTAGE REGULATOR (V_{OUT} = 7 TO 37 VOLTS)



$$V_{OUT} = \left[V_{REF} \times \frac{R_1 + R_2}{R_2}\right]$$

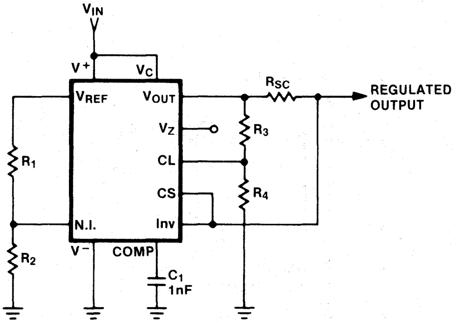
$R_3 = \frac{R_1 R_2}{R_1 + R_2}$ for minimum temperature drift

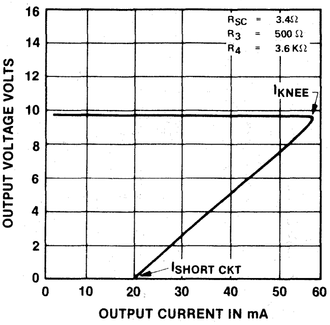
R3 may be eliminated for minimum component count

PRECISION VOLTAGE REGULATOR μA723/723C/SA723C

TYPICAL APPLICATIONS (Cont'd)

FOLDBACK CURRENT LIMITING REGULATOR
(V_{OUT} = 2 TO 7 VOLTS)





$$I_{KNEE} = \left[\frac{V_{OUT} R_3}{R_{SC} R_4} + \frac{V_{SENSE} (R_3 + R_4)}{R_{SC} R_4}\right]$$

$$V_{OUT} = \left[V_{REF} \times \frac{R_1 + R_2}{R_2}\right]$$

$$I_{SHORT\ CKT} = \left[\frac{V_{SENSE}}{R_{SC}} \times \frac{R_3 + R_4}{R_4}\right]$$

$$\frac{R_4}{R_3} = \frac{V_{OUT} I_{SC}}{V_{SENSE} (I_{KNEE} - I_{SHORT\ CKT})} - 1$$

$$R_{SC} = \frac{V_{SENSE}}{I_{SC}}\left[1 + \frac{R_3}{R_4}\right]$$

Section 7
Motor Control and Sensor Circuits

INDEX

Section 7 — Motor Control and Sensor Circuits

SERVO AMPLIFIER NE544/644

DESCRIPTION

The NE544 is a servo amplifier and pulse-width demodulator with internal motor drive transistors. It is designed for remote control applications in digital proportional systems but can be used in many other closed loop position control applications. It incorporates a linear one shot for improved positional accuracy and outputs for external pnp motor drive transistors.

FEATURES

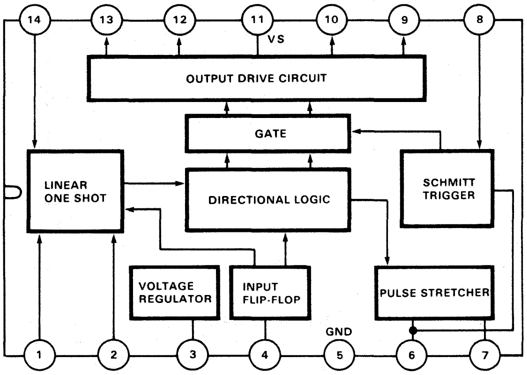
- **500mA load current capability**
- **Bidirectional bridge output with single power supply**
- **Low standby power drain**
- **Adjustable deadband and trigger thresholds**
- **High linearity, 0.5% maximum error**
- **Output drive for external PNP transistors (optional)**
- **Wide supply voltage range**

ABSOLUTE MAXIMUM RATINGS

$T_A = 25°C$ unless otherwise specified.

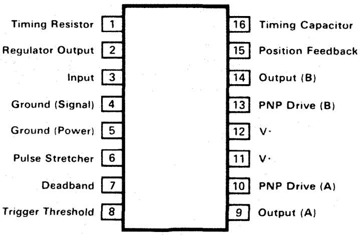
PARAMETER		RATING	UNIT
V+	Supply voltage	6.0	V
I_O	Output current	500	mA
T_A	Operating temperature	-20 to +75	°C
T_{stg}	Storage temperature	-65 to +150	°C

BLOCK DIAGRAM



PIN CONFIGURATIONS

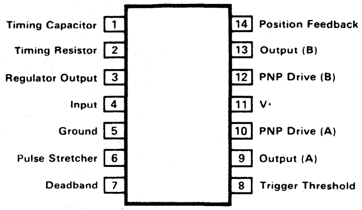
N PACKAGE



TOP VIEW

ORDER NUMBER
NE644N

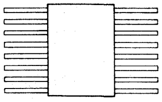
N PACKAGE



TOP VIEW

ORDER NUMBER
NE544N

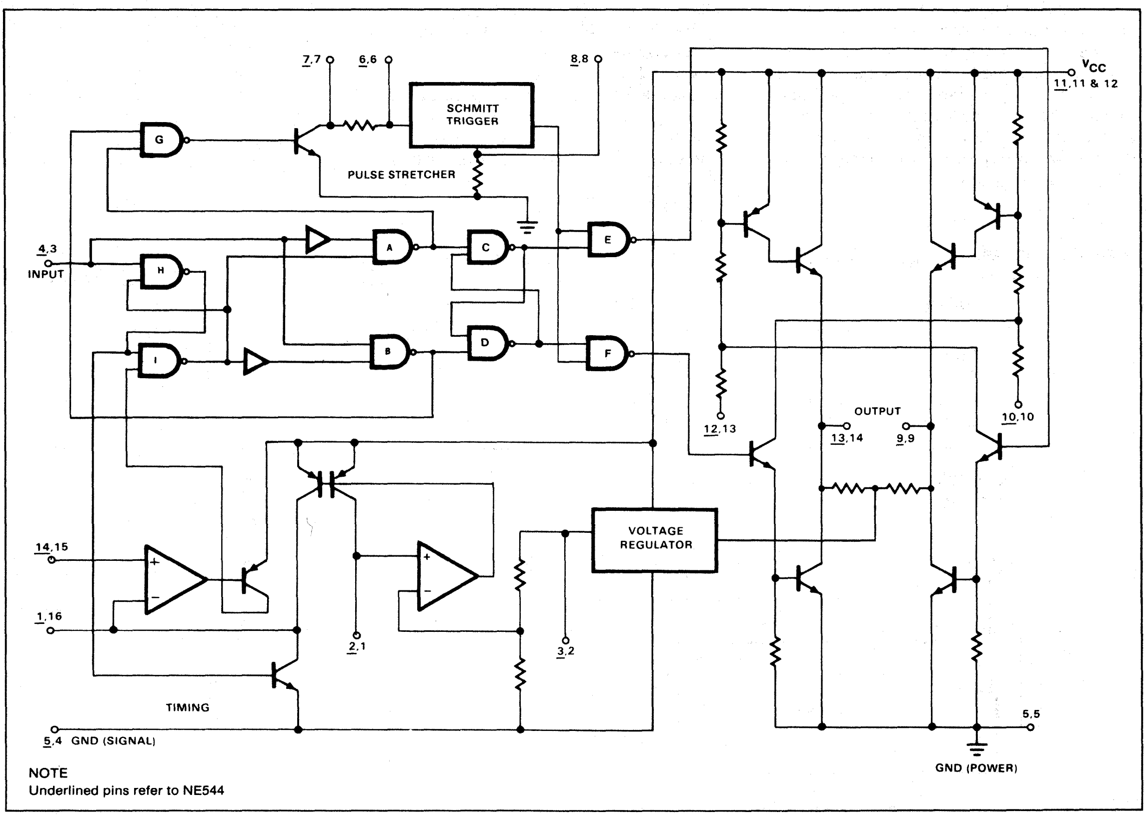
W PACKAGE*



*Pinout same as 644N package
Order part no. NE644W

SERVO AMPLIFIER NE544/644

EQUIVALENT CIRCUIT SCHEMATIC



NOTE
Underlined pins refer to NE544

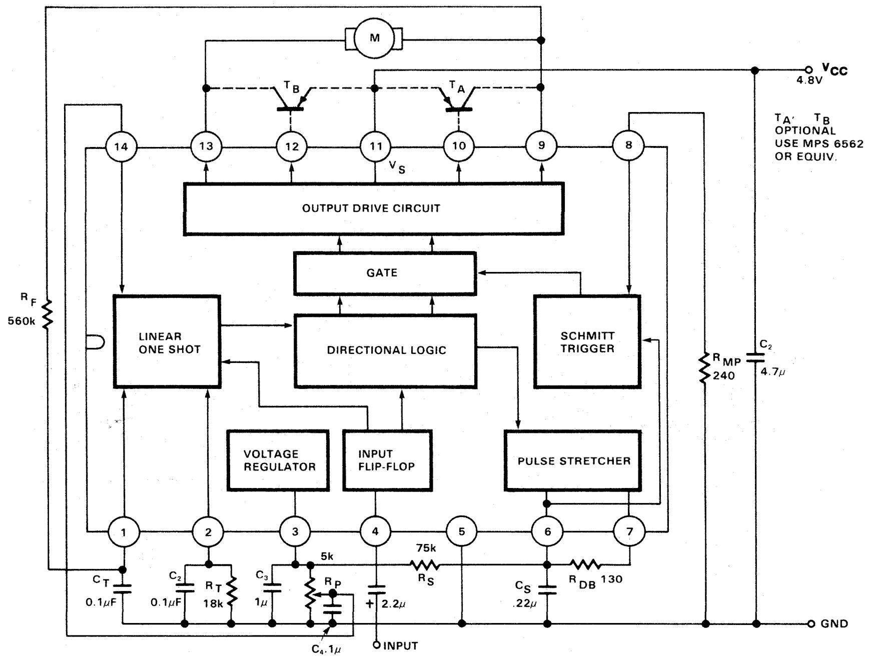
DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = 4.8V$ unless otherwise specified.

PARAMETER			TEST CONDITIONS	LIMITS			UNIT
				Min	Typ	Max	
V_{CC}	Supply voltage			3.2	4.8	6	V
I_{CC}	Supply current	Pin 11	Quiescent	4.2	5.5	10	mA
V_{TH}	Input threshold	Pin 4					V
	On				1.5		
	Off				1.4		
Z_{IN}	Input resistance	Pin 4			18		kΩ
	Output voltage						V
V_{OL}	Low		Pin 9 or 13, I_L = 400mA		0.3		
V_{OH}	High				3.9		
V_{REG}	Regulated voltage	Pin 3		2.1	2.5	2.9	V
ΔV_{REG}	Regulation	Pin 3	$3.5V \leq V_{CC} \leq 6V$		10		mV/V
	Minimum dead band	Pin 7	$R_{DB} = 0$		1		µs
	One shot temperature coefficient				.01		%/°C
	Standby output voltage		Pin 9 and 13		2.5		V
	PNP drive current		Pin 10 and 12		20		mA

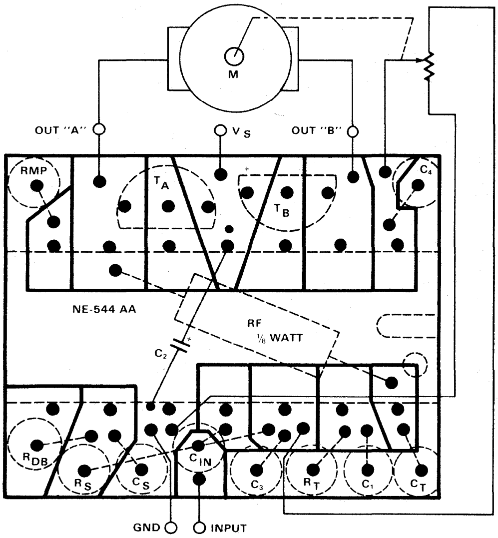
SERVO AMPLIFIER NE544/644

TYPICAL CONNECTION OF NE544N FOR LINEAR ONE SHOT TIMING

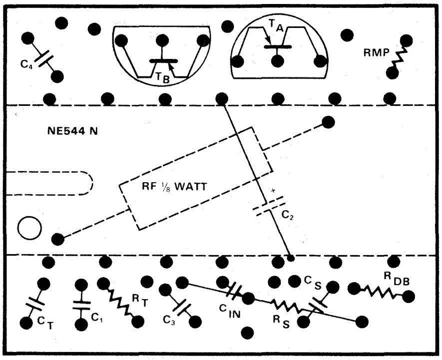


SERVO AMPLIFIER NE544/644

PC BOARD—N PACKAGE

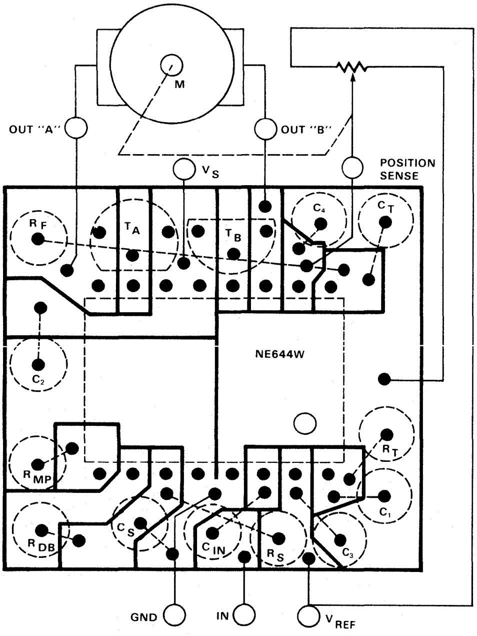


Typical PC Board Layout
Bottom View—4X

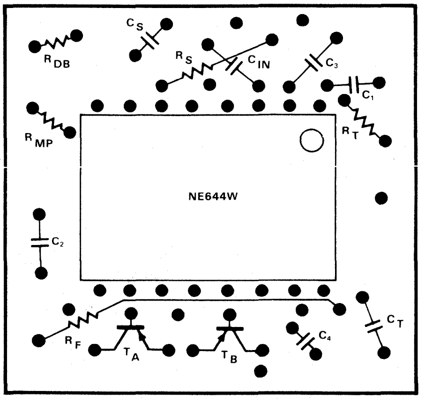


Parts Layout
Top View

PC BOARD—W PACKAGE

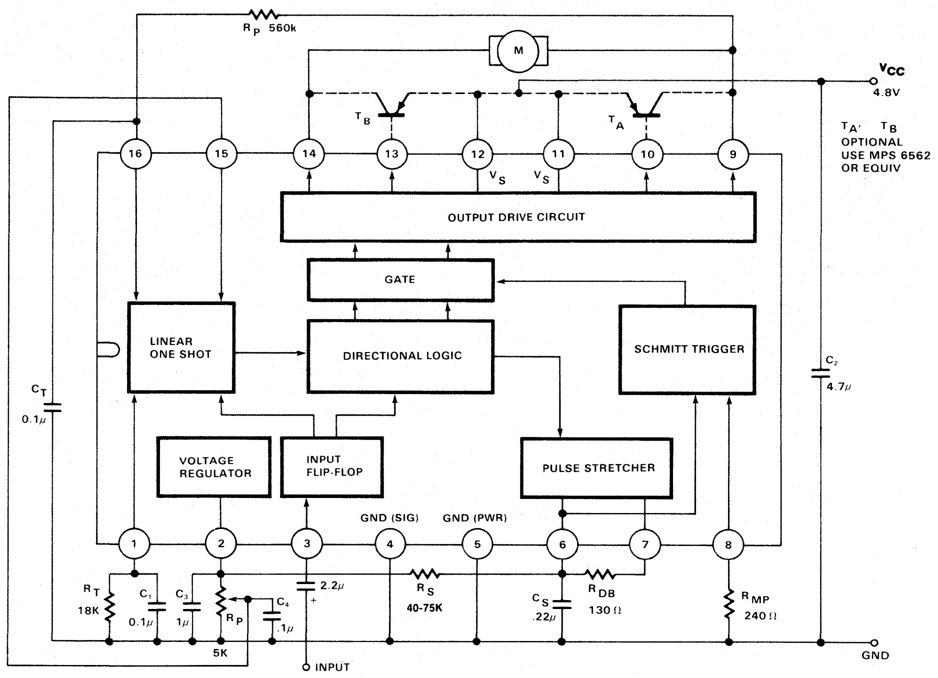


PC Board Layout
Bottom View—4X



Parts Layout
Top View

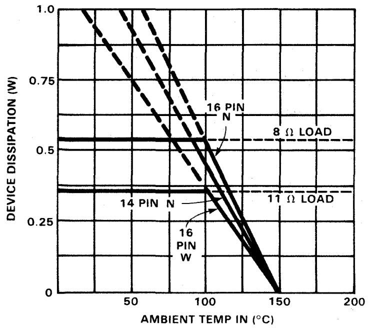
TYPICAL CONNECTION OF NE644W AND NE644N FOR LINEAR ONE SHOT TIMING



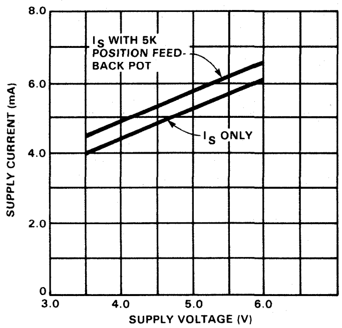
SERVO AMPLIFIER NE544/644

TYPICAL PERFORMANCE CHARACTERISTICS

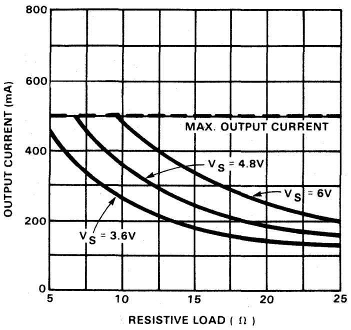
MAXIMUM DISSIPATION vs AMBIENT TEMPERATURE



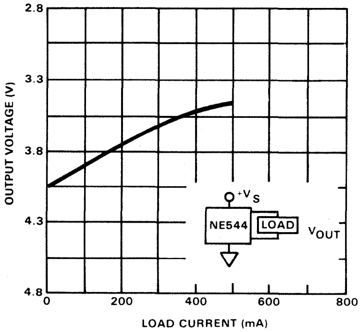
SUPPLY CURRENT vs SUPPLY VOLTAGE



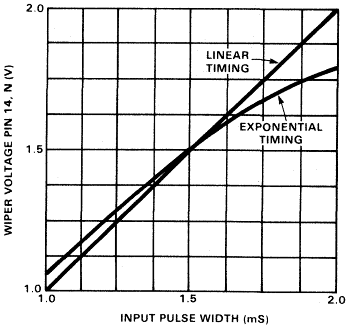
OUTPUT CURRENT vs LOAD RESISTANCE



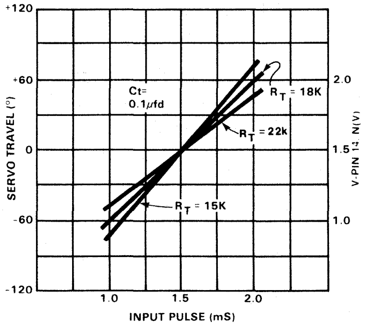
OUTPUT VOLTAGE vs LOAD CURRENT



INPUT PULSE WIDTH vs FEEDBACK POT OUTPUT



INPUT PULSE vs SERVO TRAVEL



PROGRAMMABLE SEVEN CHANNEL RC ENCODER NE5044

DESCRIPTION

The NE5044 is a programmable parallel input, serial output pulsewidth encoder. A multiplexed dual linear ramp technique is used to allow up to 7 inputs to be converted to a serial pulsewidth modulated signal with excellent linearity and minimal crosstalk. Fixed or variable frame rates can be used, externally controlled, for ease of demodulation. An onboard 5V regulator eliminates power supply sensitivities and provides up to 20mA current capability for driving external loads.

FEATURES

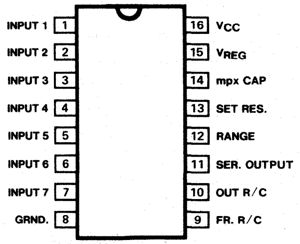
- **3 to 7 channels, externally selectable**
- **Constant current dual linear ramp for linearity better than .3%**
- **Internal voltage regulator for low drift**
- **Wide supply range 4.5 – 16V**
- **Fixed or variable frame rate set by external R-C**
- **External control for channel gain or range**
- **Versatile applications; exponential rates, mixing, dual rate, reversing etc.**
- **Compatible with all transmission mediums**

APPLICATIONS

- **Radio controlled aircraft, cars, boats, trains**
- **Industrial controllers**
- **Remote controlled entertainment systems**
- **Security systems**
- **Instrumentation recorders/controls**
- **Remote Analog/digital data transmission**
- **Automotive sensor systems**

PIN CONFIGURATION

D,N PACKAGE



TOP VIEW

ORDER NUMBERS

NE5044D NE5044N

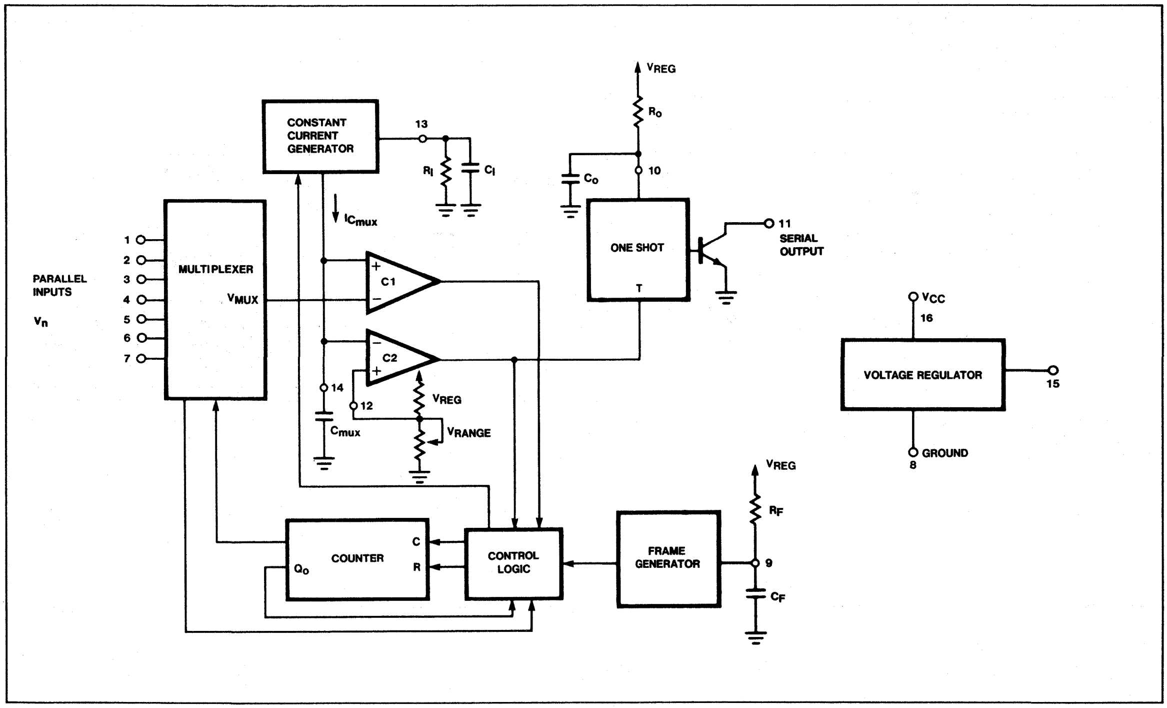
ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
V_{CC}, Supply voltage	17	V
Regulator ouput current	−25	mA
Serial output peak current	30	mA
Constant current generator	−1	mA
Parallel inputs, range input	0-V_{REG}	V
One shot input, frame generator input	0-V_{REG}	V
Operating temperature	−20 to +75	°C
Storage temperature	−65 to +150	°C

NOTE

1. T_A = 25° unless otherwise stated.

BLOCK DIAGRAM



PROGRAMMABLE SEVEN CHANNEL RC ENCODER NE5044

DC ELECTRICAL CHARACTERISTICS

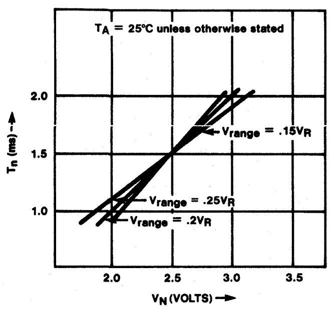
Test conditions $T_A = 25°C$, $V_{CC} = 10V$ using Test Circuit A unless otherwise stated.

PARAMETER		TEST CONDITIONS	NE 5044			UNIT
			Min	Typ	Max	
	POWER SUPPLY REQUIREMENTS[1]					
	Power supply voltage range		4.5		16	V
	Power supply current	Excluding control pots and serial output currents		11	15	mA
	VOLTAGE REGULATOR					
V_{REG}	Output voltage		4.5	5.0	5.5	V
	Output current	$V_R \geq 4.5V$			−20	mA
	Line regulation	$7 \leq V_{CC} \leq 16$		.005	0.2	V/V
	MULTIPLEXER					
	Input current	$V_n = 2.5v$		±30	±200	nA
	Input voltage range	$V_n - V_{Range} \geq .75V$	1.5		5	V
	Crosstalk			±1	±5	μs
	OUTPUT PULSE					
T_n	Position	$R_I \bullet C_{mux} = 1.25ms$ $V_n = .5V_{REG}$; $V_{RANGE} = .2V_{REG}$	1350	1500	1650	μs
	Position linearity error			5		μs
	Position tempco	$0°C \leq T_A \leq 70°C.$		.15		μs/°C
	Position PSR	$6V \leq V_{CC} \leq 16V$		.5	1	μs/V
T_O	Width	$R_OC_O = 300\mu s$	240	285	330	μs
	Saturation voltage	$I_O = 25mA$		.6	1	V
I_{11}	Leakage current			.05	50	μA
	Range input voltage	$R_I = 50k\Omega$	.75			V
		$R_I = 25k\Omega$	1.00			V
	Frame time (Fixed)	$R_FC_F = 30ms$	17	20	23	ms
	Inhibit threshold				.4	V

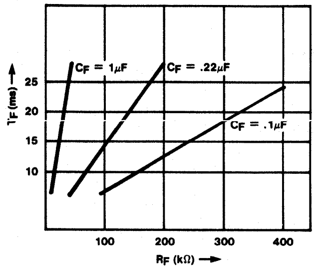
NOTE

1. At supply voltages exceeding 12 V, a current limiting resistor of 20 to 50Ω in series with V_{CC} is recommended.

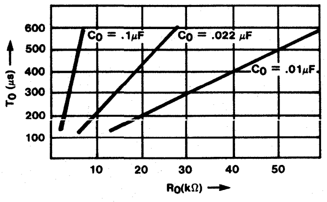
OUTPUT PULSE WIDTH (T_n) vs INPUT VOLTAGE (V_n)



FRAME TIME (T_F) vs R_F

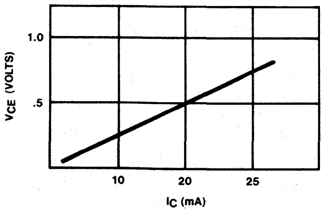


OUTPUT ONESHOT TIME (T_O) vs R_O

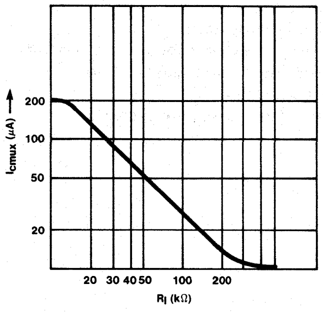


PROGRAMMABLE SEVEN CHANNEL RC ENCODER NE5044

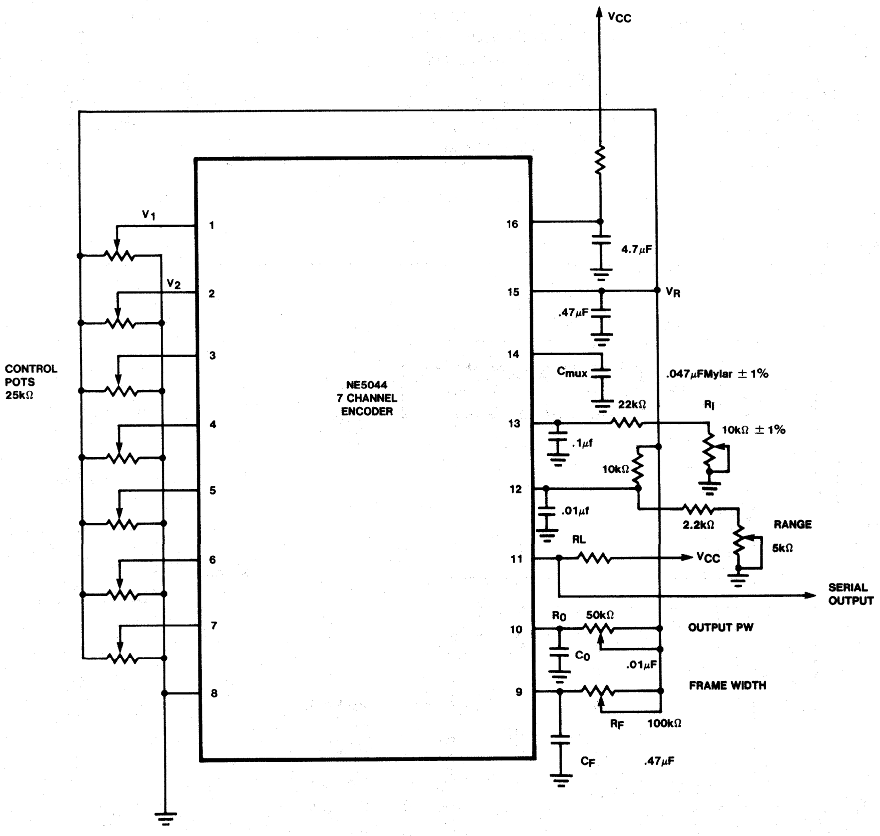
OUTPUT SATURATION VOLTAGE vs OUTPUT CURRENT



CONSTANT CURRENT vs R_I



TEST CIRCUIT A



SEVEN CHANNEL RC DECODER NE5045

DESCRIPTION

The NE5045 is a serial input, parallel output, decoder intended for applications in pulse width or pulse position modulation systems. The serial input pulse, either positive or negative, is shaped and amplified before being fed to the counter/decoder. An integrating type sync. separator detects pulses greater than $T_W = R_SC_S$. The amplified input pulse triggers an internal one-shot (minimum pulse) which in turn clocks the counter-decoder, thereby enhancing system noise rejection. A missing pulse detector resets the decoder during the sync. pause. An internal voltage regulator supplies power for the radio receiver providing excellent isolation from the power supply as well as the decoder logic.

FEATURES

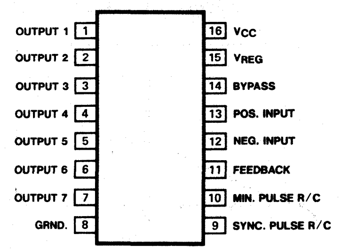
- **Decodes up to 7 channels**
- **High gain input amplifier**
- **Externally set sync. pause and minimum pulse**
- **Wide supply voltage range, 3.6V–8V.**
- **Positive or negative pulse inputs**
- **Noise and flutter rejection**
- **Outputs reset to zero without inputs**
- **Compatible with all transmission mediums**

APPLICATIONS

- **Radio controlled aircraft, cars, boats, trains**
- **Industrial controllers**
- **Remote controlled entertainment systems**
- **Security systems**
- **Instrumentation recorders/controls**
- **Remote Analog/digital data transmission**
- **Automotive sensor systems**

PIN CONFIGURATION

D,N PACKAGE



TOP VIEW

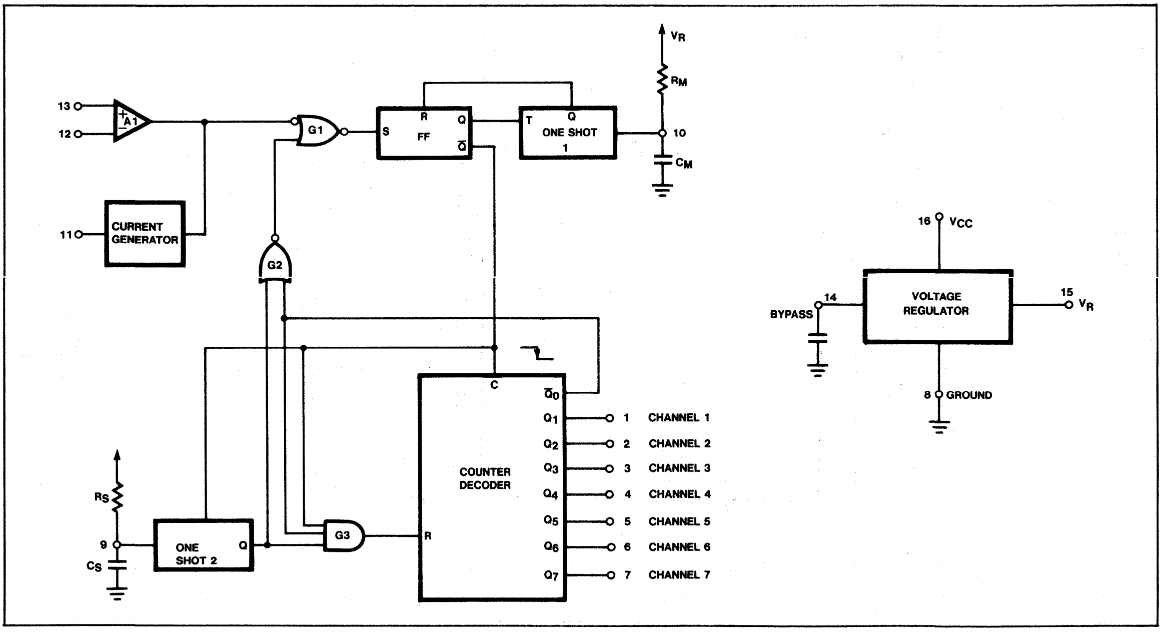
ORDER NUMBERS
NE5045N NE5045D

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
V_{CC}, Supply voltage	10	V
Regulator output current	−25	mA
Decoded output current	±5	mA
Pause input voltage	0 to V_R	V
Input amplifier voltage	0 to V_R	V
Operating temperature	−20 to +75	°C
Storage temperature	−65 to +150	°C

NOTE
1. T_A = 25°C unless otherwise stated

BLOCK DIAGRAM

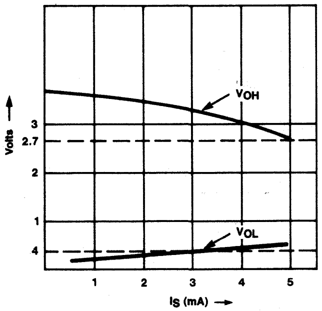


SEVEN CHANNEL RC DECODER NE5045

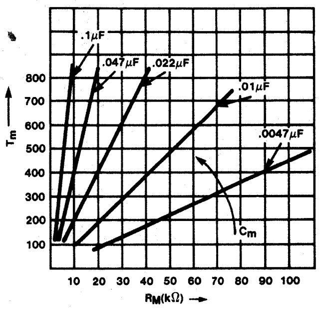
DC ELECTRICAL CHARACTERISTICS

Standard conditions: (T_A = 25°C, V_{CC} = 5.0V unless otherwise stated), using Test Circuit #1

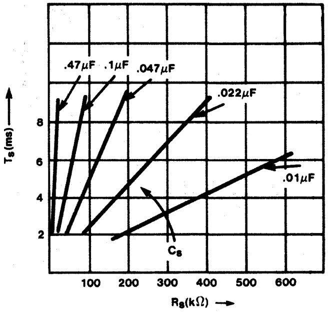
PARAMETER	TEST CONDITIONS	NE5045			UNIT
		Min	Typ	Max	
POWER SUPPLY REQUIREMENTS					
Power supply voltage range	Test circuit #1	3.6		8.0	V
Power supply current	Excluding input bias current		9.0	14.0	mA
VOLTAGE REGULATOR					
Output voltage		3.7	4.1	4.5	V
V_R Output current	$V_R \geq 3.7V$			−15	mA
Line regulation	V_{CC} = 6V to 8V		.01	.05	V/V
Voltage drop	V_{CC} = 4V, I_R = −10mA			1.3	V
INPUT AMPLIFIER					
Input bias current			10	100	nA
Input voltage range		2.0		4.0	V
Open loop gain			60		dB
Feedback current		100	200	400	µA
Detection threshold	Test circuit #1, ΔV12 & 13		8	20	mV
T_S Sync. pause time	$R_s C_s$ = 6.0ms	5.1	6.0	6.9	ms
T_M Minimum pulse time	$R_m C_m$ = 500µs	405	475	545	µs
OUTPUTS-ALL CHANNELS					
V_{OL}	I_{SINK} = 1mA		.25	.5	V
V_{OH}	I_{SOURCE} = 2mA	2.7			V



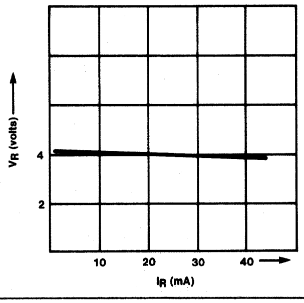
V_{OL} vs SINK CURRENT AND V_{OH} vs SOURCE CURRENT



MINIMUM PULSE TIME, T_M vs R_M, C_M



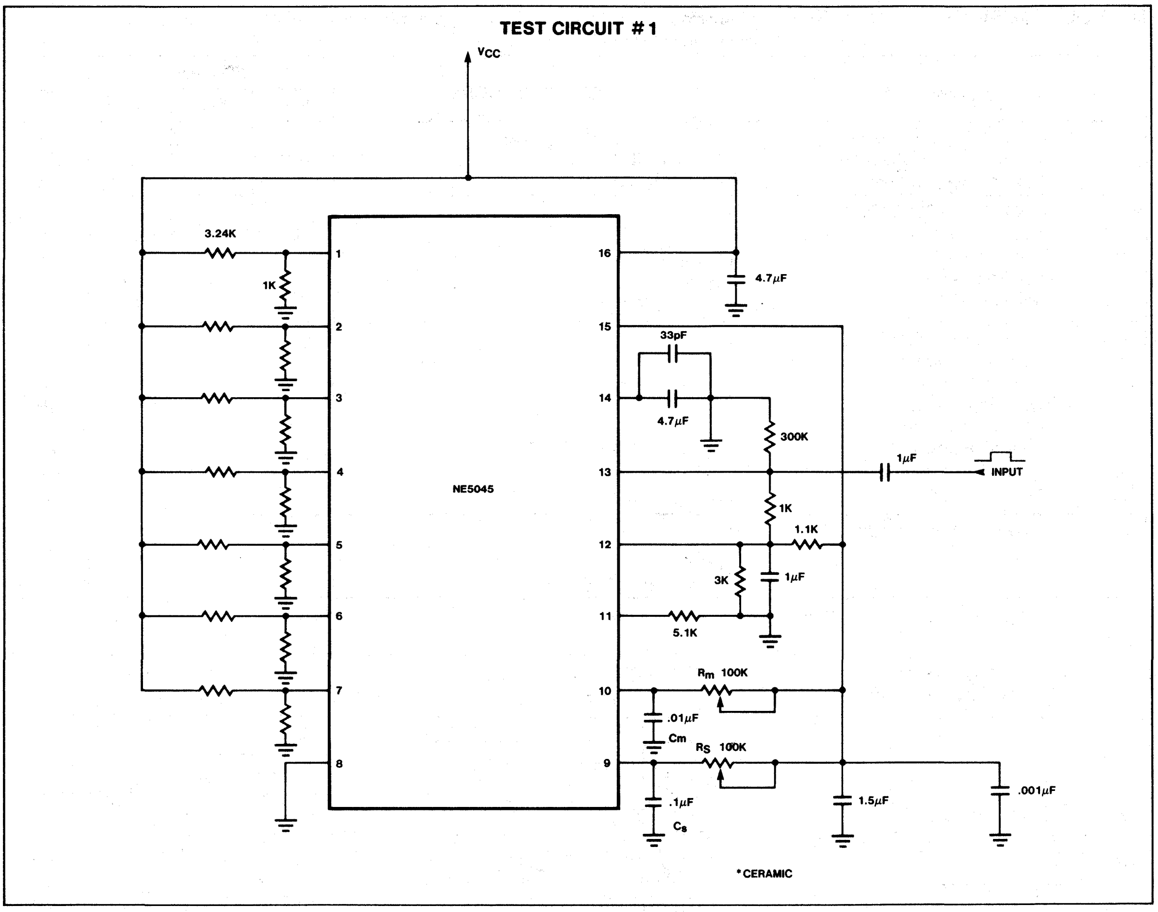
SYNC. PAUSETIME, T_s vs R_sC_s



REGULATOR VOLTAGE vs LOAD CURRENT

SEVEN CHANNEL RC DECODER

NE5045



2 CHANNEL RC DECODER NE5046

DESCRIPTION

The NE5046 is a serial input parallel output decoder designed for 2 channel digital proportional pulse width or pulse position modulation systems. The detection threshold is internally set and has hysteresis to prevent false triggering on noise. In a typical application, the serial input from the receiver is processed through an amplifier and pulse shaper, then converted to parallel output with a shift register. An internal sync separator detects the sync pause and clears the shift register. An internal voltage regulator provides power for the decoder and can be used to supply power for a radio receiver.

FEATURES

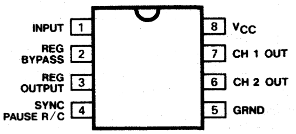
- **High gain input amplifier with hysteresis**
- **Externally adjustable sync separator**
- **Wide supply voltage range 3.6V–8V**
- **Noise and flutter rejection**
- **Outputs reset to zero without input**
- **Compatible with all transmission mediums**

APPLICATIONS

- **Radio-controlled aircraft, cars, boats, trains**
- **Industrial controllers**
- **Remote-controlled entertainment systems**
- **Security systems**
- **Instrumentation recorders/controls**
- **Remote Analog/digital data transmission**
- **Automotive sensor systems**

PIN CONFIGURATION

N PACKAGE



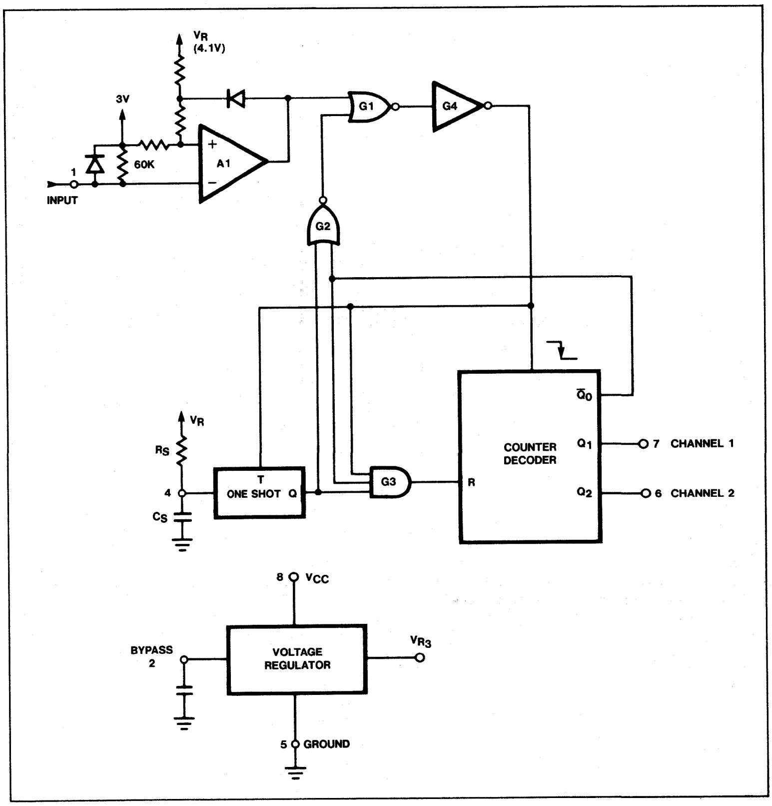
TOP VIEW
ORDER NUMBER
NE5046N (2 CHANNEL DECODER)

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
V_{CC}, Supply voltage	10	V
Regulator output current	−25	mA
Decoded output current	±5	mA
Sync pause input	0 to V_R	V
Input amplifier voltage	0 to V_R	V
Input amplifier current	±1	mA
Operating temperature	−20 to +75	°C
Storage temperature	−65 to +150	°C

NOTE
1. T_A = 25°C unless otherwise stated.

BLOCK DIAGRAM



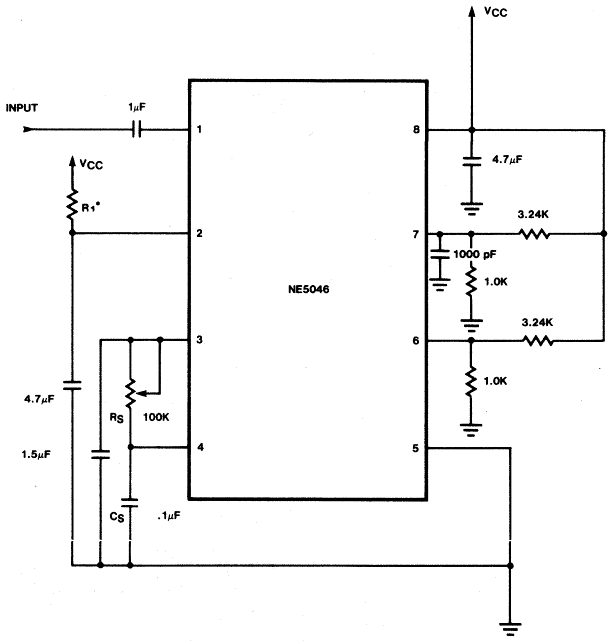
2 CHANNEL RC DECODER

NE5046

DC ELECTRICAL CHARACTERISTICS Test Conditions: $T_A = 25°C$, $V_{CC} = 5V$, Test Circuit 1, unless otherwise stated.

PARAMETER	TEST CONDITIONS	NE5046			UNIT
		Min	Typ	Max	
V_{CC} supply voltage		3.6	5.0	8.0	V
Power supply current			6.0	9.0	mA
Regulator output voltage		3.0	4.1	4.5	V
Regulator output current	$V_R \geq 3.6V$			−15	mA
Regulator line regulation	$V_{CC} = 6V$ to $8V$		.01	.05	V/V
Regulator voltage drop	$V_{CC} = 4V$, $I_R = -10mA$			1.0	V
Input threshold voltage		.15			V
Sync. pause time	$R_S C_S = 6ms$	5.1	6.0	6.9	ms
Output voltage both channels			.25		
V_{OL}	$I_{SINK} = 1mA$			.5	V
V_{OH}	$I_{SOURCE} = 2mA$	2.7			V

TEST CIRCUITS



NOTE
*A 2kΩ to 10kΩ resistor may be required to insure start-up under extreme load current and supply voltage conditions at low temperatures.

LVDT SIGNAL CONDITIONER

NE/SE5520

Preliminary

DESCRIPTION

The NE/SE5520 is a signal conditioning circuit for use with Linear Variable Differential Transformers (LVDT). The chip includes a low distortion amplitude stable sine wave oscillator with programmable frequency to drive the primary of the LVDT; a synchronous demodulator to convert the LVDT output amplitude and phase to position information; and an output amp to provide gain and filtering.

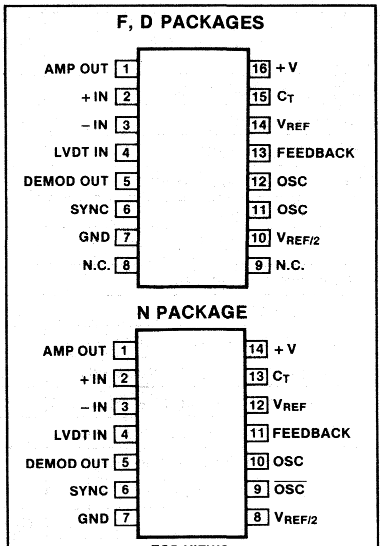
FEATURES

- Oscillator frequency: 1kHz to 20kHz
- Low distortion <5%
- Capable of ratiometric operation
- Single supply operation 5 to 25V or dual supply ±5 to ±12V
- Low power consumption

APPLICATIONS

- LVDT signal conditioning
- RVDT signal conditioning

PIN CONFIGURATION



TOP VIEWS

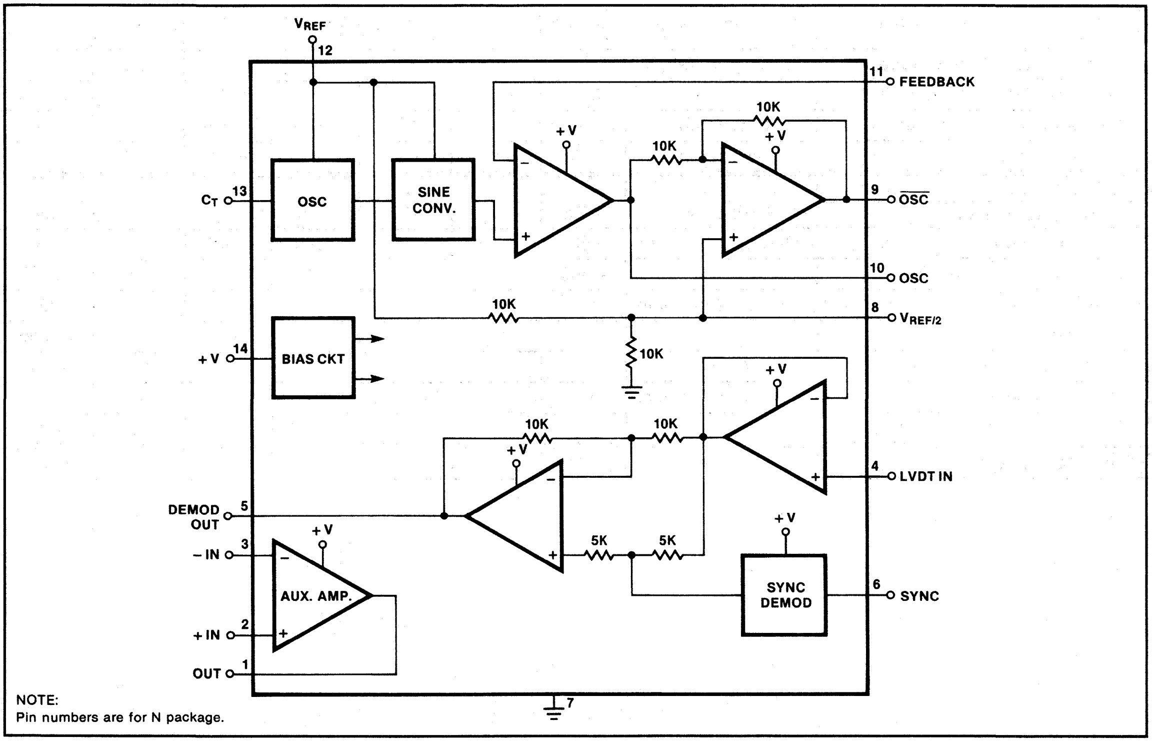
ORDER NUMBERS

NE5520D, NE5520F, SE5520F (16-Pin)
NE5520N (14-Pin)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	+30	V
Split supply voltage	(±15)	V
Operating temperature range		
SE5520	−55 to +125	°C
NE5520	0 to +70	°C
Storage temperature range	−65 to 150	°C

BLOCK DIAGRAM



NOTE:
Pin numbers are for N package.

LVDT SIGNAL CONDITIONER NE/SE5520

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DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_R = V+ = 10V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE5520			NE5520			UNIT
		Min	Typ	Max	Min	Typ	Max	
Supply voltage range	Over temp.	5		25	5		25	V
Supply current	Over temp.		7.0	9		7.0	8.5	mA
Reference current	Over temp.		5.5	8.0		5.5	7.0	mA
Reference voltage range	Over temp.	5		V+	5		V+	V
Oscillator section								
Oscillator output			$\frac{V_R}{8}$			$\frac{V_R}{8}$		Vrms
Sine wave distortion	Over temp.		3.5	5		3.5	5	%
Initial amplitude error			0.5	1.0		0.5	1.0	%
Tempco of amplitude error				0.05			0.05	%/°C
Voltage coef. of amplitude error				0.05			0.05	%/V
Voltage coef. of ratiometric error	Over temp.	0.99		1.01	0.995		1.005	V/V
Initial accuracy of osc. frequency			10	20		10		%
Tempco of frequency error			0.05	0.1		.05		%/°C
Voltage coef. of frequency			10	15		10		%/V(V_R)
Frequency range	$C_T = 0.005$ to $0.1\mu F$	1		20	1		20	kHz
Oscillator output load		1			1			kΩ
Demodulator section								
Linearity error	Over temp.		0.05	0.1		.05		%
Maximum demodulator input	Over temp. range	$\frac{V_R}{2} - 0.5$		$\frac{V_R}{2} + 0.5$	$\frac{V_R}{2} - 0.5$		$\frac{V_R}{2} + 0.5$	V
Demodulator offset voltage	Over temp. range			50			65	mV
Tempco of demodulator offset	Over temp.	0.20	0.25	0.30		0.25		mV/°C
Demodulator input current	Over temp.	− 500	− 300		− 500	− 300		nA
$V_R/2$ accuracy	Over temp.	− 3	± 0.5	+ 3	− 3	± 0.5	+ 3	%
Output amplifier								
Input offset voltage	Over temp.	− 7.5		+ 7.5	− 10		10	mV
Input bias current	Over temp. range	− 500	− 300		− 500	− 300		nA
Input offset current		− 100		100	− 100		100	nA
Gain	$R_L = 10k\Omega$ over temp.	90	108			100		dB
Slew rate			1.5			1.5		V/μsec
Gain bandwidth	$A_V = 1$		1			1		MHz
Output voltage swing	$R_L = 10K$ over temp.	1.5		V+ − 1.5	1.5		V+ − 1.5	V
Output short circuit current				25			25	mA
Oscillator current	Over temp.	0.095	0.12	0.15		0.12		mA/V-V_R

LVDT SIGNAL CONDITIONER NE/SE5520

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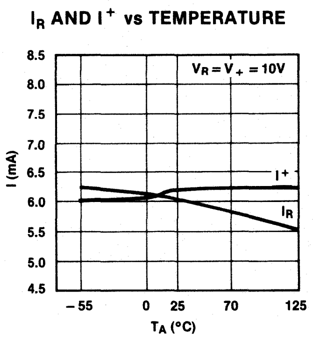
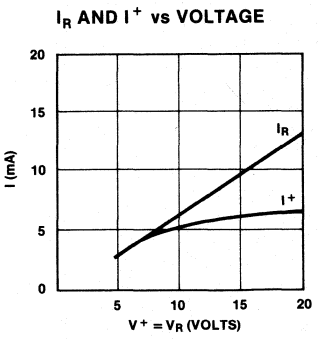
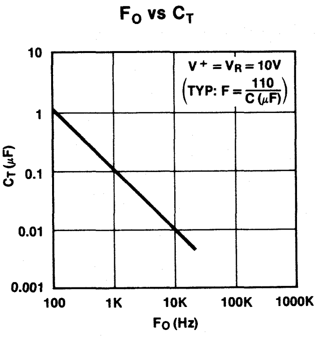
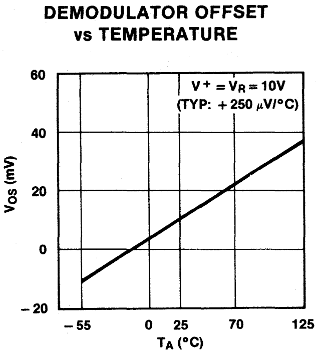
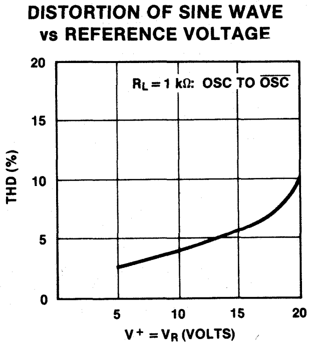
TYPICAL PERFORMANCE CHARACTERISTICS

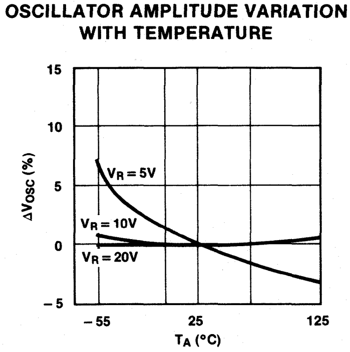

I_R AND I^+ vs TEMPERATURE


I_R AND I^+ vs VOLTAGE


F_O vs C_T


DEMODULATOR OFFSET vs TEMPERATURE


DISTORTION OF SINE WAVE vs REFERENCE VOLTAGE


OSCILLATOR AMPLITUDE VARIATION WITH TEMPERATURE

LVDT SIGNAL CONDITIONER NE/SE5520

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ALL PIN NUMBERS REFER TO N PACKAGE

INTRODUCTION

An LVDT is an electromechanical transducer which makes possible the measurement of very small motion in a structure or mechanical device. Mechanical motion is translated to an electrical signal which contains position information much as a radio frequency carrier contains sound information. The position information from the LVDT is contained in the phase and amplitude of the output AC waveform. In order to remove the position information (demodulation), a system such as is shown in block form in Figure 1 must be used. Once signal demodulation is achieved the position data may be read out on a meter or digital display in addition to being processed by microprocessor or computer. The Signetics NE5520 is a new *Monolithic LVDT Driver-Demodulator* designed to interface with most LVDT's presently being used in the industry.

Uses will range over a large number of potential applications including the accurate measurement of position, pressure, load weight, angular position and even acceleration. Historically, LVDT's have been used in the following applications:

- Load cell
- Linear motion
- Torque cell
- Vibration
- Fluid pressure
- Accelerometer
- Inclinometer
- Seismic load cell

MOTION MAY-BE

- Linear
- Rotary

The NE5520 provides sinusoidal drive to the Linear Variable Differential Transformer (LVDT), the output of which is buffered, rectified and phase demodulated to obtain both direction and displacement information in the form of a DC output signal (Figure 2).

THE LVDT WITH SINEWAVE EXCITATION AND SYNCHRONOUS DEMODULATION

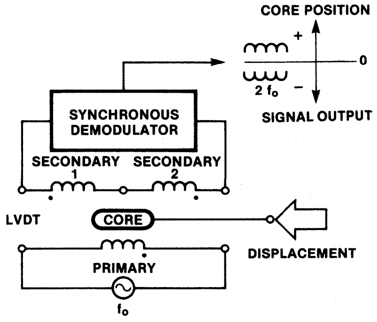


Figure 1

LVDT SYSTEM TRANSFER FUNCTION

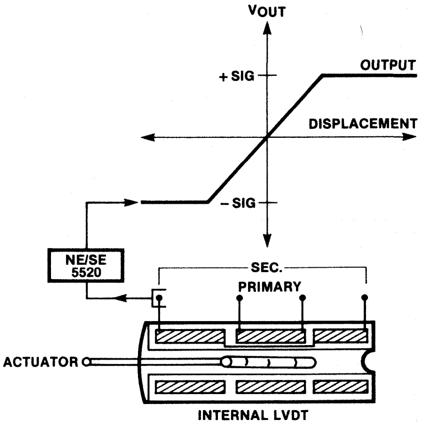


Figure 2

LVDT LOADING

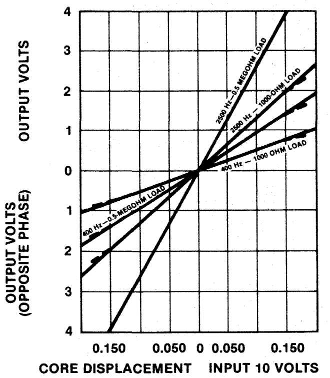
Due to the loosely coupled characteristics of the typical LVDT, loading effects versus frequency may be critical to a successful design. The graph (Figure 3A) shows this relationship in the form of a family of curves relative to LVDT core displacement for 400Hz and 2500Hz. From the curves it is obvious that the linearity and output level versus displacement is superior for an LVDT operated at 2000Hz with a very high impedance load (0.5 meg ohm). The NE/SE5520 demodulator presents a very high input impedance to the LVDT secondary for maximum linearity. (Fig. 3B)

LVDT INTERFACING: SIGNAL CONDITIONING IS REQUIRED

In order to obtain usable information from the LVDT a series of signal conditioning circuit operations are required. First, a stable source of constant frequency excitation voltage must be applied to the primary of the LVDT.

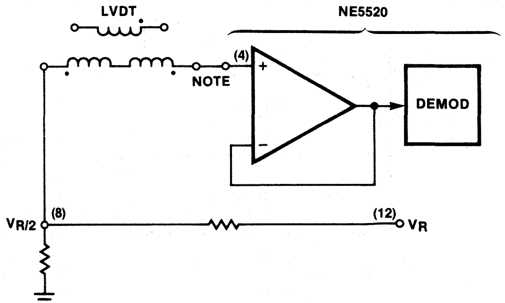
Next some form of demodulator is needed to extract position information from the LVDT secondary output signal. A full wave rectifier will provide usable amplitude information when adequately filtered, however, relative phase information is lacking. In order to obtain both phase and amplitude information synchronous demodulation is needed. This type of demodulator

OUTPUT CHARACTERISTICS OF A TYPICAL LVDT FOR VARIOUS LOADS AND EXCITATION FREQUENCIES



BY PERMISSION SCHAEVITZ ENGINEERING
"HANDBOOK OF MEASUREMENT AND CONTROL" BY HERCEG.

Figure 3a



NOTE: INTERNAL BUFFER AMP PROVIDES HIGH IMPEDANCE LOAD TO SECONDARY.

Figure 3b

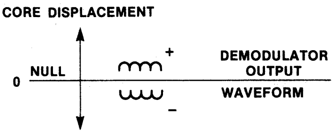


Figure 3c

exists in the Signetics NE5520. Once phase and amplitude information is obtained in the form of a polar full wave rectified signal (see Figure 3C) from the synchronous demodulator, the carrier component (actually 2nd harmonic of the carrier plus higher order spectral components) must be filtered out leaving only the true position information. This is accomplished by passing the demodulated signal through a low-pass active filter. An auxiliary operational amplifier is provided for this purpose within the NE5520, in addition to adjustable signal gain for proper full scale output (span adjustment). In addition, DC offsets are nulled by a simple offset adjustment at the auxiliary amplifier. The resulting system is a complete LVDT signal conditioner. Figure 4 shows a block diagram of the NE5520. The device will operate in a single supply range from 5 to 25 volts DC or with split supplies of ± 5 to ± 12 volts DC. A device current, I_{CC}, of 10 milliamperes at an operating voltage of 10 volts is typical.

DESCRIPTION OF THE NE5520 (Figure 4)

The NE5520 oscillator consists of a triangle wave generator, a current source-sink circuit which switches when the capacitor voltage reaches discrete levels at 1/4 and 3/4 V_{REF}. The total swing being $V_{REF/2}$ volts p-p. The triangle wave is fed into a non-linear load which generates a sinusoidal waveform with low distortion. The sine wave output is then buffered by two op amps, the output of which appear on pins 9 and 10 in phase opposition. This then is the excitation signal for the LVDT primary.

The second major functional portion of the NE5520 is the synchronous demodulator and this section performs full wave rectification in phase synchronism (pin 6) with the above oscillator output. In order to extract true position information, the phase relationship of the LVDT secondary must be obtained. This means that as the LVDT core passes through null an abrupt 180° phase change occurs. Once full wave rectification is accomplished, the resulting signal carrier frequency must be removed by filtering. Demodulator output appears on pin 5. This is accomplished by an active filter incorporating the auxiliary op amp (pins 1, 2, 3). The original position information then appears ripple free on pin 1 of the auxiliary amplifier.

LVDT SIGNAL CONDITIONER NE/SE5520

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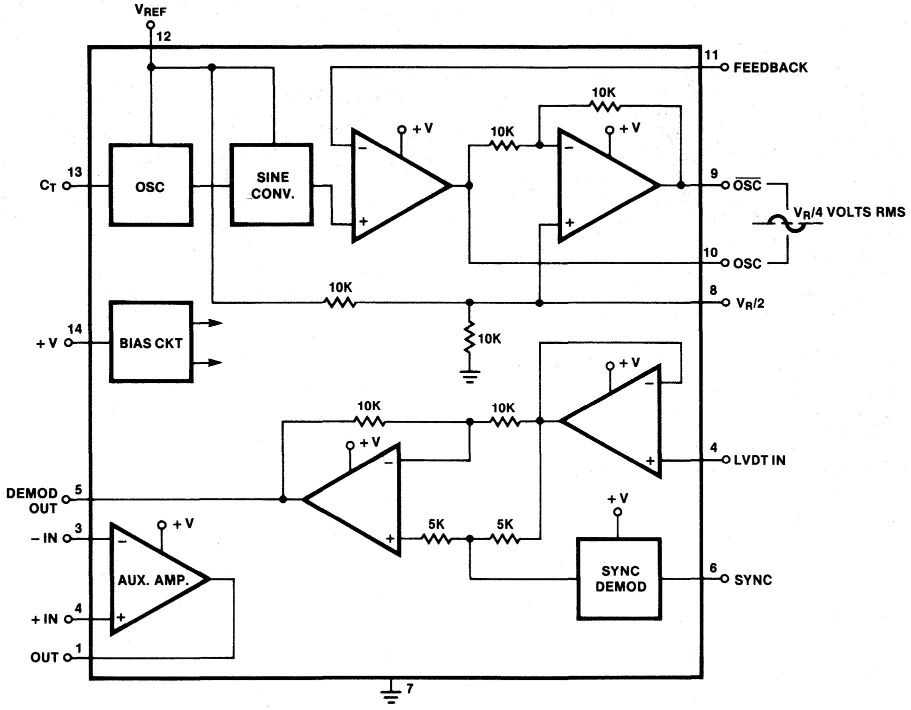
BLOCK DIAGRAM



NOTE:
Pin numbers for for N package.

Figure 4

Other functions include buffer amplifier feedback in the oscillator circuit. The loop is closed with negative feedback around both amplifiers (pin 10 to 11) operating at unity gain.

The oscillator timing capacitor controls the frequency as shown in the graph, Figure 5. The frequency is related by the equation $f_{OSC} = 110/C_{\mu F}$ Absolute output frequency will vary slightly with supply voltage.

BIASING THE REFERENCE V_{REF} (PIN 12)

The manner in which the V_R pin is biased will effect the output voltage function of the NE5520 and consideration must be given to this in order to arrive at an optimum system design. There are two basic modes of operation involved as listed below:

OSCILLATOR FREQUENCY vs CAPACITANCE

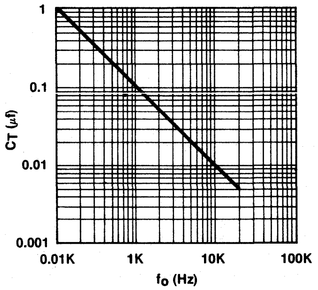


Figure 5

1) Ratiometric
2) Fixed Reference

With the *ratiometric mode*, pin 12 (V_{REF}) is connected to pin 14 (+V). Since V_R controls the DC common mode voltage of the demodulator and the oscillator rms output, these magnitudes will now change with supply voltage. The DC output from pin 1, using a single ground referenced supply, will be ratiometric with the supply voltage and centered within the common mode range of the output amplifier when the LVDT transducer is at null. Single or dual supply operation will be ratiometric when +V is connected to V_R.

The alternate method of biasing is the *fixed reference* mode with pin 12 (V_R) connected to a fixed reference voltage such as +10 volts and pin 14 (+V) allowed to vary with an incoming poorly regulated supply. This might occur in automotive applications where battery voltage may vary from 10 to 14 volts. However, with a fixed reference driving V_R, DC voltage at the output will not vary with supply but will vary within the common mode limits

LVDT SIGNAL CONDITIONER NE/SE5520

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of the amplifier as the LVDT core traverses its path. Output voltage of pin 1 at LVDT null will be $V_R/2$. Thus, for the case mentioned with $V_R = 10$ volts, the null voltage will be +5 volts. The maximum linear swing would be 1.5-8.5 volts around this value. The fixed reference mode may be used with single or dual supply operation.

DUAL SUPPLY OPERATION

When connected to a typical LVDT transducer as shown in Figure 6, the NE5520 will exhibit an extremely linear transfer function. Very important to precision position measurement is the inherent repeatability of the system. The graphs in Figure 7A, B illustrate the highly linear transfer function and its repeatable accuracy with different supply voltages, in this case ± 6 and ± 10 volts. The transducer motion was over a range of ± 150 milli-inches each side of the LVDT null. Typical DC output signal is shown with an output amplifier gain of X10 in both cases. Note that linearity remains constant, however, full scale output varies with supply voltage. This is due to the increased excitor drive to the LVDT with increased supply voltage. LVDT output is a linear function of excitor amplitude on the primary winding. The addition of a single gain control may easily be added between pins 1 and 3 to reduce gain in order to retain constant output for different supply voltages (see Figure 8) or V_R may be connected to a fixed voltage. (See 'Biasing.')

TRANSFER FUNCTION ± 6V

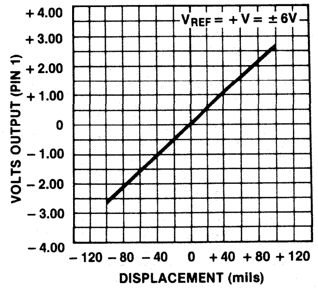

Figure 7a

± 10V

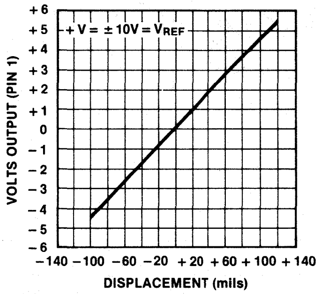

Figure 7b

TYPICAL GAIN ADJUST CIRCUIT

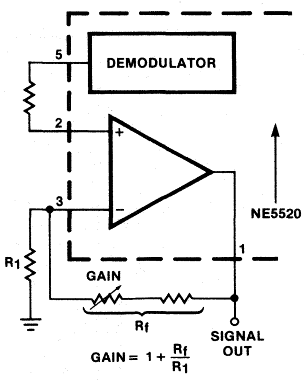

Figure 8

It is strongly recommended that dual output tracking regulated supplies be used in this type of application in order to minimize system DC offset and impaired measurement accuracy due to power supply unbalance. An optional circuit capable of automatically tracking and nulling power supply offset is shown in Figure 9. The bipolar output signal is referenced to ground.

TYPICAL MEASURING SYSTEM (RATIOMETRIC MODE)

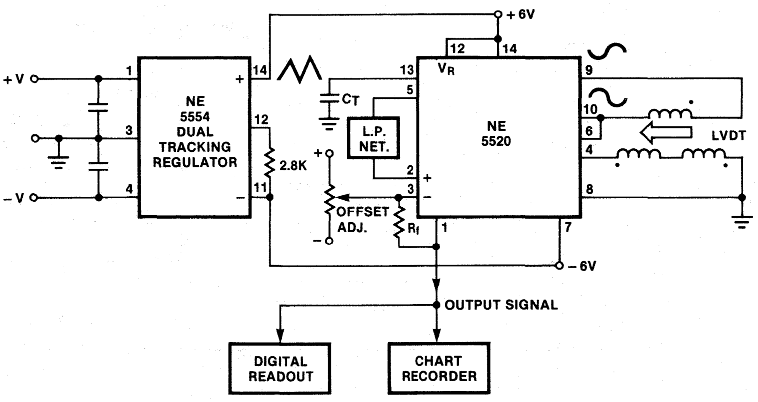

Figure 6

LVDT SIGNAL CONDITIONER NE/SE5520

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AUTO PSRR FOR USE WITH NON-TRACKING SUPPLIES

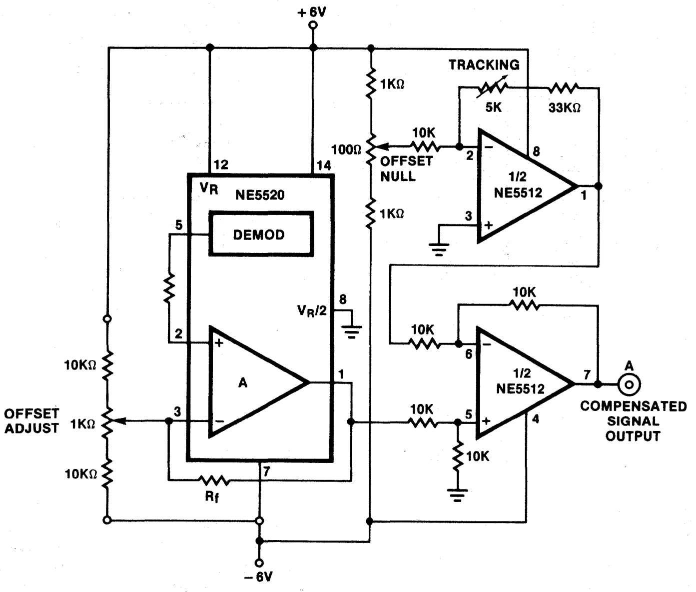

Figure 9

NULLING PROCEDURE (Ref Fig. 9)

1. Null transducer position by observing pin 4 waveform. Set supply voltage for ± 6.00 volts.
2. Set offset adjust pot (feeds pin 3 of NE5520) for 0.00 volts and DC at pin 1 of NE5520.
3. Adjust offset null pot (NE5512) for zero output on Terminal A.
4. Check for equal voltage ± deflection when transducer is displaced equal distances from physical null position.
5. Adjust tracking control for minimum DC output change when either supply is varied over operating range at 'A'.

SINGLE SUPPLY OPERATION

Single ended supply operation requires a different circuit approach to obtain measurement system interface. Figure 10 shows a typical circuit using a single 10-volt supply. Note that the output (pin 1) of the NE5520 is now floating above ground at approximately $V_R/2$. Simple measuring circuits may be realized (Figures 11A, B, C) by placing a DC microammeter between pin 1 and a resistive divider

TYPICAL SINGLE SUPPLY LVDT CIRCUIT

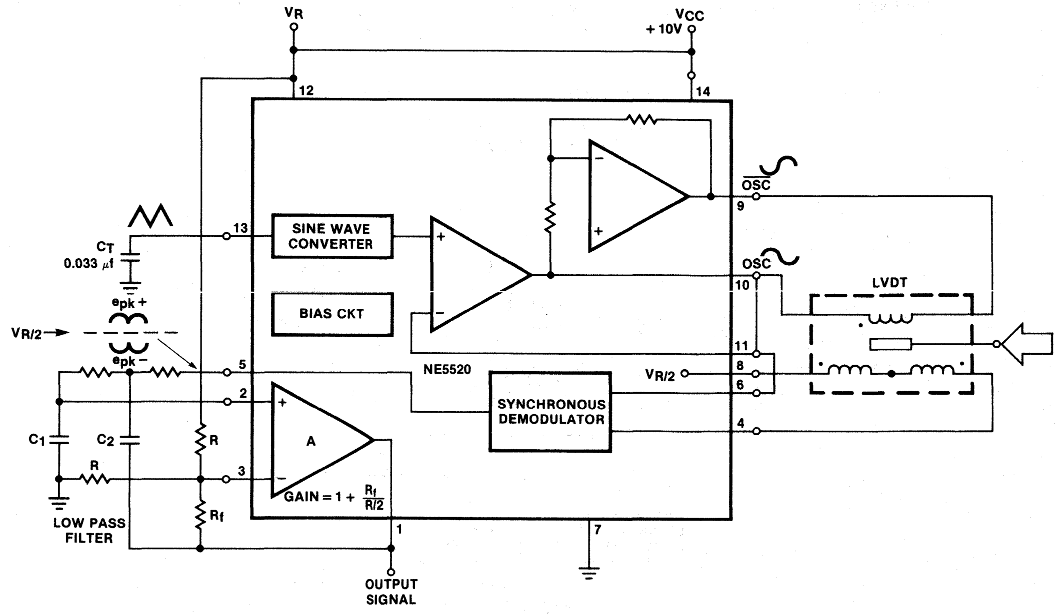

Figure 10

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creating a bridge readout which is ratiometric with supply voltage variations. In case more precision is necessary, a buffer amplifier may be added between the voltage divider or $V_R/2$ and the readout circuit in order to minimize offset due to measuring circuit loading. DC offset due to internal tracking error in the NE5520 may be reduced by using the nulling circuit shown in Figure 12. Offset sensitivity and its effect on system accuracy will be inversely proportional to full scale signal output of the NE5520 which is a function of the DC gain of the auxiliary amplifier and LVDT output. A typical full scale output with 10-volt supply operation is $V_R/2 \pm 3.5$ volts with gain equal to 10.

OUTPUT INTERFACING EXAMPLES

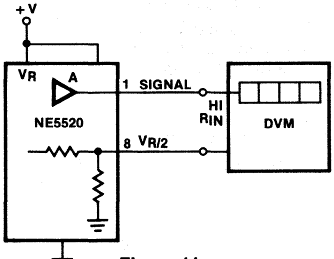


Figure 11a

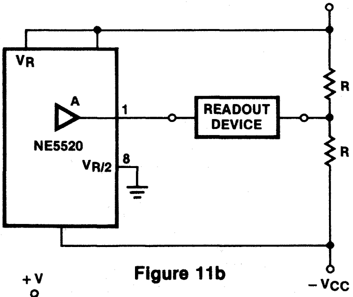


Figure 11b

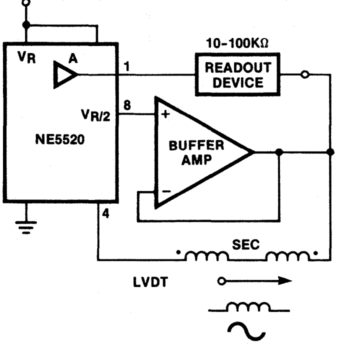


Figure 11c

D.C. OFFSET ADJUST

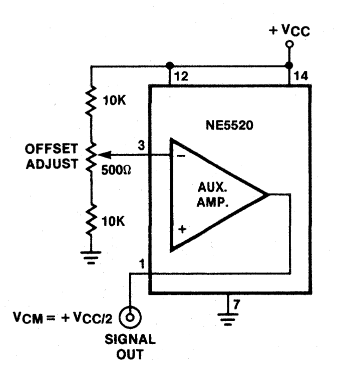


Figure 12

MATCHING THE NE/SE5520 TO LOW IMPEDANCE LVDT's

The NE5520 exciter output is capable of driving LVDT primary windings with a minimum impedance of 1K ohm. When a significantly lower impedance primary is driven by the device some form of step-down impedance matching or a power buffer is recommended. Figure 13 shows a step-down matching transformer approach. A transformer with primary impedance of approximately 1K ohm (audio type) with the proper secondary impedance to match the LVDT primary is used to couple oscillator excitation. Depending on the output efficiency of the LVDT, output signal losses may occur with a corresponding loss in measuring sensitivity. The auxiliary amplifier gain may be increased to offset this loss.

A second approach makes use of a power buffer amplifier constructed from discrete transistors (2N2222, 2N3644). This circuit (Figure 14) results in less signal loss and is inexpensive. A DC decoupling capacitor must be used to prevent DC offset currents from flowing in the LVDT primary winding. A 3dB signal reduction is noted when driving a 15-ohm load to 6 volts peak to peak (10-volt operation); and 12 volts peak to peak for 20-volt supply.

NE5520 TEMPERATURE COMPENSATION

Internal offset voltages originating in the NE5520 synchronous demodulator require external compensation to obtain best measurement accuracy when operating over the full temperature range. The circuits shown (Figures 15A, B) give a simple approach using a thermistor inserted in series with the offset null resistors to reduce voltage drift to a reasonable level. These tolerances are based on ± 3.5 volts full scale output for LVDT displacements each side of physical null. A thermistor having a positive coefficient of +0.7%/°C is used. Obviously, if the total divider resistance is changed a different thermistor resistance will be required.

DRIVING LOW Z LVDT'S WITH THE NE/SE5520

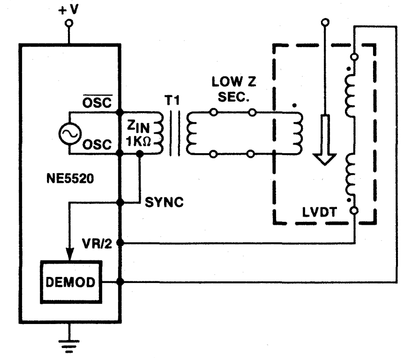
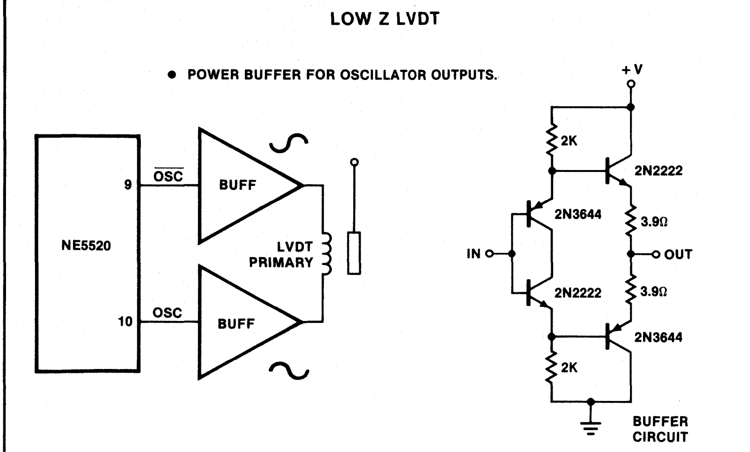


Figure 13

Preliminary


LOW Z LVDT

- POWER BUFFER FOR OSCILLATOR OUTPUTS.

Figure 14

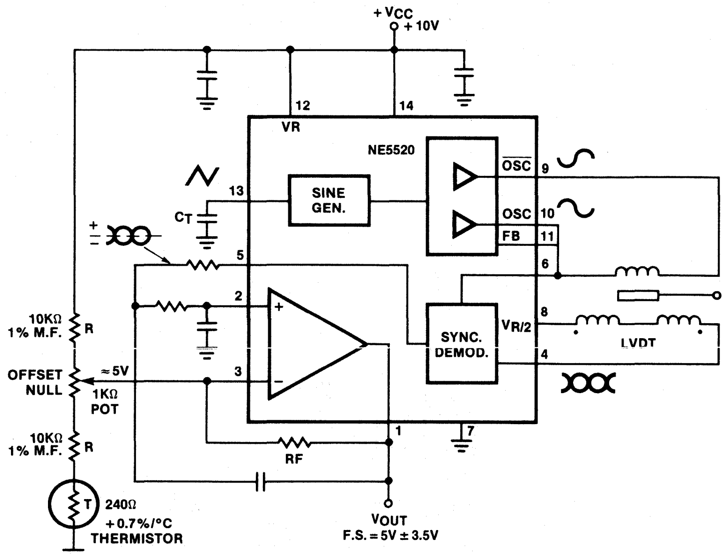
DEMODULATOR DISTORTION (OVERDRIVE)

When the demodulator input exceeds 2 volts peak to peak clipping distortion will increase and must be avoided by controlling oscillator drive to the primary of the LVDT. Figure 16 shows an example of a circuit for attenuating primary excitation using a 1K ohm potentiometer.

The procedure for adjusting the level is simply to:

1. Set LVDT core position for maximum output from the secondary.
2. Monitor the waveform on (pin 5 demodulator output) and adjust oscillator level for the amplitude just below clipping. Normally this should result in a maximum of 2 volts peak to peak at pin 4 of the NE5520 (25°C).

LVDT DRIVER-DEMODULATOR



- WITH TEMPERATURE COMPENSATION 0-70°C

Figure 15a

THERMISTOR TEMPERATURE COMPENSATION

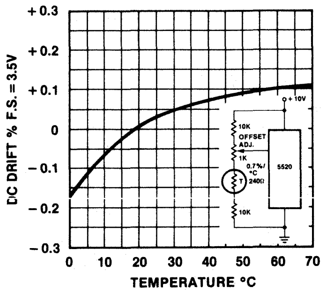
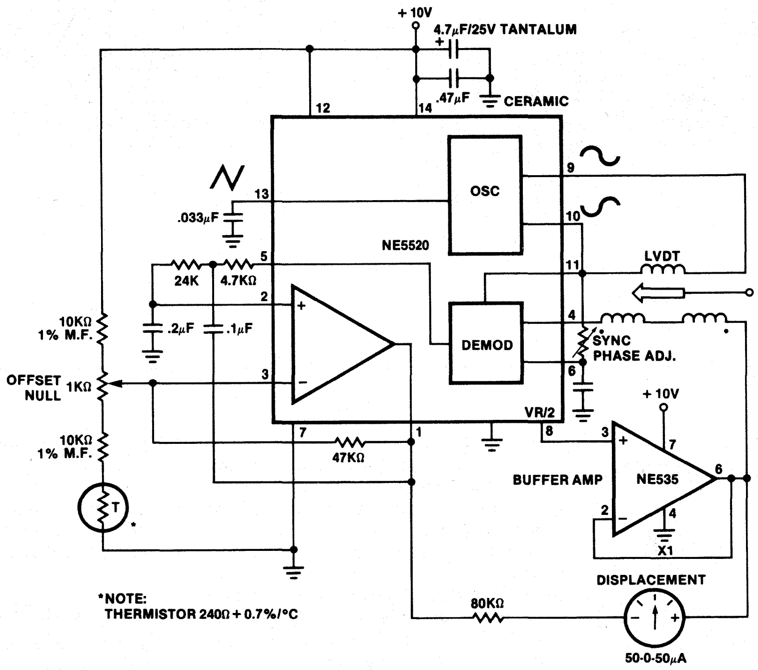


Figure 15b.

Preliminary

LVDT MEASURING GAUGE



*NOTE:
THERMISTOR 240Ω + 0.7%/°C

Figure 19a

NE/SE5520 DEMODULATOR PHASING

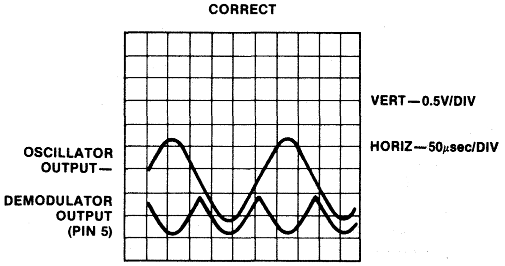


Figure 18a

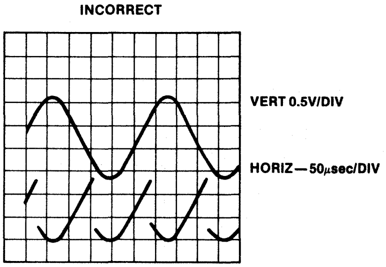


Figure 18b

NE5520 LVDT DRIVER DEMODULATOR APPLICATIONS

OPERATED WITH A SINGLE POWER SUPPLY

The NE5520 may be operated with a single ended power supply ranging from +5 to 25 volts.

A very simple motion transducer may be constructed using the circuit shown in Figure 19A, B. The output is biased to one-half the supply voltage. This requires special interface circuitry for the signal readout. One simple method is to use a zero center meter in a bridge configuration as shown. Displacement now may be measured as a positive or negative meter reading. Readout sensitivity is a function of the particular LVDT and of the gain of the error amplifier. DC offsets may be nulled by using a simple offset adjustment circuit as indicated.

The transducer is centered in its displacement and the *offset adjust* pot set for a zero meter reading. Once this procedure is completed, the circuit is capable of making measurements based on transducer displacement. Displacement sensitivity is a function of the LVDT transducer rated in volts-per-inch in addition to the transfer gain of the NE5520 demodulator. The input excitation is generally a fixed level as is the LVDT transducer transformer ratio. However, the auxiliary gain stage may be used to adjust the overall system sensitivity. This section of the device is also used to obtain a low-pass active filter for the smoothing of demodulator ripple. The design examples use a simple VCVS low-pass filter which allows gain and cut-off frequency to be adjusted independently. Gain equals ten in the example.

Note that using a single supply results in a DC common mode voltage at the output of one-half the reference voltage on pin 12. *This voltage V_R may be equal to but not greater than the supply voltage on pin 14.*

LVDT MEASURING CIRCUIT USING A DUAL SUPPLY

A second mode of operation makes use of dual power supply. A common choice may be ±5, ±6, or ±10 volts. Special consideration must be made in properly biasing the internal circuitry to operate under these conditions. Figure 20 shows a simple design for working with ±6-volt supplies. Special provisions for minimizing DC power supply offsets may be made by using the NE5512 dual op amp as a tracking voltage source and difference amplifier-output buffer (see Figure 9). A second method is to use a dual tracking regulator to supply the NE5520.

LVDT IN CLOSED LOOP SERVO

The LVDT provides an excellent method of obtaining position information for closed loop servo drive systems. Pressure rollers, hydraulic drivers, and motor driven linear motion transducers are a few of the general applications which may benefit from the accuracy and speed of response inherent in the LVDT sensor.

A simple block diagram (Figure 21A) shows one possible application in which the NE5520 with LVDT sensor provides accurate position control in a closed loop servo. Linear motion from millimeters to inches of translational motion are possible using the LVDT technique.

In practice the position voltage may be the output of a D/A converter which in turn is activated digitally from a controlling microprocessor. Keyboard information or software commands are translated directly into mechanical motion (Figure 21B).

Preliminary

LVDT SECONDARY PHASE ANGLE COMPENSATION BY EXCITATION FREQUENCY

The LVDT has a frequency dependent phase shift associated with the particular characteristics of the device and its excitation frequency. This phase shift is in addition to the 180° shift which occurs when passing through null position.

By adjusting the frequency of the sine wave excitation a condition results which causes secondary voltage to be in phase with primary excitation. The adjustment of relative primary and secondary phase angles has several effects. First, if the primary excitation is referenced to the synchronous demodulator, as in the NE5520, optimum rectification occurs at zero phase differential between secondary AC phase and demodulator switching relative to the waveform zero crossings. Second, "Exciting an LVDT at its zero phase angle frequency results in minimum sensitivity to frequency and temperature variations" (Schaevitz Handbook of Measurement and Control, 1976).

DEMODULATOR SYNC PHASE

A second method of phase compensation of the NE5520 versus the LVDT is to use a variable phase shift network between the *oscillator* output and the *sync* input to the NE5520. This is shown in Figure 17. The oscillator frequency remains fixed and the pot is tuned for optimum demodulator phasing.

It is emphasized that an external phasing adjustment as outlined above is not always necessary. Some LVDT's operating in the 1-5kHz range will be near zero phase and will need no phase compensation. Experimental evaluation of the prototype design combined with system specifications will be the best means of making this decision.

Waveform photo in Figure 18A-B, shows the demodulator output signal when phasing of the synchronous demodulator is correct (A) and improperly adjusted (B).

Proper phasing of the sync signal to the demodulator results in optimum sensitivity and linearity.

LIMITING LVDT EXCITATION TO PREVENT DEMODULATOR DISTORTION

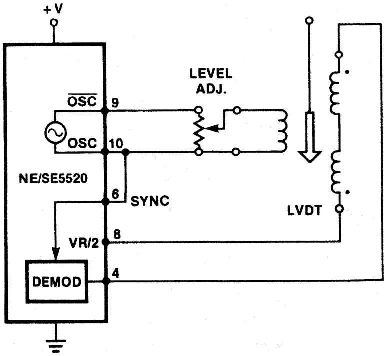
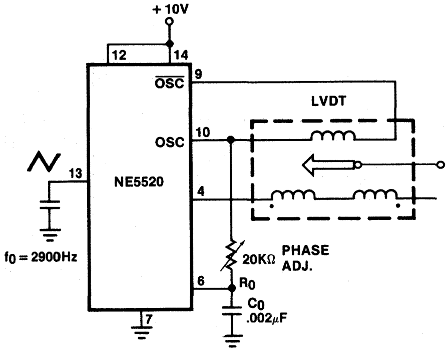


Figure 16

EXTERNAL PHASE ADJUSTMENT

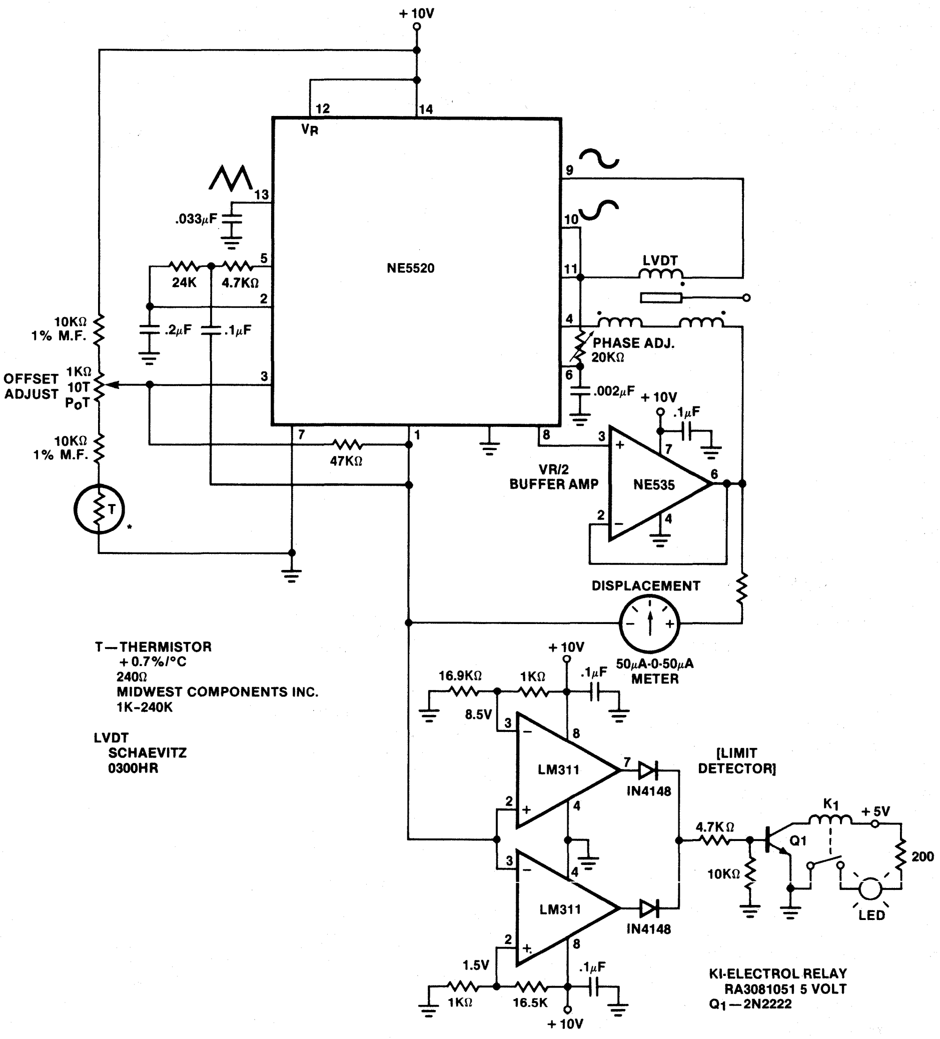


EXAMPLE: $R_0 = 10K\Omega$ $f_0 = 2900Hz$
$C_0 = 2nf$ $\Delta\phi = -\tan^{-1}\omega RC$
$= -20°$

Figure 17

Preliminary

NE5520 LVDT MEASURING CIRCUIT WITH LIMIT DETECTOR



T—THERMISTOR
+0.7%/°C
240Ω
MIDWEST COMPONENTS INC.
1K-240K

LVDT
SCHAEVITZ
0300HR

KI-ELECTROL RELAY
RA3081051 5 VOLT
Q1—2N2222

Figure 19b

LVDT SIGNAL CONDITIONER NE/SE5520

Preliminary

NE5520 LVDT DRIVER-DEMODULATOR $<f_o = 2900Hz>$

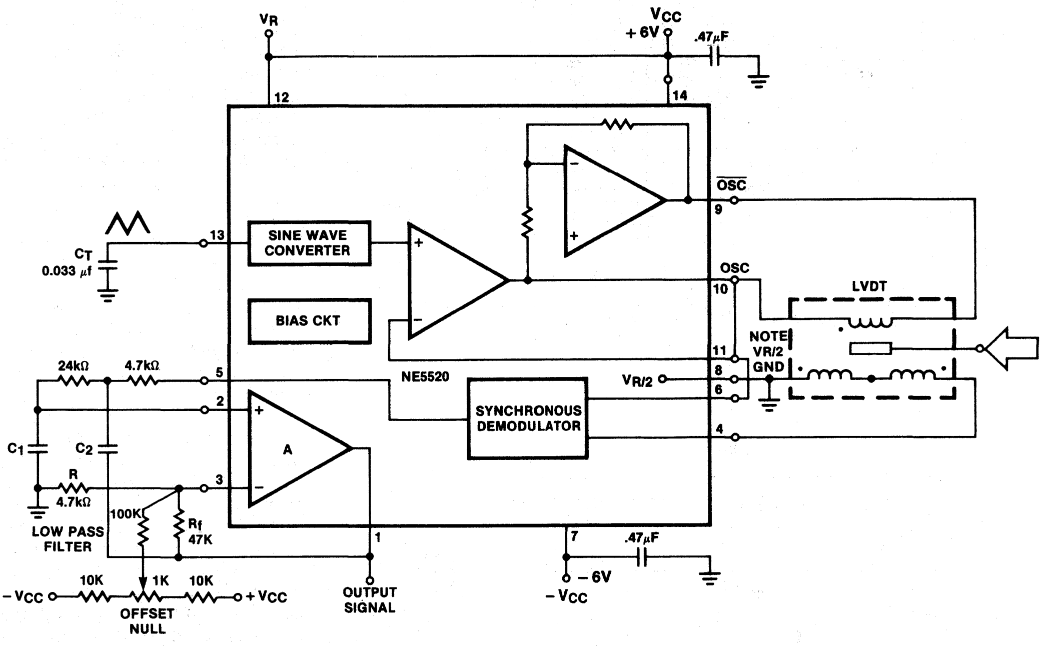


Figure 20

LVDT SIGNAL CONDITIONER NE/SE5520

Preliminary

NE5520 POSITION SERVO WITH LVDT SENSOR

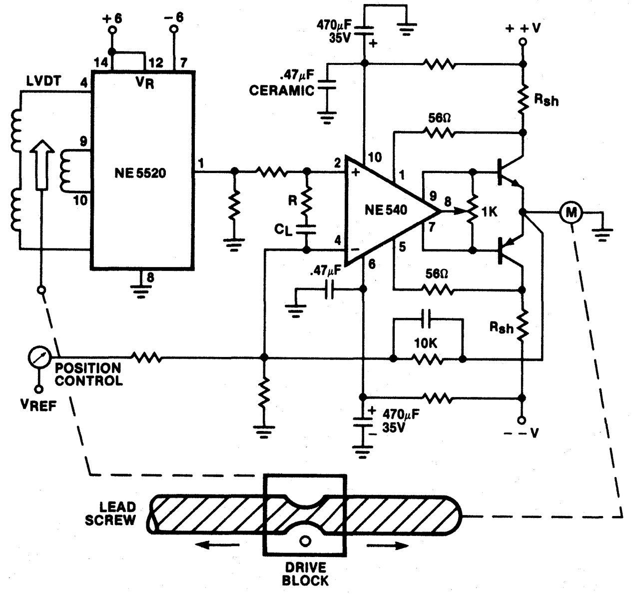


Figure 21a

MICROPROCESSOR CONTROL INTERFACE

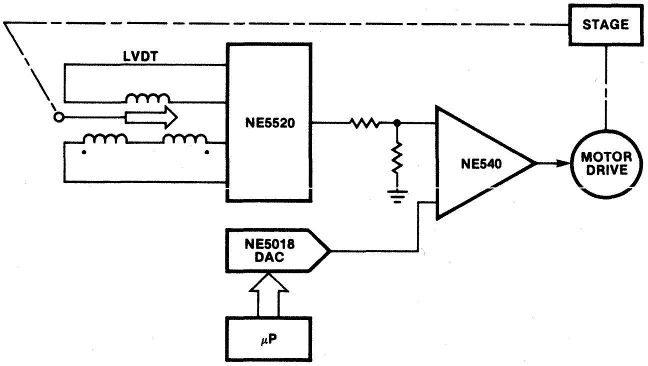


Figure 21b

LVDT SIGNAL TRANSMISSION BY CURRENT LOOP

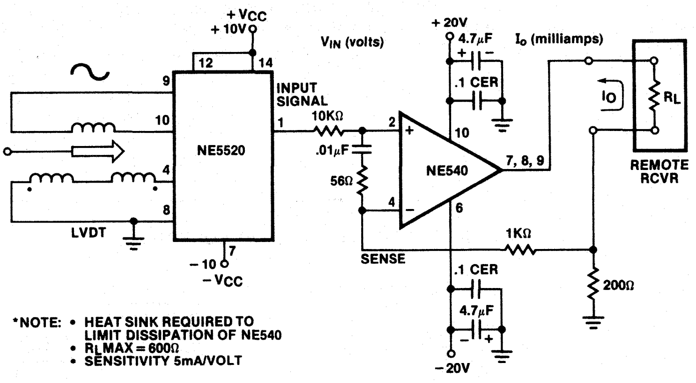
In certain situations the demodulated output signal must be transmitted over long wires or cables before reaching the signal monitoring equipment. The receiver end may consist of chart recorders, digital panel meters and computers or microprocessors. In some systems many LVDT signals must be monitored from different locations thus requiring variable wire length between transmitter and receiver, thus a different line resistance in each case. If voltage feed were used, signal accuracy would be affected by line resistance. This need for accurate signal transmission necessitates the use of a current loop. A current loop develops a current exactly in proportion to the demodulated LVDT output voltage. It is not affected by line resistance within certain limits governed by the current generator.

The conversion to current loop output may facilitate a bipolar output from a dual supply system as in Figure 22. A third method uses the $V_{R/2}$ common mode reference to create a null balance signal circuit which is converted to a bipolar current signal corresponding to the LVDT transducer null (i.e. physical displacement center null position at which zero current occurs). This method is shown in Figure 23 and requires the use of an external dual op amp, half of which is used to provide a buffered reference ($V_{R/2}$) voltage return for the current loop. With $R_2 = 200$ ohms the current loop sensitivity is 5 milliamperes per volt of input signal. In all cases, the current output to the loop receiver will remain constant with fixed input voltage (LVDT demodulator) even for varying line resistance up to 600 ohms. This resistance must include all wire and load drops in the loop. Various full scale current limits require different supply voltages and without external supplies will be limited by op amp swing characteristics. That is in order to force a given current across $R_L + R_2$ results in an ultimate voltage limit from the op amp output in the current converter as total resistance increases.

A fourth method uses an external supply and discrete transistor controlled by the closed loop op amp referenced to shunt resistor R_{SH} in the emitter return circuit. This of course is a unipolar current loop. See Figure 24.

Preliminary

NE5520 LVDT SYSTEM WITH BIPOLAR CURRENT LOOP USING NE540 POWER DRIVER



*NOTE:
- HEAT SINK REQUIRED TO LIMIT DISSIPATION OF NE540
- RL MAX = 600Ω
- SENSITIVITY 5mA/VOLT

Figure 22

NE5520 WITH BIPOLAR CURRENT LOOP OUTPUT ± 10mA F.S. — SINGLE SUPPLY OPERATION

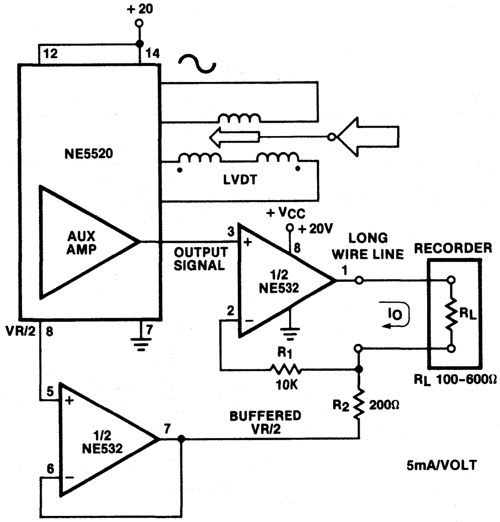


Figure 23

LVDT SIGNAL CONDITIONER NE/SE5520

Preliminary

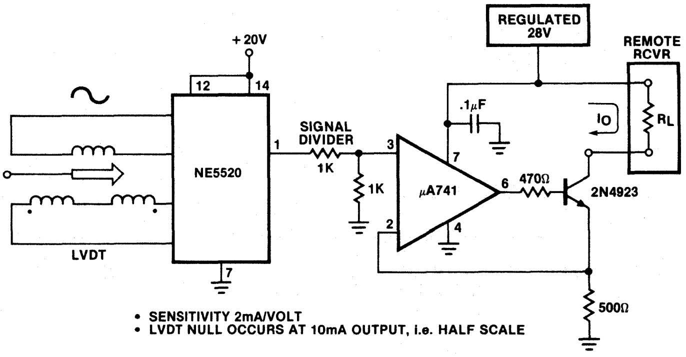
Some systems in common use require two wire source to include both the device operating current and the signal loop current. Thus the quiescent device current must be nulled out at the receiver end leaving the residual signal loop current. The NE5520 is not well suited to this particular design since the device standby current is approximately 10 milliamperes.

A current loop operated from supply voltage sources at the transducer location is a better choice for the operation of an output signal loop where long lines must carry locally generated LVDT signals after demodulation back to the monitor site. Supply voltages in the range from 20 to 48 volts will fill nearly every loop requirement.

POSITIONING THE NE/SE5520 LVDT 3-WIRE REMOTE DRIVER DEMODULATOR SENSING HEAD

The NE5520 may be placed in close proximity to the LVDT transducer provided the environment stays within device specifications. This physical arrangement allows only DC supply and low frequency signal lines (3 wires) being run between the transducer-conditioner unit and the signal processing station as shown in Figure 25.

NE5520 WITH UNIPOLAR CURRENT SOURCE



- SENSITIVITY 2mA/VOLT
- LVDT NULL OCCURS AT 10mA OUTPUT, i.e. HALF SCALE

Figure 24

POSITIONING THE NE/SE5520 LVDT 3 WIRE REMOTE DEMODULATOR SENSING HEAD

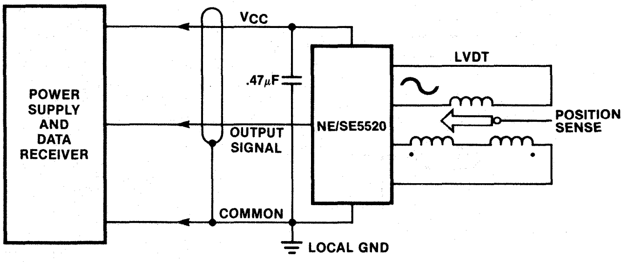


Figure 25

Preliminary

MULTIPLE TRANSDUCER OPERATION — SYNCHRONOUS OSCILLATOR MODE

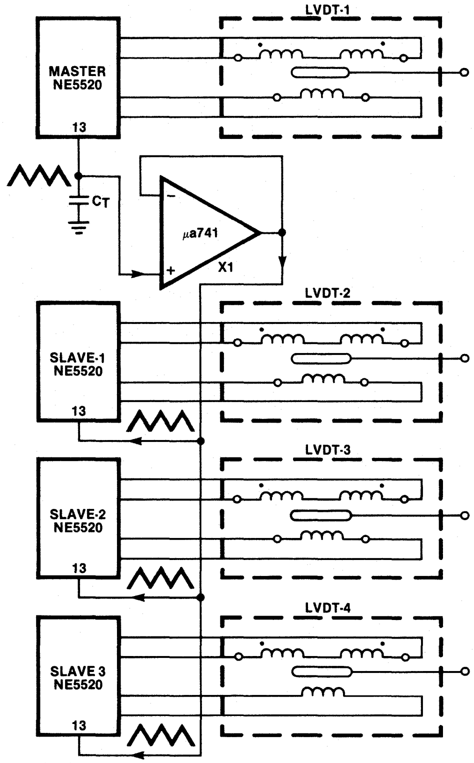


Figure 26

REFERENCES

Handbook of Measurement and Control, Revised Edition 1976, by Edward Herceg, Schaevitz Engineering Publication, Pennsauken, New Jersey.

Handbook of Integrated-Circuit Operational Amplifiers, by George B. Rutkowski, Prentice Hall 1975, Englewood Cliffs, New Jersey.

Signetics Analog Applications Manual, 1979 Edition, Signetics Corporation, Sunnyvale, California.

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Section 8
Comparators

INDEX

ANALOG DIVISION MARCH 1982

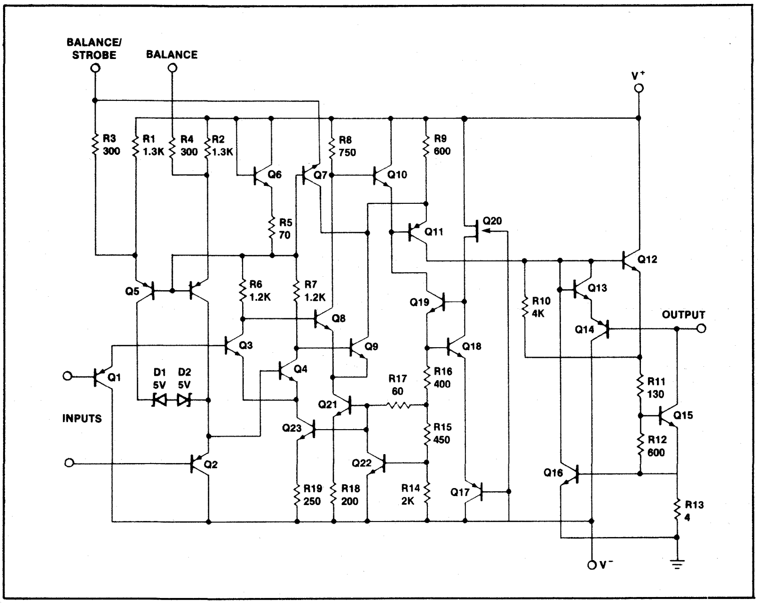
VOLTAGE COMPARATOR LM111/211/311

DESCRIPTION

The LM111 series are voltage comparators that have input currents approximately a hundred times lower than devices like the μA710. They are designed to operate over a wider range of supply voltages; from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Their output is compatible with RTL, DTL, and TTL as well as MOS circuits. Further, they can drive lamps or relays, switching voltages up to 50V at currents as high as 50mA.

Both the inputs and the outputs of the LM111 series can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the μA710 (200ns response time vs 40ns) the devices are also much less prone to spurious oscillations. The LM111 series has the same pin configuration as the μA710 series.

EQUIVALENT SCHEMATIC

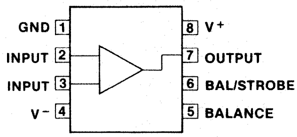


FEATURES

- **Operates from single 5V supply**
- **Maximum input bias current: 150nA (LM311 - 250nA)**
- **Maximum offset current: 20nA (LM311 - 50nA)**
- **Differential input voltage range: ±30V**
- **Power consumption: 135mW at ±15V**
- **High sensitivity—200V/mV**

PIN CONFIGURATIONS

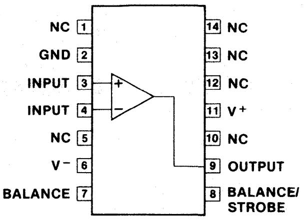
N PACKAGE



TOP VIEW

ORDER NUMBERS
LM211N/LM311N
LM311D

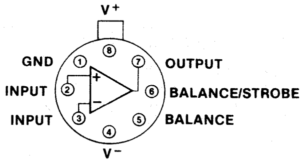
F,N-14 PACKAGE



TOP VIEW

ORDER NUMBERS
LM111F/LM211F/LM211N-14
LM311F/LM311N-14

H PACKAGE*



ORDER NUMBERS
LM111H/LM211H/LM311H

*Metal cans (H) not recommended for new designs

VOLTAGE COMPARATOR LM111/211/311

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Total supply voltage	36	V
Output to negative supply voltage:		
LM111/LM211	50	V
LM311	40	V
Ground to negative supply voltage	30	V
Differential input voltage	±30	V
Input voltage[1]	±15	V
Power dissipation[2]	500	mW
Output short circuit duration	10	sec
Operating temperature range		
LM111	-55 to +125	°C
LM211	-25 to +85	°C
LM311	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 10sec)	300	°C

DC ELECTRICAL CHARACTERISTICS [1,2,3]

PARAMETER	TEST CONDITIONS	LM111/LM211			LM311			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage[4]	$T_A = 25^\circ C$, $R_S \le 50k\Omega$		0.7	3.0		2.0	7.5	mV
Input offset current[4]	$T_A = 25^\circ C$		4.0	10		6.0	50	nA
Input bias current	$T_A = 25^\circ C$		60	100		100	250	nA
Voltage gain	$T_A = 25^\circ C$		200			200		V/mV
Response time[5]	$T_A = 25^\circ C$		200			200		ns
Saturation voltage	$V_{IN} \le -5mV$, $I_{OUT} = 50mA$ $T_A = 25^\circ C$		0.75	1.5		0.75	1.5	V
Strobe on current	$T_A = 25^\circ C$		3.0			3.0		mA
Output leakage current	$V_{IN} \ge 5mV$, $V_{OUT} = 35V$ $T_A = 25^\circ C$, $I_{STROBE} = 3mA$		0.2	10		0.2	50	nA
Input offset voltage[4]	$R_S \le 50k\Omega$			4.0			10	mV
Input offset current[4]				20			70	nA
Input bias current				150			300	nA
Input voltage range			±14			±14		V
Saturation voltage	$V+ \ge 4.5V$, $V- = 0$ $V_{IN} \le -6mV$, $I_{SINK} \le 8mA$		0.23	0.4		0.23	0.4	V
Output leakage current	$V_{IN} \ge 5mV$, $V_{OUT} = 35V$		0.1	0.5				µA
Positive supply current	$T_A = 25^\circ C$		5.1	6.0		5.1	7.5	mA
Negative supply current	$T_A = 25^\circ C$		4.1	5.0		4.1	5.0	mA

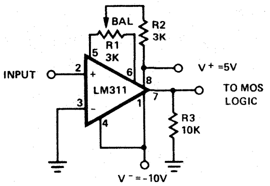
NOTES

1. This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.
2. The maximum junction temperature of the LM311 is 110°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, in the N package, a thermal resistance of 162°C/W, and °C/W for the Ceramic package. The maximum junction temperature of the LM111 is 150°C, while that of the LM211 is 110°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient. The thermal resistance of the Cerdip package is 110°C/W, junction to ambient.
3. These specifications apply for $V_S = \pm15V$ and $0^\circ C < T_A < 70^\circ C$ unless otherwise specified. With the LM211, however, all temperature specifications are limited to $-25^\circ C \le T_A \le 85^\circ C$ and for the LM111 is limited to $-55^\circ C < T_A < 125^\circ C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.
4. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
5. The response time specified (see definitions) is for a 100mV input step with 5mV overdrive.

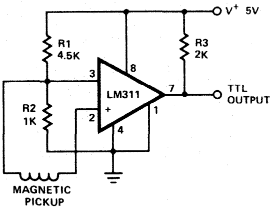
VOLTAGE COMPARATOR LM111/211/311

TYPICAL APPLICATIONS

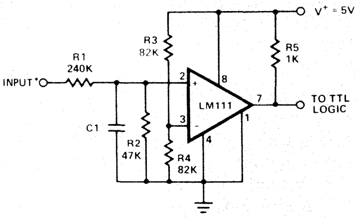
ZERO CROSSING DETECTOR DRIVING MOS LOGIC



DETECTOR FOR MAGNETIC TRANSDUCER



TTL INTERFACE WITH HIGH LEVEL LOGIC



*Values shown are for a 0 to 30V logic swing and a 15V threshold.

†May be added to control speed and reduce susceptability to noise spikes.

DUAL VOLTAGE COMPARATOR LM119/219/319

DESCRIPTION

The LM119 series are precision high speed dual comparators fabricated on a single monolithic chip. They are designed to operate over a wide range of supply voltages down to a single 5V logic supply and ground. Further, they have higher gain and lower input currents than devices like the μA710. The uncommitted collector of the output stage makes the LM119 compatible with RTL, DTL and TTL as well as capable of driving lamps and relays at currents up to 25mA.

Although designed primarily for applications requiring operation from digital logic supplies, the LM119 series are fully specified for power supplies up to ±15V. It features faster response than the LM111 at the expense of higher power dissipation. However, the high speed, wide operating voltage range and low package count make the LM119 much more versatile than older devices like the μA711.

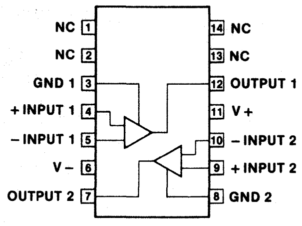
The LM119 is specified from -55°C to +125°C, the LM219 is specified from -25°C to +85°C, and the LM319 is specified from 0°C to +70°C.

FEATURES

- **Two independent comparators**
- **Operates from a single 5V supply**
- **Typically 80ns response time at ±15V**
- **Minimum fan-out of 3 (each side)**
- **Maximum input current of 1μA over temperature**
- **Inputs and outputs can be isolated from system ground**
- **High common mode slew rate**
- **MIL-STD-883 A, B, C available**

PIN CONFIGURATIONS

D,F,N PACKAGE

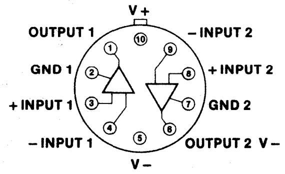


TOP VIEW

ORDER NUMBERS

LM119F,N LM219F,N LM319D,F,N

H PACKAGE*

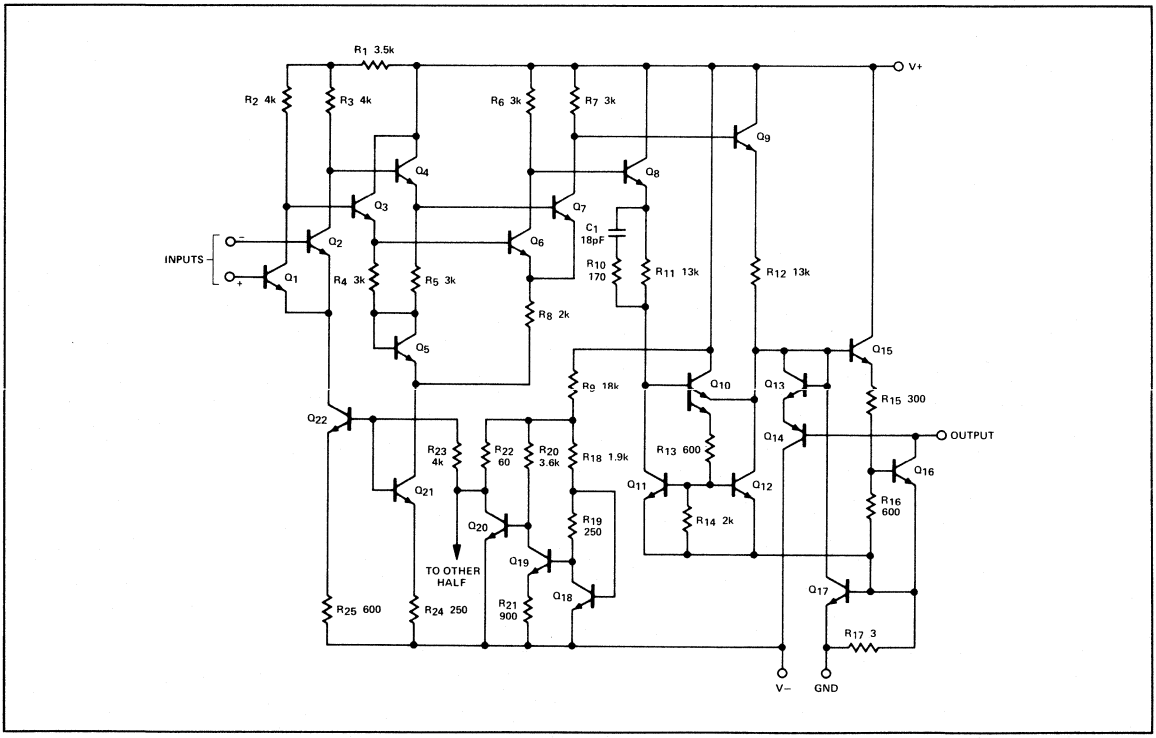


ORDER NUMBERS

LM119H LM219H LM319H

*Metal cans (H) not recommended for new designs

EQUIVALENT SCHEMATIC



DUAL VOLTAGE COMPARATOR LM119/219/319

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Total supply voltage	36	V
Output to negative supply voltage	36	V
Ground to negative supply voltage	25	V
Ground to positive supply voltage	18	V
Differential input voltage	±5	V
Input voltage[1]	±15	V
Power dissipation[2]	500	mW
Output short circuit duration	10	s
Operating temperature range		
LM119	-55 to +125	°C
LM219	-25 to +85	°C
LM319	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 10sec)	300	°C

NOTES

1. For supply voltages less than ±15V, the absolute maximum rating is equal to the supply voltage.
2. The absolute maximum junction temperature is 150°C. Device dissipation must be derated as follows:
   N/K package—150°C/watt above 75°C
   F package —110°C/watt above 95°C

DC ELECTRICAL CHARACTERISTICS

$V_S = \pm15V$, for LM119, $-55°C \le T_A \le 125°C$
LM219, $-25°C \le T_A \le 85°C$
LM319, $0°C \le T_A \le 70°C$
unless otherwise specified.

PARAMETER		TEST CONDITIONS	LM119/219			LM319			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[1,2]	$R_S \le 5K\Omega$, $T_A = 25°C$		0.7	4.0		2.0	8.0	mV
		Over temp.			7			10	mV
I_{OS}	Input offset current[1,2]	$T_A = 25°C$		30	75		80	200	nA
		Over temp.			100			300	nA
I_B	Input bias current[1]	$T_A = 25°C$		150	500		250	1000	nA
		Over temp.			1000			1200	nA
A_V	Voltage gain	$T_A = 25°C$	10	40		8	40		V/mV
V_{OL}	Saturation voltage	$V_{IN} = 5mV$, $I_{OUT} = 25mA$, $T_A = 25°C$		0.75	1.5				V
		$V_{IN} = 10mV$, $I_{OUT} = 25mA$, $T_A = 25°C$					0.75	1.5	V
		$V^+ \ge 4.5V$, $V^- = 0$							
		$V_{IN} = 6mV$, $I_{OUT} = 3.2mA$							
		$T_A \ge 0°C$		0.23	0.4				V
		$T_A \le 0°C$			0.6				
		$V_{IN} = 10mV$, $I_{OUT} = 3.2mA$					0.3	0.4	V
I_{OH}	Output leakage current	$V^- = 0V$, $V_{IN} = 5mV$							
		$V_{OUT} = 35V$, $T_A = 25°C$		0.2	2				µA
		Over temp.		1	10				µA
		$V^- = 0V$, $V_{IN} = 10mV$							
		$V_{OUT} = 35V$, $T_A = 25°C$					0.2	10	µA
V_{IN}	Input voltage range	$V_S = \pm15V$		±13			±13		V
		$V^+ = 5V$, $V^- = 0V$	1		3	1		3	V
V_{ID}	Differential input voltage				±5			±5	V
I^+	Positive supply current	$V^+ = 5V$, $V^- = 0V$, $T_A = 25°C$		4.3			4.3		mA
I^+	Positive supply current	$V_S = \pm15V$, $T_A = 25°C$		8.0	11.5		8.0	12.5	mA
I^-	Negative supply current	$V_S = \pm15V$, $T_A = 25°C$		3.0	4.5		3.0	5.0	mA

NOTES

1. V_{OS}, I_{OS} and I_B specifications apply for a supply voltage range of $V_S = \pm15V$ down to a single 5V supply.
2. The offset voltages and offset currents given are the maximum values required to drive the output to within 1 volt of either supply with a 1mA load. Thus these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

DUAL VOLTAGE COMPARATOR LM119/219/319

AC ELECTRICAL CHARACTERISTICS

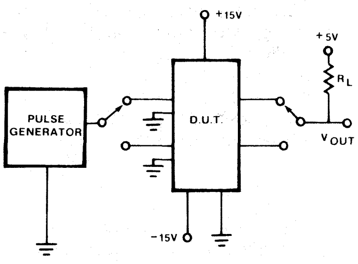
PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Response time*	$V_S = \pm 15V$, $T_A = 25°C$ $R_L = 500\Omega$ (see test figure)		80		ns

*NOTE

The response time specified is for a 100mV step with 5mV overdrive.

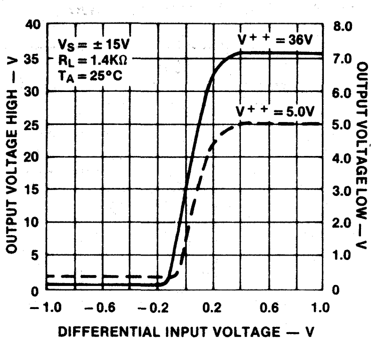
TEST CIRCUIT

RESPONSE TIME MEASUREMENT

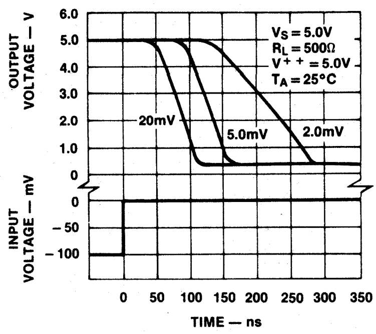


TYPICAL PERFORMANCE CHARACTERISTICS

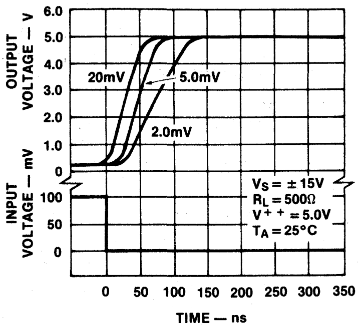
TRANSFER FUNCTION



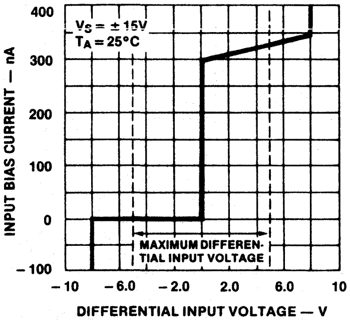
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



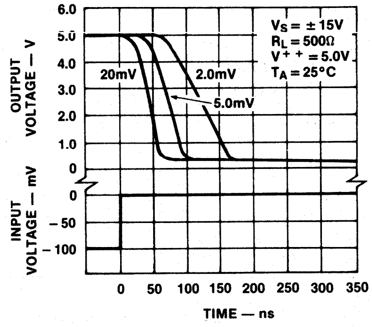
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



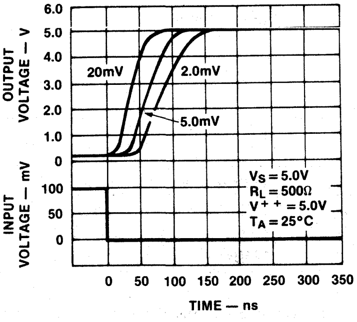
INPUT CHARACTERISTICS



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



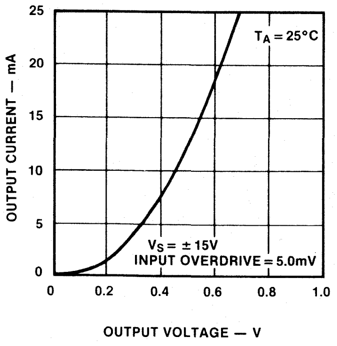
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



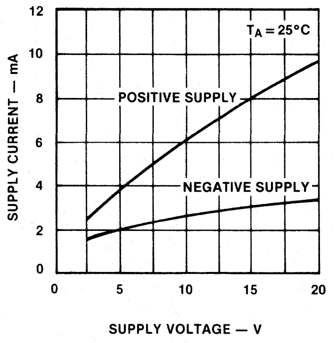
DUAL VOLTAGE COMPARATOR LM119/219/319

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

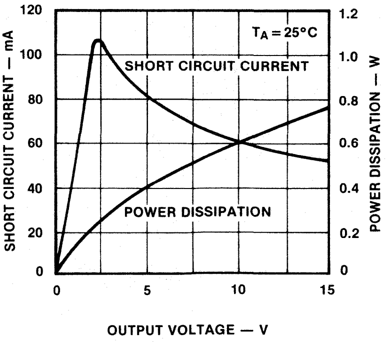
OUTPUT SATURATION VOLTAGE



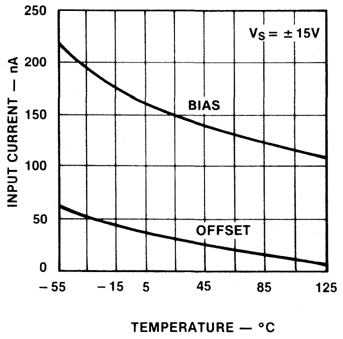
SUPPLY CURRENT



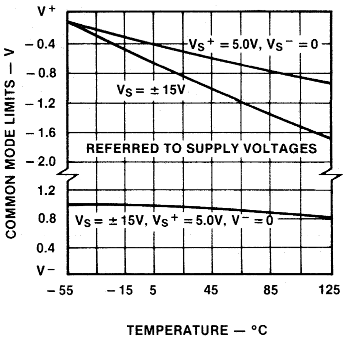
OUTPUT LIMITING CHARACTERISTICS



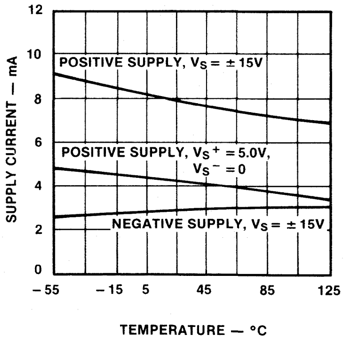
INPUT CURRENTS (LM119/219)



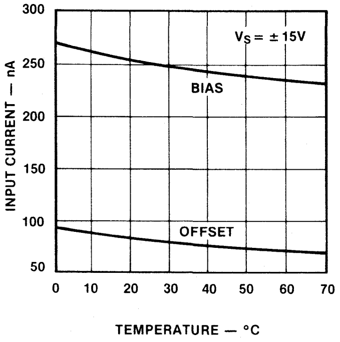
COMMON MODE LIMITS (LM119/219)



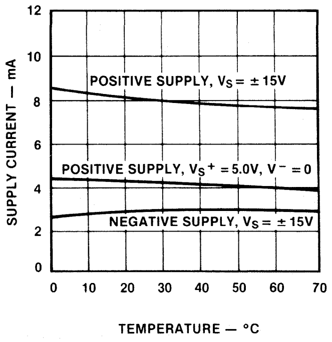
SUPPLY CURRENT (LM119/219)



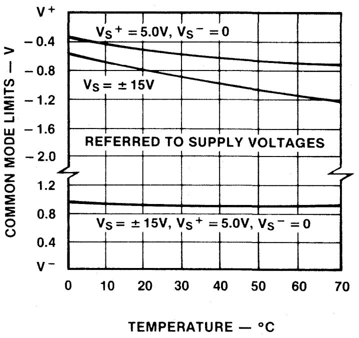
INPUT CURRENTS (LM319)



SUPPLY CURRENTS (LM319)

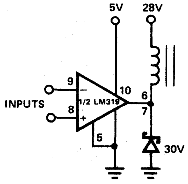


COMMON MODE LIMITS (LM319)

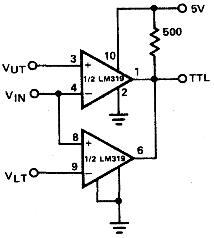


TYPICAL APPLICATIONS

RELAY DRIVER

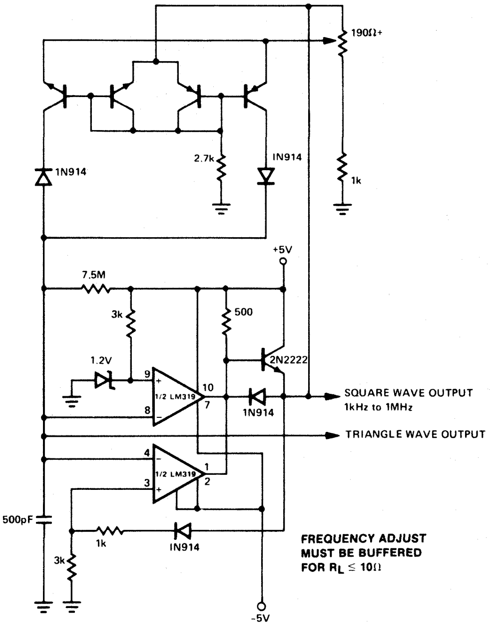


WINDOW DETECTOR



$V_{OUT} = 5V$ for $V_{LT} < V_{IN} < V_{UT}$
$V_{OUT} = 0$ for $V_{IN} < V_{LT}$ or $V_{IN} > V_{UT}$

WIDE RANGE VARIABLE OSCILLATOR



FREQUENCY ADJUST MUST BE BUFFERED FOR $R_L \leq 10\Omega$

QUAD VOLTAGE COMPARATOR

LM139/239/339 MC3302/LM2901

DESCRIPTION

The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2.0mV max for each comparator which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common mode voltage range includes ground, even though operated from a single power supply voltage.

The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM139 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

FEATURES

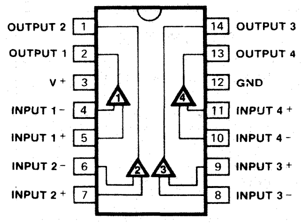
- **Wide single supply voltage range 2.0Vdc to 36Vdc or dual supplies ±1.0Vdc to ±18Vdc**
- **Very low supply current drain (0.8mA) independent of supply voltage (1.0mW/-comparator at 5.0Vdc)**
- **Low input biasing current 25nA**
- **Low input offset currrent ±5nA and offset voltage ±2mV**
- **Input common-mode voltage range includes ground**
- **Differential input voltage range equal to the power supply voltage.**
- **Low output 250mV at 4mA saturation voltage**
- **Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems.**

APPLICATIONS

- **A/D converters**
- **Wide range VCO**
- **MOS clock generator**
- **High voltage logic gate**
- **Multivibrators**

PIN CONFIGURATION

D,F,N PACKAGE



TOP VIEW

ORDER NUMBERS

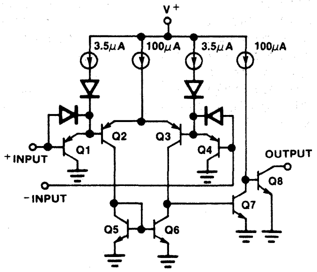
LM139/239/339F,N LM2901F,N
MC3302F,N LM339D

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V_{CC} supply voltage	36 or ±18	
Differential input voltage	36	
Input voltage	-0.3 to +36	
Power dissipation[1]		
Molded DIP	570	mW
CERDIP	900	mW
Output short circuit to ground[2]	Continuous	
Input current (V_{IN} < -0.3Vdc)[3]	50	mA
Operating temperature range		
LM139	-55 to +125	°C
LM239	-25 to +85	°C
LM339	0 to +70	°C
LM2901/MC3302	-40 to +85	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 10 sec.)	300	°C

EQUIVALENT CIRCUIT

(1 Comparator Only)



QUAD VOLTAGE COMPARATOR LM139/239/339 MC3302/LM2901

DC ELECTRICAL CHARACTERISTICS

V+ = 5Vdc, LM139: $-55°C \leq T_A \leq 125°C$ unless otherwise specified
LM239: $-25°C \leq T_A \leq 85°C$ unless otherwise specified
LM339: $0°C \leq T_A \leq 70°C$ unless otherwise specified

PARAMETER	TEST CONDITIONS	LM139			LM239/339			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OS} Input offset voltage[5]	$T_A = 25°C$		±2.0	±5.0		±2.0	±5.0	mV
	Over temp.			9.0			9.0	
V_{CM} Input common mode voltage range[6]	$T_A = 25°C$	0		V+-1.5	0		V+-1.5	V
	Over temp.	0		V+-2.0	0		V+-2.0	
V_{IDR} Differential input voltage[4]	Keep all V_{IN}'s ≥ 0Vdc (or V-if used)			V+			V+	V
I_B Input bias current[7]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range							
	$T_A = 25°C$		25	100		25	250	
	Over temp.			300			400	nA
I_{OS} Input offset current	$I_{IN(+)} - I_{IN(-)}$							
	$T_A = 25°C$		±3.0	±25		±5.0	±50	nA
	Over temp.			±100			±150	nA
I_{OL} Output sink current	$V_{IN(-)} \geq 1$Vdc, $V_{IN(+)} = 0$, $V_O \leq 1.5$Vdc, $T_A = 25°C$	6.0	16		6.0	16		mA
I_{OH} Output leakage current	$V_{IN(+)} \geq 1$Vdc, $V_{IN(-)} = 0$							
	$V_O = 5$Vdc, $T_A = 25°C$		0.1			0.1		nA
	$V_O = 30$Vdc, over temp.			1.0			1.0	μA
I_{CC} Supply current	$R_L = \infty$ on all comparators, $T_A = 25°C$		0.8	2.0		0.8	2.0	mA
A_V Voltage gain	$R_L \geq 15k\Omega$, V+ = 15Vdc $T_A = 25°C$	50	200		50	200		V/mV
V_{OL} Saturation voltage	$V_{IN(-)} \geq 1$Vdc, $V_{IN(+)} = 0$, $I_{SINK} \leq 4$mA							
	$T_A = 25°C$		250	400		250	400	
	Over temp.			700			700	mV
T_{LSR} Large signal response time	V_{IN} = TTL logic swing, $V_{REF} = 1.4$Vdc, $V_{RL} = 5$Vdc, $R_L = 5.1k\Omega$, $T_A = 25°C$		300			300		ns
T_R Response time[8]	$V_{RL} = 5$Vdc, $R_L = 5.1k\Omega$, $T_A = 25°C$		1.3			1.3		μs

NOTES

1. For operating at high temperatures, the LM339/339A, LM2901 and MC3302 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM139/139A/239/239A must be derated on a 150°C maximum junction temperature. The low power dissipation and the "On-Off" characteristics of the outputs keep the chip dissipation very small ($P_D \leq 100$mW), provided the output transistors are allowed to saturate.
2. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA independent of the magnitude of V+.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3Vdc.
4. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than -0.3Vdc (or 0.3Vdc below the magnitude of the negative power supply, if used).
5. At output switch point, $V_O \cong 1.4$Vdc, $R_S = 0\Omega$ with V+ from 5Vdc to 30Vdc; and over the full input common-mode range (0Vdc to V+ -1.5Vdc).
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ -1.5V, but either or both inputs can go to 30Vdc without damage.
7. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
8. The response time specified is for a 100mV input step with a 5mV overdrive. For larger overdrive signals, 300ns can be obtained, see typical performance characteristics section.

DC ELECTRICAL CHARACTERISTICS

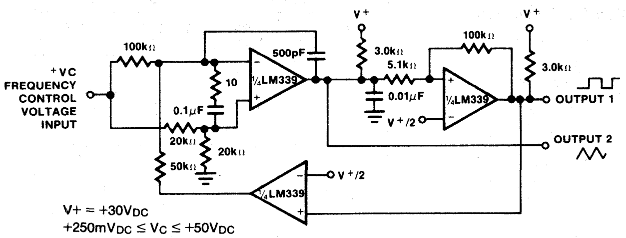
V+ = 15Vdc, MC3302
LM2901/MC3302: -40°C ≤ T_A ≤ 85°C unless otherwise specified

PARAMETER		TEST CONDITIONS	LM2901			MC3302			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[5]	T_A = 25°C Over temp.		±2.0 ±9	±7.0 ±15		±3.0	±20 ±40	mV
V_{CM}	Input common mode voltage range[6]	T_A = 25°C Over temp.	0 0		V+-1.5 V+-2.0			V+-1.5 V+-2.0	V
V_{IDR}	Differential input voltage[4]	Keep all $V_{IN's}$ ≥ 0Vdc (or V-if need)			V+			V+	V
I_B	Input bias current[7]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range T_A = 25°C Over temp.		25 200	250 500		25	500 1000	nA
I_{OS}	Input offset current	$I_{IN(+)} - I_{IN(-)}$ T_A = 25°C Over temp.		±5 ±50	±50 ±200		±5		nA nA
I_{OL}	Output sink current	$V_{IN(-)}$ ≥ 1Vdc, $V_{IN(+)}$ = 0, V_O ≤ 1.5Vdc, T_A = 25°C V_O = 800mV, Over temp.	6.0	16		2.0			mA
I_{OH}	Output leakage current	$V_{IN(+)}$ ≥ 1Vdc, $V_{IN(-)}$ = 0 V_O = 5Vdc, T_A = 25°C V_O = 30V Over temp. V_O = 28V T_A = 25° C		0.1	1.0		0.1	1.0	nA μA
I_{CC}	Supply current	R_L = ∞ on comparators, V+ = 5Vdc, T_A = 25°C V+ = 30V, T_A = 25°C V+ = 5 to 28 Vdc, T_A = 25°C		0.8 1.0	2.0 2.5		0.8	2.0	mA
A_V	Voltage gain	R_L ≥ 15kΩ, V+ = 15Vdc T_A = 25°C	25	100		2	100		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)}$ ≥ 1Vdc, $V_{IN(+)}$ = 0, I_{SINK} ≤ 4mA T_A = 25°C Over temp. I_{SINK} = 2mA, V+ = 5V to 28V, T_A = 25°C		400	400 700		150	400	mV
T_{LSR}	Large signal response time	V_{IN} = TTL logic swing, V_{REF} = 1.4Vdc, V_{RL} = 5Vdc, R_L = 5.1kΩ, T_A = 25°C		300			300		ns
T_R	Response time[8]	V_{RL} = 5Vdc, R_L = 5.1kΩ, T_A = 25°C		1.3			1.3		μs

Notes 1-8, refer to preceding page.

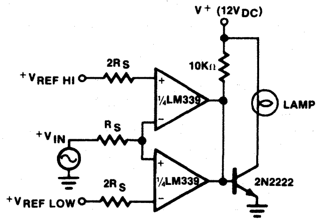
TYPICAL APPLICATIONS

TWO-DECADE HIGH-FREQUENCY VCO

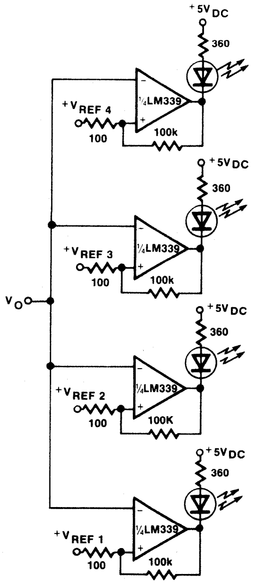


V+ = +30VDC
+250mVDC ≤ VC ≤ +50VDC
700Hz ≤ fO ≤ 100kHz

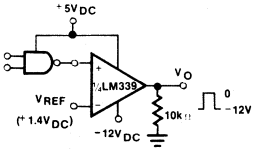
LIMIT COMPARATOR



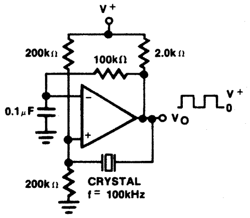
VISIBLE VOLTAGE INDICATOR



TTL TO MOS LOGIC CONVERTER



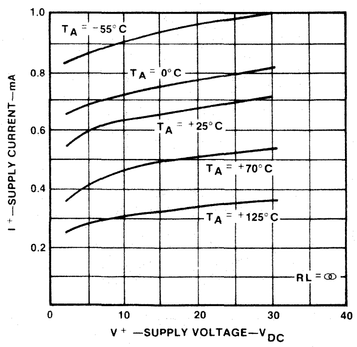
CRYSTAL CONTROLLED OSCILLATOR



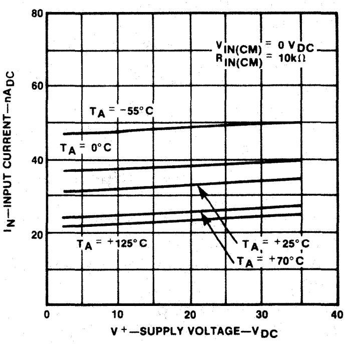
QUAD VOLTAGE COMPARATOR LM139/239/339 MC3302/LM2901

TYPICAL PERFORMANCE CHARACTERISTICS

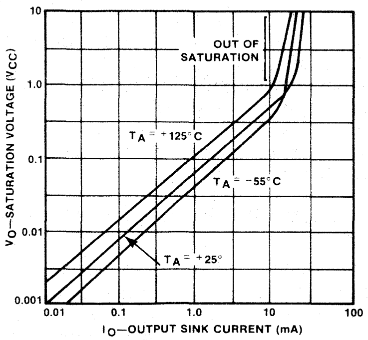
SUPPLY CURRENT



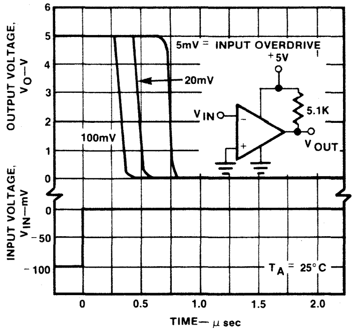
INPUT CURRENT



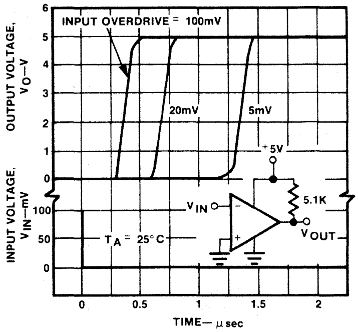
OUTPUT SATURATION VOLTAGE



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES— NEGATIVE TRANSITION



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES— POSITIVE TRANSITION



ANALOG DIVISION MARCH 1982

LOW POWER DUAL VOLTAGE COMPARATOR LM193/A/293/A/393/A/2903

DESCRIPTION

The LM193 series consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common mode voltage range includes ground, even though operated from a single power supply voltage.

The LM193 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM193 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

FEATURES

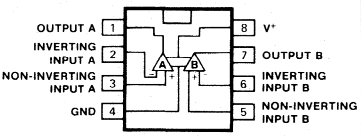
- **Wide single supply voltage range 2.0Vdc to 36Vdc or dual supplies ±1.0Vdc to ±18Vdc**
- **Very low supply current drain (0.8mA) independent of supply voltage (2.0mW/-comparator at 5.0Vdc)**
- **Low input biasing current 25nA**
- **Low input offset current ±5nA and offset voltage ±2mV**
- **Input common-mode voltage range includes ground**
- **Differential input voltage range equal to the power supply voltage.**
- **Low output 250mV at 4mA saturation voltage**
- **Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems.**

APPLICATIONS

- **A/D converters**
- **Wide range VCO**
- **MOS clock generator**
- **High voltage logic gate**
- **Multivibrators**

PIN CONFIGURATIONS

N,FE PACKAGE



TOP VIEW

ORDER NUMBERS

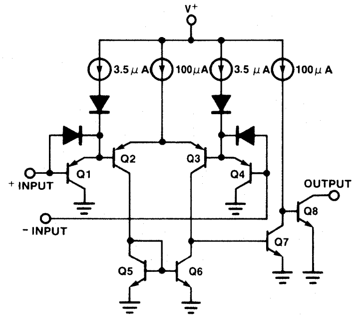
LM193FE
LM293FE
LM293AFE
LM293N
LM293AN
LM393FE
LM393AFE
LM393N
LM393AN
LM2903N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V_{CC} supply voltage	36 or ±18	Vdc
Differential input voltage	36	Vdc
Input voltage	-0.3 to +36	Vdc
Power dissipation[1]		
Molded DIP	570	mW
Metal can	900	mW
Output short circuit to ground[2]	Continuous	
Input current (V_{IN} < -0.3Vdc)[3]	50	mA
Operating temperature range		
LM193/193A	-55 to +125	°C
LM293/293A	-25 to +85	°C
LM393/393A	0 to +70	°C
LM2903	-40 to +85	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 10 sec.)	300	°C

EQUIVALENT CIRCUIT

(One Comparator Only)



DC ELECTRICAL CHARACTERISTICS

V+ = 5Vdc, LM193/193A: −55°C ≤ T_A ≤ +125°C unless otherwise specified.
LM293/293A: −25°C ≤ T_A ≤ +85°C unless otherwise specified.
LM393/393A: 0°C ≤ T_A ≤ +70°C unless otherwise specified.
LM2903: −40°C ≤ T_A ≤ +85°C unless otherwise specified.[7]

PARAMETER	TEST CONDITIONS	LM193A			LM293A/393A			LM2903			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS} Input offset voltage[5]	T_A = 25°C Over temp.		±1.0	±2.0 ±4.0		±1.0	±2.0 ±4.0		±2.0 ±9	±7.0 ±15	mV
V_{CM} Input common mode voltage range[6,10]	T_A = 25°C Over temp.	0 0		V+−1.5 V+−2.0	0 0		V+−1.5 V+−2.0	0 0		V+−1.5 V+−2.0	V
V_{IDR} Differential input voltage[4]	Keep all $V_{IN's}$ ≥ 0Vdc (or V-if need)			V+			V+			V+	V
I_B Input bias current[8]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range T_A = 25°C Over temp.		25	100 300		25	250 400		25 200	250 500	nA
I_{OS} Input offset current	$I_{IN(+)} - I_{IN(-)}$ T_A = 25°C Over temp.		±3.0	±25 ±100		±5.0	±50 ±150		±5 ±50	±50 ±200	nA nA
I_{OL} Output sink current	$V_{IN(-)} \geq$ 1Vdc, $V_{IN(+)}$ = 0, $V_O \leq$ 1.5Vdc, T_A = 25°C	6.0	16		6.0	16		6.0	16		mA
I_{OH} Output leakage current	$V_{IN(+)} \geq$ 1Vdc, $V_{IN(-)}$ = 0 V_O = 30Vdc Over temp. V_O = 5Vdc, T_A = 25°C		0.1	1.0		0.1	1.0		0.1	1.0	µA na
I_{CC} Supply current	R_L = ∞ on both comparators. T_A = 25°C V+ = 30V, over temp.		0.8 1	1 2.5		0.8 1	1 2.5		0.8 1	1 2.5	mA
A_V Voltage gain	$R_L \geq$ 15kΩ, V+ = 15Vdc, T_A = 25°C	50	200		50	200		25	100		V/mV
V_{OL} Saturation voltage	$V_{IN(-)} \geq$ 1Vdc, $V_{IN(+)}$ = 0, $I_{SINK} \leq$ 4mA T_A = 25°C Over temp.		250	400 700		250	400 700		400	400 700	mV
T_{LSR} Large signal response time	V_{IN} = TTL logic swing, V_{REF} = 1.4Vdc, V_{RL} = 5Vdc, R_L = 5.1kΩ, T_A = 25°C		300			300			300		ns
T_R Response time[9]	V_{RL} = 5Vdc, R_L = 5.1kΩ, T_A = 25°C		1.3			1.3			1.3		µs

DC ELECTRICAL CHARACTERISTICS (Cont'd) V+ = 5Vdc, LM193/193A: -55°C ≤ T_A ≤ +125°C unless otherwise specified.

LM293/293A: -25°C ≤ T_A ≤ +85°C unless otherwise specified.
LM393/393A: 0°C ≤ T_A ≤ +70°C unless otherwise specified.
LM2903: -40°C ≤ T_A ≤ +85°C unless otherwise specified.[7]

PARAMETER		TEST CONDITIONS	LM193			LM293/393			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[5]	T_A = 25°C Over temp.		±2.0	±5.0 ±9.0		±2.0	±5.0 ±9.0	mV
V_{CM}	Input common mode voltage range[6,10]	T_A = 25°C Over temp.	0 0		V±-1.5 V±-2.0	0 0		V±-1.5 V±-2.0	V
V_{IDR}	Differential input voltage[4]	Keep all $V_{IN's}$ ≥ 0Vdc (or V-if need)			V+			V+	V
I_B	Input bias current[8]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range T_A = 25°C Over temp.		25	100 300		25	250 400	nA
I_{OS}	Input offset current	$I_{IN(+)} - I_{IN(-)}$ T_A = 25°C Over temp.		±3.0	±25 ±100		±5.0	±50 ±150	nA nA
I_{OL}	Output sink current	$V_{IN(-)}$ ≥ 1Vdc, $V_{IN(+)}$ = 0, V_O ≤ 1.5Vdc, T_A = 25°C	6.0	16		6.0	16		mA
I_{OH}	Output leakage current	$V_{IN(+)}$ ≥ 1Vdc, $V_{IN(-)}$ = 0 V_O = 5Vdc, T_A =25°C V_O = 30Vdc, over temp.		0.1	 1.0		0.1	 1.0	nA μA
I_{CC}	Supply current	R_L = ∞ on both comparators T_A = 25°C V+ = 30V, over temp.		0.8	1 2.5		0.8	1 2.5	mA
A_V	Voltage gain	R_L ≥ 15KΩ, V+ = 15Vdc	50	200		50	200		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)}$ ≥ 1Vdc, $V_{IN(+)}$ = 0, I_{SINK} ≤ 4mA T_A = 25°C Over temp.		250	400 700		250	400 700	mV
T_{LSR}	Large signal response time	V_{IN} = TTL logic swing, V_{REF} = 1.4Vdc, V_{RL} = 5Vdc, R_L = 5.1kΩ, T_A = 25°C		300			300		ns
T_R	Response time[9]	V_{RL} = 5Vdc, R_L = 5.1kΩ, T_A = 25°C		1.3			1.3		μs

NOTES

1. For operating at high temperatures, the LM393/393A and LM2903 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM193/193A/293/293A must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "On-Off" characteristics of the outputs keeps the chip dissipation very small (P_D ≤ 100mW), provided the output transistors are allowed to saturate.
2. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA independent of the magnitude of V+.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3Vdc.
4. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than -0.3Vdc (Vdc below the magnitude of the negative power supply, if used).
5. At output switch point, V_O ≅ 1.4Vdc, R_S = 0Ω with V+ from 5Vdc to 30Vdc; and over the full input common-mode range (0Vdc to V+ -1.5Vdc).
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ -1.5V, but either or both inputs can go to 30Vdc without damage.
7. With the LM293/293A, all temperature specifications are limited to -25°C ≤ T_A ≤ +85°C and the LM393/393A, all temperature specifications are limited to 0°C ≤ T_A ≤ +70°C. The LM2903 is limited to -40°C ≤ T_A ≤85°C.
8. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
9. The response time specified is for a 100mV input step with a 5mV overdrive.
10. For input signals that exceed V_{CC}, only the overdriven comparator is affected. With a 5V supply, V_{IN} should be limited to 25V max., and a limiting resistor should be used on all inputs that might exceed the positive supply.

ANALOG DIVISION MARCH 1982

HIGH SPEED DUAL DIFFERENTIAL COMPARATOR/SENSE AMP NE/SE521

FEATURES

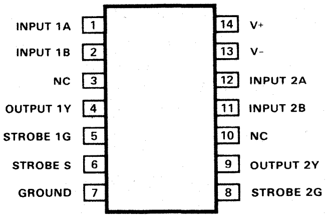
- **12ns maximum guaranteed propagation delay**
- **20μA maximum input bias current**
- **TTL compatible strobes and outputs**
- **Large common mode input voltage range**
- **Operates from standard supply voltages**
- **Military qualifications pending**

APPLICATIONS

- **MOS memory sense amp**
- **A-to-D conversion**
- **High speed line receiver**

PIN CONFIGURATION

D,F,N PACKAGE



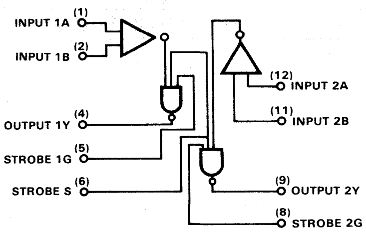
TOP VIEW

ORDER NUMBERS
NE521D,F,N SE521F

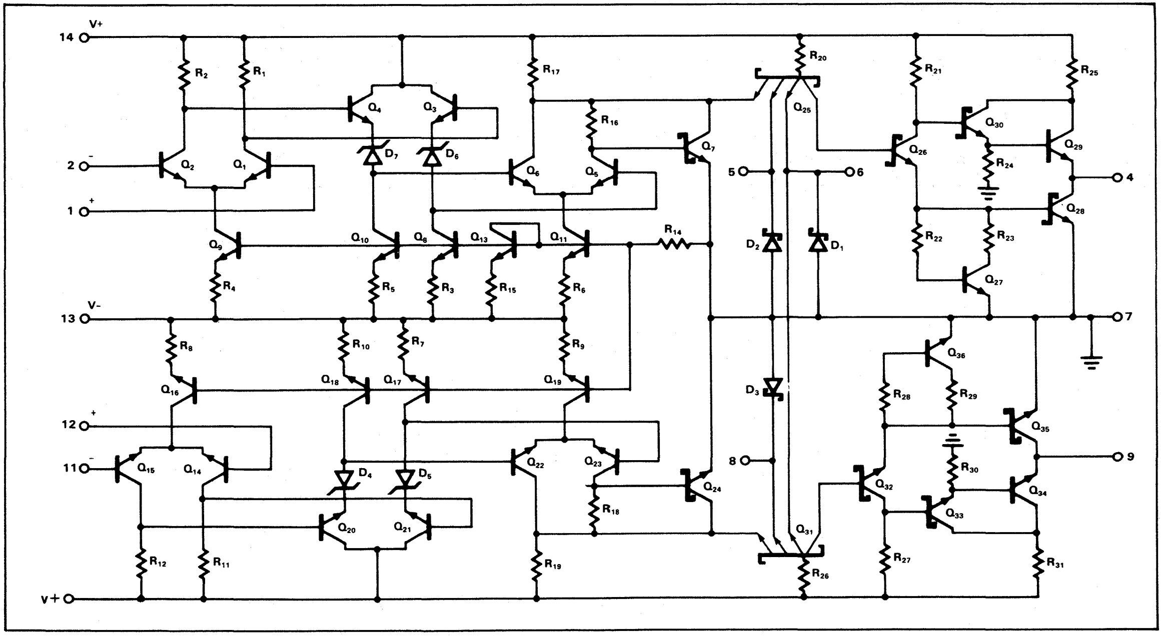
ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
	Supply voltage		V
V+	Positive	+7	
V-	Negative	-7	
V_{IDR}	Differential input voltage	±6	V
V_{IN}	Input voltage		V
	Common mode	±5	
	Strobe/gate	+5.25	
P_D	Power dissipation	600	mW
T_A	Operating temperature range		
	NE521	0 to 70	°C
	SE521	-55 to +125	
T_{stg}	Storage temperature range	-65 to +150	°C
	Lead temperature (solder, 60 sec)	+300	°C

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



HIGH SPEED DUAL DIFFERENTIAL COMPARATOR/SENSE AMP NE/SE521

DC ELECTRICAL CHARACTERISTICS $V+ = +5V$, $V- = -5V$, $T_A = -55$ to $+125°C$ unless otherwise specified

PARAMETER		TEST CONDITIONS	SE LIMITS			UNITS
			Min	Typ	Max	
V_{OS}	Input offset voltage	$V+ = +4.5V$, $V- = -4.5V$				mV
	At 25°C			6	7.5	
	Over temperature range				15	
I_{BIAS}	Input bias current	$V+ = +5.5V$, $V- = -5.5V$				μA
	At 25°C			7.5	20	
	Over temperature range				40	
I_{OS}	Input offset current	$V+ = +5.5V$, $V- = -5.5V$				μA
	At 25°C			1.0	5	
	Over temperature range				12	
V_{CM}	Common mode voltage range	$V+ = +4.5V$, $V- = -4.5V$	±3			V
V_{IL}	Low level input voltage					V
	At 25°C				0.8	
	Over temperature				0.7	
V_{IH}	High level input voltage		2.0			V
	Input current	$V+ = +5.5V$, $V- = -5.5V$				
I_{IH}	High	$V_{IH} = 2.7V$				
		1G or 2G strobe			50	μA
		Common strobe S			100	μA
I_{IL}	Low	$V_{IL} = 0.5V$				
		1G or 2G strobe			-2.0	mA
		Common strobe S			-4.0	mA
	Output voltage	$V_{I(S)} = 2.0V$				V
V_{OH}	High	$V+ = +4.5V$, $V- = -4.5V$, $I_{LOAD} = -1mA$	2.5	3.4		
V_{OL}	Low	$V+ = +4.5V$, $V- = -4.5V$, $I_{LOAD} = 10mA$			0.5	
		$T_A = 25°C$, $I_{LOAD} = 20mA$			0.5	
	Supply voltage					V
$V+$	Positive		4.5	5.0	5.5	
$V-$	Negative		-4.5	-5.0	-5.5	
	Supply current	$V+ = 5.5V$, $V- = -5.5V$, $T_A = 25°C$				mA
I_{CC+}	Positive			27	35	
I_{CC-}	Negative			-15	-28	
I_{SC}	Short circuit output current		-35		-115	mA

HIGH SPEED DUAL DIFFERENTIAL COMPARATOR/SENSE AMP NE/SE521

DC ELECTRICAL CHARACTERISTICS (Cont'd) V+ = +5V, V- = -5V, T_A = 0 to 70°C unless otherwise specified

PARAMETER		TEST CONDITIONS	NE LIMITS			UNITS
			Min	Typ	Max	
V_{OS}	Input offset voltage	V+ = +4.75V, V- = -4.75V				mV
	At 25°C			6	7.5	
	Over temperature range				10	
I_{BIAS}	Input bias current	V+ = +5.25V, V- = -5.25V				μA
	At 25°C			7.5	20	
	Over temperature range				40	
I_{OS}	Input offset current	V+ = +5.25V, V- = -5.25V				μA
	At 25°C			1.0	5	
	Over temperature range				12	
V_{CM}	Common mode voltage range	V+ = +4.75V, V- = -4.75V	±3			V
	Input current	V+ = +5.25V, V- = -5.25V				
I_{IH}	High	V_{IH} = 2.7V				
		1G or 2G strobe			50	μA
		Common strobe S			100	μA
I_{IL}	Low	V_{IL} = 0.5V				
		1G or 2G strobe			-2.0	mA
		Common strobe S			-4.0	mA
	Output voltage	$V_{I(S)}$ = 2.0V				V
V_{OH}	High	V+ = +4.75V, V- = -4.75V, I_{LOAD} = -1mA	2.7	3.4		
V_{OL}	Low	V+ = +5.25V, V- = -5.25V, I_{LOAD} = 20mA			0.5	
	Supply voltage					V
V+	Positive		4.75	5.0	5.25	
V-	Negative		-4.75	-5.0	-5.25	
	Supply current	V+ = 5.25V, V- = -5.25V, T_A = 25°C				mA
I_{CC+}	Positive			27	35	
I_{CC-}	Negative			-15	-28	
I_{SC}	Short circuit output current		-40		-100	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, R_L = 280Ω C_L = 15pF V+ = +5V V- = -5V

PARAMETER		FROM INPUT	TO OUTPUT	LIMITS			UNIT
				Min	Typ	Max	
Large Signal Switching Speed							
	Propagation delay						ns
$t_{PLH(D)}$	Low to high[1]	Amp	Output		8	12	
$t_{PHL(D)}$	High to low[1]	Amp	Output		6	9	
$t_{PLH(S)}$	Low to high[2]	Strobe	Output		4.5	10	
$t_{PHL(S)}$	High to low[2]	Strobe	Output		3.0	6	
	Maximum operating frequency			40	55		MHz

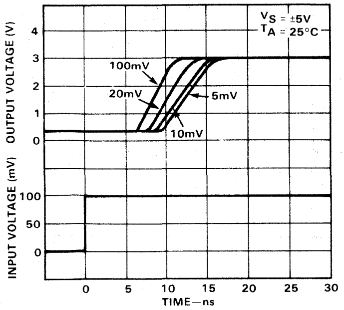
NOTES

1. Response time measured from 0V point of ±100mV p-p 10MHz square wave to the 1.5V point of the output
2. Response time measured from 1.5V point of input to 1.5V point of the output

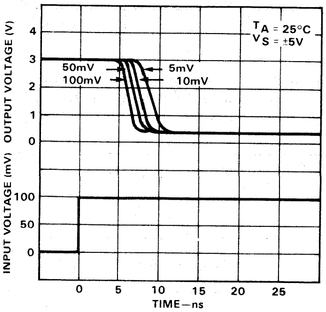
HIGH SPEED DUAL DIFFERENTIAL COMPARATOR/SENSE AMP NE/SE521

TYPICAL PERFORMANCE CHARACTERISTICS

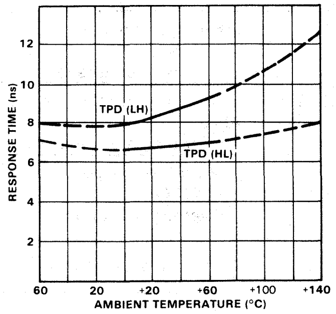
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



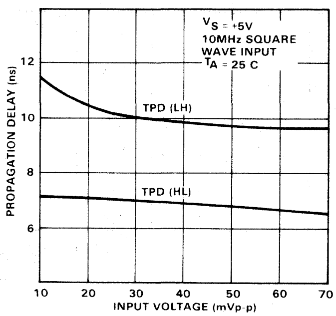
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



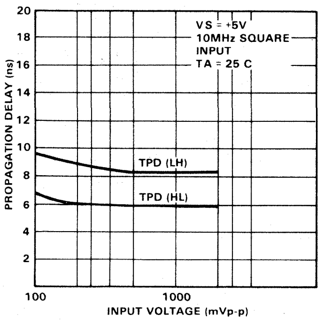
RESPONSE TIME vs TEMPERATURE



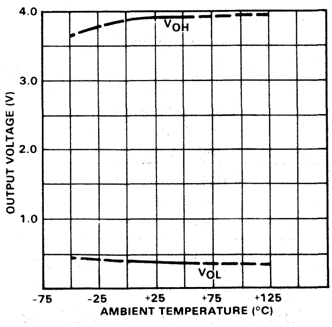
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGE



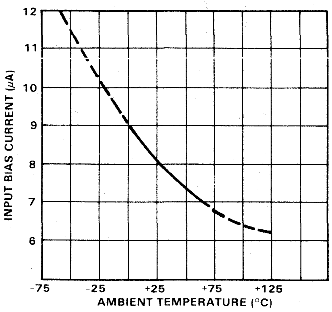
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



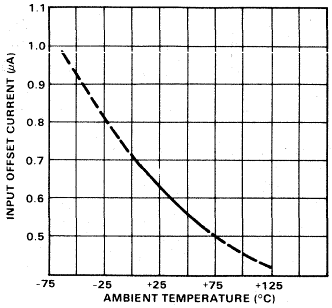
OUTPUT VOLTAGE vs AMBIENT TEMPERATURE



INPUT BIAS CURRENT vs AMBIENT TEMPERATURE



INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE



ANALOG DIVISION MARCH 1982

HIGH SPEED DUAL DIFFERENTIAL COMPARATOR/SENSE AMP NE/SE522

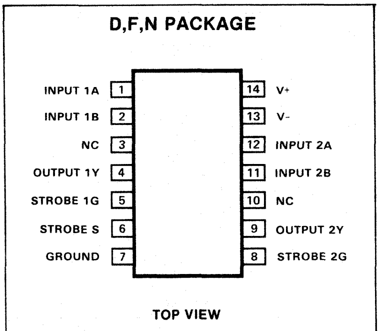
FEATURES

- **15ns maximum guaranteed propagation delay**
- **20μA maximum input bias current**
- **TTL compatible strobes and outputs**
- **Open collector output for wire-OR'd applications**
- ***Large common mode input voltage range***
- **Operates from standard supply voltages**

APPLICATIONS

- **MOS memory sense amp**
- **A-to-D conversion**
- **High speed line receiver**

PIN CONFIGURATION

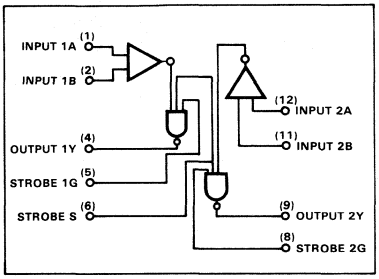


ORDER NUMBERS
NE522D,F,N SE522F

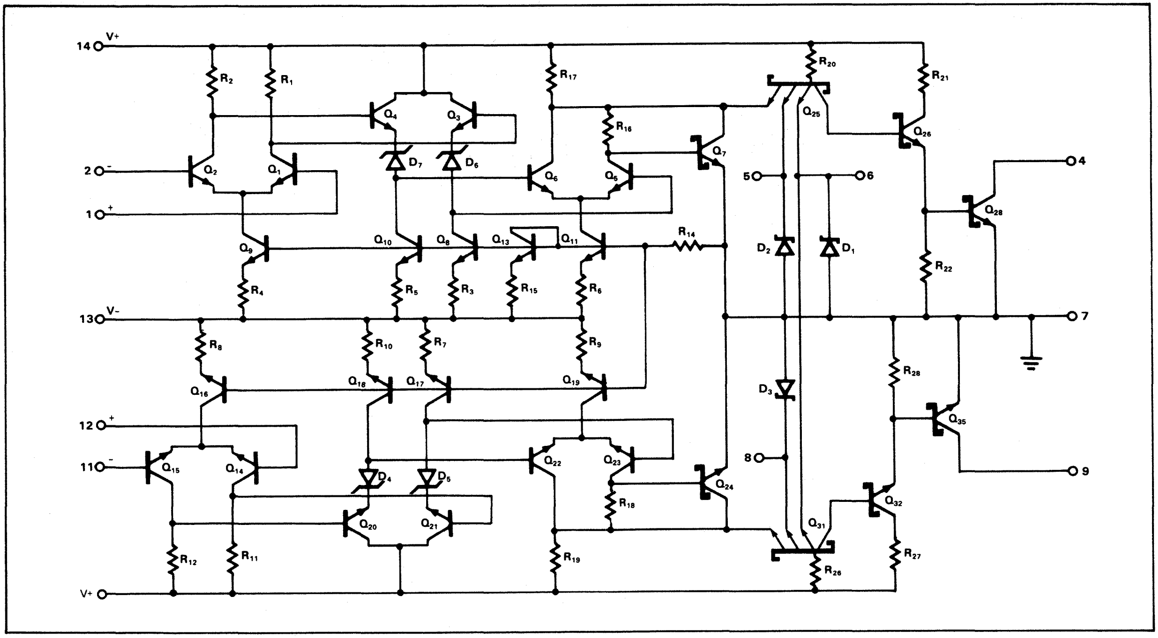
ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
	Supply voltage		V
V+	Positive	+7	
V-	Negative	-7	
V_{IDR}	Differential input voltage	±6	V
V_{IN}	Input voltage		V
	Common mode	±5	
	Strobe/gate	±5.25	
P_D	Power dissipation	600	mW
T_A	Operating temperature range NE	0 to 70	°C
	SE	-55 to +125	
T_{stg}	Storage temperature range	-65 to +150	°C
	Lead temperature (solder, 60 sec)	+300	°C

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



HIGH SPEED DUAL DIFFERENTIAL COMPARATOR/SENSE AMP NE/SE522

DC ELECTRICAL CHARACTERISTICS ±5V ±10%, T_A = -55 to 125°C unless otherwise specified

PARAMETER		TEST CONDITIONS	SE LIMITS			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage	V+ = +4.5V, V- = -4.5V				mV
	At 25°C			6	7.5	
	Over temperature range				15.	
I_{BIAS}	Input bias current	V+ = +5.5V, V- = -5.5V				μA
	At 25°C			7.5	20.	
	Over temperature range				40.	
I_{OS}	Input offset current	V+ = +5.5V, V- = -5.5V				μA
	At 25°C			1.0	5.	
	Over temperature range				12.	
V_{CM}	Common mode voltage range	V+ = +4.5V, V- = -4.5V	±3			V
V_{IL}	Low level input					V
	Voltage at 25°C				.08	
	over temperature				.07	
V_{IH}	High level temperature		2.0			V
	Input current	V+ = +5.5V, V- = -5.5V				
I_{IH}	High	V_{IH} = 2.7V				
		1G or 2G strobe			50	μA
		Common strobe S			100	μA
I_{IL}	Low	V_{IL} = 0.5V				
		1G 2G strobe			-2	mA
		Common strobe S			-4	mA
	Output voltage					V
V_{OL}	Low	V+ = +4.5V, V- = -4.5V				
		I_{OL} = 20mA, T_A = 25°C			.5	
		I_{OL} = 10mA			.5	
	Output current					μA
I_{OH}	High	V_{CC+} = +4.5, V_{CC-} = -4.5V, V_{OH} = 5.5V			250	
	Supply voltage					V
V+	Positive		4.5	5.0	5.5	
V-	Negative		-4.5	-5.0	-5.5	
	Supply current	V+ = 5.5V, V- = -5.5V				mA
I_{CC+}	Positive			27	35	
I_{CC-}	Negative			-15	– 28	

DC ELECTRICAL CHARACTERISTICS (Cont'd) ±5V ±5%, T_A = 0 to 70°C unless otherwise specified

PARAMETER		TEST CONDITIONS	NE LIMITS			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage	V+ = +4.75V, V- = -4.75V				mV
	At 25°C			6	7.5	
	Over temperature range				10	
I_{BIAS}	Input bias current	V+ = +5.25V, V- = -5.25V				µA
	At 25°C			7.5	20	
	Over temperature range				40	
I_{OS}	Input offset current	V+ = +5.25V, V- = -5.25V				µA
	At 25°C			1.0	5	
	Over temperature range				12	
V_{CM}	Common mode voltage range	V+ = +4.75V, V- = -4.75V	±3			V
	Input current	V+ = +5.25V, V- = -5.25V				
I_{IH}	High	V_{IH} = 2.7V				
		1G or 2G strobe			50	µA
		Common strobe S			100	µA
I_{IL}	Low	V_{IL} = 0.5V				
		1G 2G strobe			-2.0	mA
		Common strobe S			-4.0	mA
	Output voltage	V+ = +5.25V, V- = -5.25V, $V_{I(S)}$ = 2.0V				V
V_{OL}	Low	I_{LOAD} = 20mA			0.5	
	Output current					µA
I_{OH}	High	V_{CC+} = +4.75,				
		V_{CC-} = -4.75V, V_{OH} = 5.25V			250	
	Supply voltage					V
V+	Positive		4.75	5.0	5.25	
V-	Negative		-4.75	-5.0	-5.25	
	Supply current	V+ = 5.25V, V- = -5.25V, T_A = 25°C				mA
I_{CC+}	Positive			27	50	
I_{CC-}	Negative			-15	-28	

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, R_L = 280Ω, C_L = 15pF

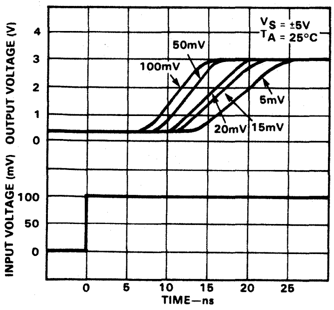
PARAMETER		FROM INPUT	TO OUTPUT	LIMITS			UNIT
				Min	Typ	Max	
	Input resistance				4		kΩ
	Input capacitance				3		pF
Large Signal Switching Speed							
	Propagation delay						ns
$t_{PLH(D)}$	Low to high[1]	Amp	Output		10	15	
$t_{PHL(D)}$	High to low[1]	Amp	Output		8	12	
$t_{PLH(S)}$	Low to high[2]	Strobe	Output		6	13	
$t_{PHL(S)}$	High to low[2]	Strobe	Output		5	9	
	Maximum operating frequency			25	35		MHz

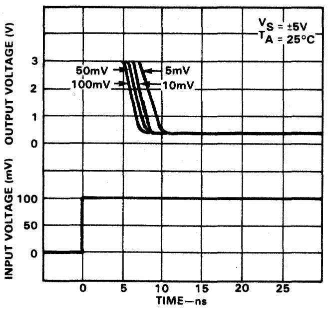
NOTES

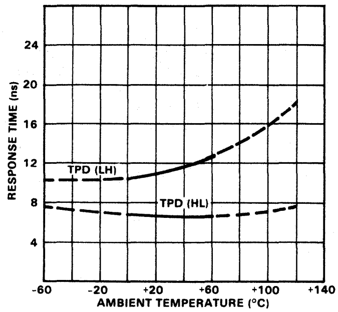
1. Response time measured from 0V point of ±100mV p-p 10MHz square wave to the 1.5V point of the output
2. Response time measured from 1.5V point of input to 1.5V point of the output

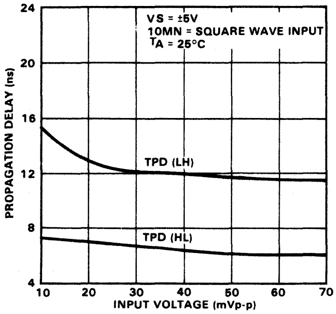
HIGH SPEED DUAL DIFFERENTIAL COMPARATOR/SENSE AMP NE/SE522

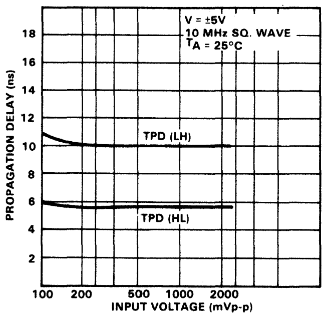
TYPICAL PERFORMANCE CHARACTERISTICS

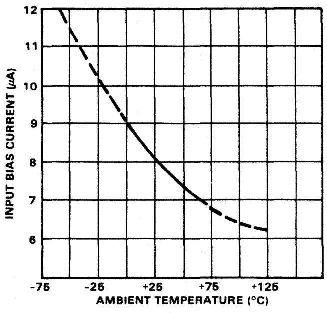

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

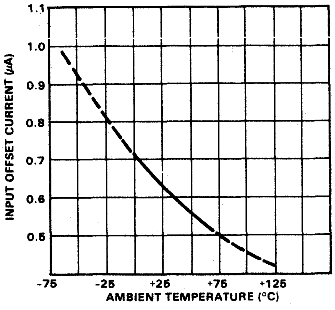

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES


RESPONSE TIME vs TEMPERATURE


PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES


PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES


INPUT BIAS CURRENT vs AMBIENT TEMPERATURE


INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE

VOLTAGE COMPARATOR

NE/SE527

DESCRIPTION

The SE/NE527 is a high speed analog voltage comparator which, in the first time mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed T2L gates with a precision linear amplifier on a single monolithic chip. The SE/NE527 is similar in design to the Signetics SE/NE529 voltage comparator except that it incorporates a "Emitter Follower" input stage for extremely low input currents. This opens the door to a whole new range of applications for analog voltage comparators.

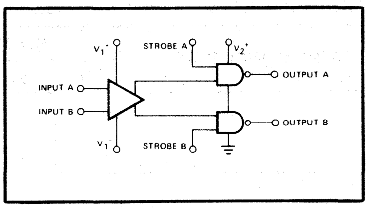
FEATURES

- **15ns propagation delay**
- **Complementary output gates**
- **TTL or ECL compatible outputs**
- **Wide common mode and differential voltage range**
- **Mil std 883A,B,C available**

APPLICATIONS

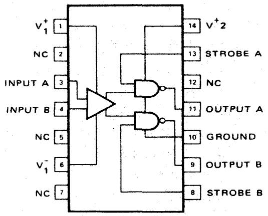
- **A/D conversion**
- **ECL to TTL interface**
- **TTL to ECL interface**
- **Memory sensing**
- **Optical data coupling**

BLOCK DIAGRAM



PIN CONFIGURATIONS

D,F,N PACKAGE

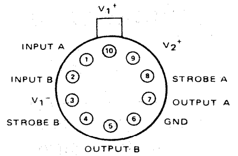


TOP VIEW

ORDER NUMBERS

NE527D,N,F SE527N,F

H PACKAGE *

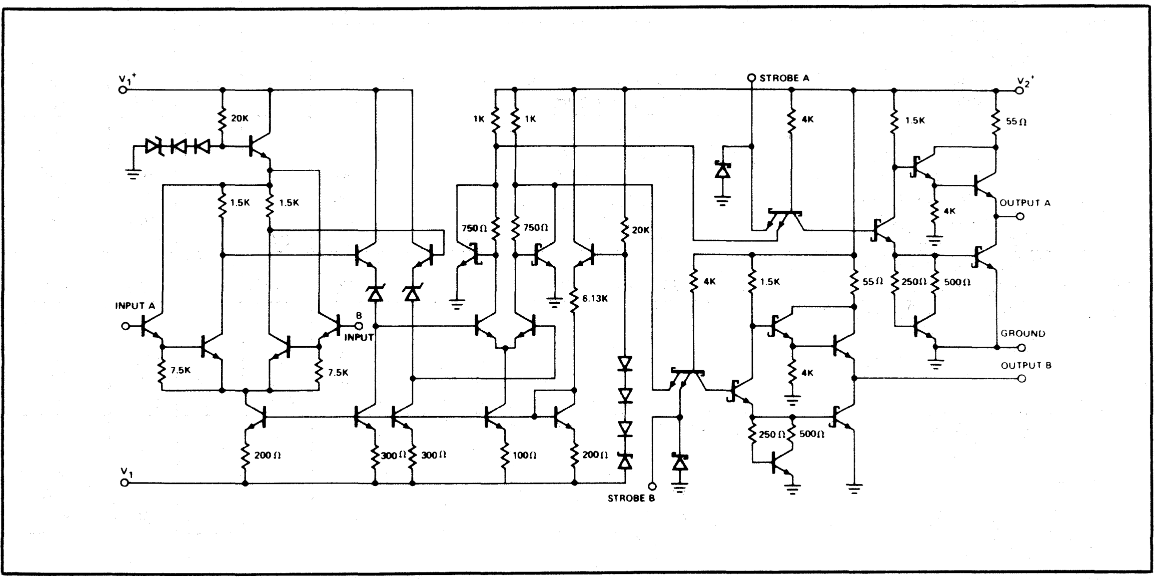


ORDER NUMBERS

NE/SE527H

*Metal cans (H) not recommended for new designs

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive supply voltage (V1+)	+15	V
Negative supply voltage (V1-)	-15	V
Gate supply voltage (V2+)	+7	V
Output voltage	+7	V
Differential input voltage	±5	V
Input common mode voltage	±6	V
Power dissipation	600	mW
Operating temperature range		
NE527	0 to +70	°C
SE527	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	+300	°C

DC ELECTRICAL CHARACTERISTICS $V_1^+ = 10V$, $V_1^- = -10V$, $V_2^+ = +5.0V$

PARAMETER	TEST CONDITIONS	SE527			NE527			UNIT
		Min	Typ	Max	Min	Typ	Max	
INPUT CHARACTERISTICS								
Input offset voltage @ 25°C				4			6	mV
Over temperature range				6			10	mV
Input bias current @ 25°C				2			2	μA
Over temperature range				4			4	μA
Input offset current @ 25°C				0.5			0.75	μA
Over temperature range	$V_{IN} = 0V$			1			1	μA
GATE CHARACTERISTICS								
Output voltage								
"1" State	$V_2^+ = 4.75V$, $I_{SOURCE} = -1mA$	2.5	3.3		2.7	3.3		V
"0" State	$V_2^+ = 4.75V$, $I_{SINK} = 10mA$			0.5			0.5	V
Strobe inputs								
"0" Input current[1]	$V_2^+ = 5.25V$, $V_{STROBE} = 0.5V$			-2			-2	mA
"1" Input current @ 25°C[1]	$V_2^+ = 5.25V$, $V_{STROBE} = 2.7V$			50			100	μA
Over temperature range	$V_2^+ = 5.25V$, $V_{STROBE} = 2.7V$			200			200	μA
"0" Input voltage	$V_2^+ = 4.75V$			0.8			0.8	V
"1" Input voltage	$V_2^+ = 4.75V$	2.0			2.0			V
Short circuit								
Output current	$V_2^+ = 5.25V$, $V_{OUT} = 0V$	-18		-70	-18		-70	mA
POWER SUPPLY REQUIREMENTS								
Supply voltage								
V_1^+		5		10	5		10	V
V_1^-		-6		-10	-6		-10	V
V_2^+		4.5	5	5.5	4.75	5	5.25	V
Supply current	$V_1^+ = 10V$, $V_1^- = -10V$							
	$V_2^+ = 5.25V$							
I_1^+	Over temp.			5			5	mA
I_1^-	Over temp.			10			10	mA
I_2^+	Over temp.			20			20	mA

NOTES

1. Strobe input current test conditions

INPUT A (V_{IN})	INPUT B		STROBE A	STROBE B
> V Offset	GND	Measure	IIL	IIH
< V Offset	GND	Measure	IIH	IIL

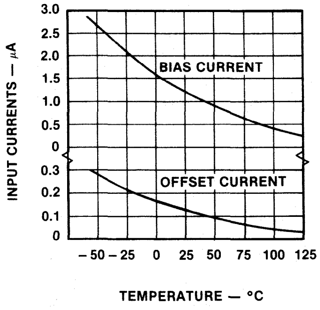
2. Parameters are guaranteed over the temperature range unless otherwise specified.

AC ELECTRICAL CHARACTERISTICS

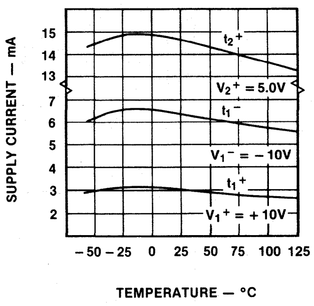
$T_A = 25°C$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Transient response propagation delay time t_{PLH} t_{PHL}	$V_{IN} = \pm100mV$ step		 16 14	 26 24	 ns ns
Delay between output A and B			2	5	ns
Strobe delay time t_{on} Turn-on time t_{off} Turn-off time			 6 6		 ns ns

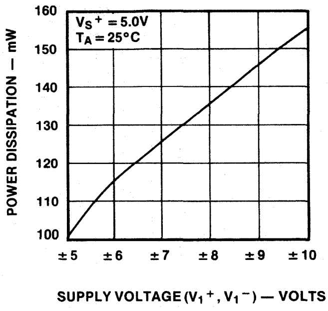
TYPICAL PERFORMANCE CHARACTERISTICS



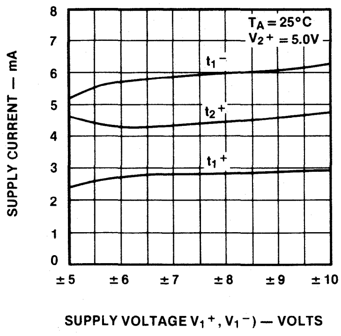
INPUT CURRENTS vs TEMPERATURE



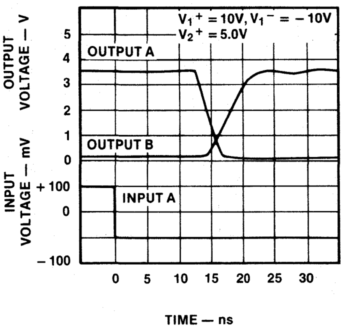
SUPPLY CURRENT vs TEMPERATURE



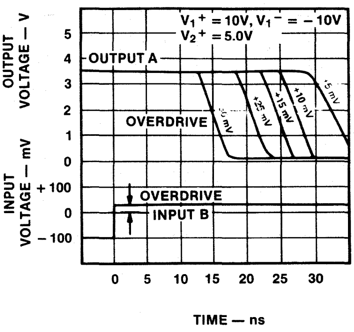
POWER DISSIPATION vs SUPPLY VOLTAGE



SUPPLY CURRENT vs SUPPLY VOLTAGE



OUTPUT PROPAGATION DELAYS



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

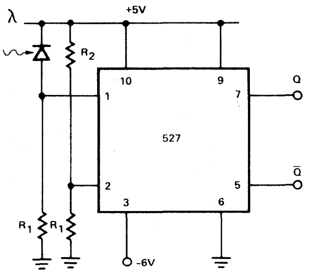
APPLICATIONS

One of the main features of the device is that supply voltages (V1+, V1-) need not be balanced, as indicated in the following diagrams. For proper operation, however, negative supply (V1-) should always be at least six volts more negative than the ground terminal (pin 6). Input Common Mode range should be limited to values of two volts less than the supply voltages (V1+ and V1-) up to a maximum of ±6 volts as supply voltages are increased.

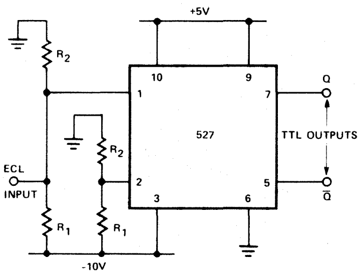
It is also important to note that Output A is in phase with Input A and Output B is in phase with Input B.

TYPICAL APPLICATIONS

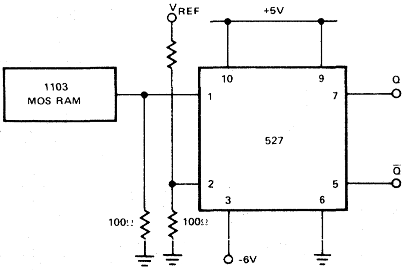
PHOTODIODE DETECTOR



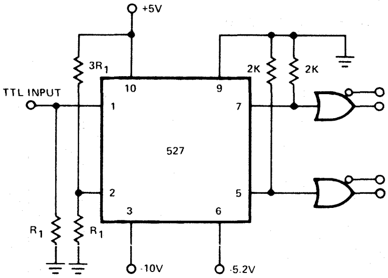
ECL TO TTL INTERFACE



MOS MEMORY SENSE AMP



TTL TO ECL INTERFACE



VOLTAGE COMPARATOR NE/SE529

DESCRIPTION

The SE/NE529 is a high speed analog voltage comparator which, for the first time mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed T²L gates with a precision linear amplifier on a single monolithic chip.

FEATURES

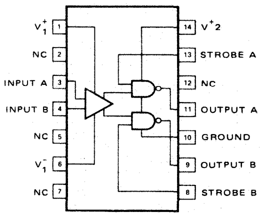
- **10ns propagation delay**
- **Complementary output gates**
- **TTL or ECL compatible outputs**
- **Wide common mode and differential voltage range**

APPLICATIONS

- **A/D conversion**
- **ECL to TTL interface**
- **TTL to ECL interface**
- **Memory sensing**
- **Optical data coupling**
- **Mil std 883A,B,C available**

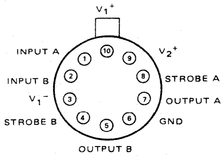
PIN CONFIGURATION

D,F,N PACKAGE



TOP VIEW
ORDER NUMBERS
NE/SE529F, NE529N,D

H PACKAGE*

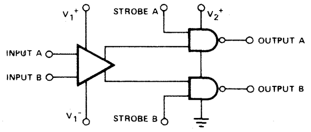


ORDER NUMBERS
NE/SE529H
*Metal cans (H) not recommended for new designs

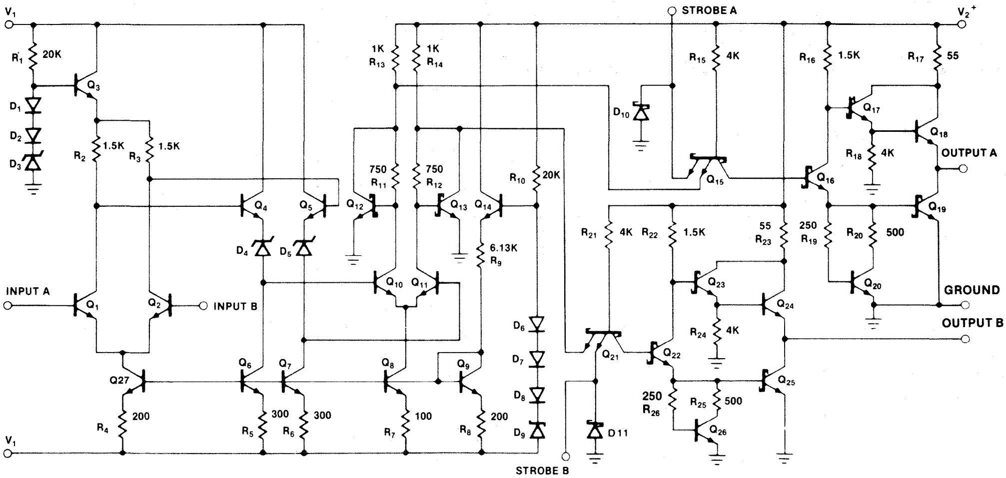
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive supply voltage (V1+)	+15	V
Negative supply voltage (V1-)	-15	V
Gate supply voltage (V2+)	+7	V
Output voltage	+7	V
Differential input voltage	±5	V
Input common mode voltage	±6	V
Power dissipation	600	mW
Operating temperature range		
NE529	0 to +70	°C
SE529	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature		
(soldering, 60 sec)	+300	°C

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



VOLTAGE COMPARATOR NE/SE529

DC ELECTRICAL CHARACTERISTICS $V_{1}+ = +10V$, $V_{2}+ = +5.0V$, $V_{1}- = -10V$

PARAMETER	TEST CONDITIONS	SE529			NE529			UNIT
		Min	Typ	Max	Min	Typ	Max	
INPUT CHARACTERISTICS								
Input offset voltage @25°C				4			6	mV
Over temperature range				6			10	mV
Input bias current @25°C			5	12		5	20	μA
Over temperature range	$V_{IN} = 0V$			36			50	μA
Input offset current @25°C			2	3		2	5	μA
Over temperature range	$V_{IN} = 0V$			9			15	μA
GATE CHARACTERISTICS								
Output voltage								
"1" state	$V_{2}+ = 4.75V$, $I_{source} = -1mA$	2.5	3.3		2.7	3.3		V
"0" state	$V_{2}+ = 4.75V$, $I_{sink} = 10mA$			0.5			0.5	V
Strobe inputs								
"0" Input current[1]	$V_{2}+ = 5.25V$, $V_{strobe} = 0.5V$			-2			-2	mA
"1" Input current @ 25°C[1]	$V_{2}+ = 5.25V$, $V_{strobe} = 2.7V$			50			100	μA
Over temperature range	$V_{2}+ = 5.25V$, $V_{strobe} = 2.7V$			200			200	μA
"0" input voltage	$V_{2}+ = 4.75V$			0.8			0.8	V
"1" input voltage	$V_{2}+ = 4.75V$	2.0			2.0			V
Short circuit								
Output current	$V_{2}+ = 5.25V$, $V_{OUT} = 0V$	-18		-70	-18		-70	mA
POWER SUPPLY REQUIREMENTS								
Supply voltage								
$V_{1}+$		5		10	5		10	V
$V_{1}-$		-6		-10	-6		-10	V
$V_{2}+$		4.5	5	5.5	4.75	5	5.25	V
Supply current	$V_{1}+ = 10V$, $V_{1}- = -10V$ $V_{2}+ = 5.25V$							
$I_{1}+$	Over temp.			5			5	mA
$I_{1}-$	Over temp.			10			10	mA
$I_{2}+$	Over temp.			20			20	mA

NOTES

1. Strobe input current test conditions

INPUT A (V_{IN})	INPUT B		STROBE A	STROBE B
> V Offset	GND	Measure	IIL	IIH
< V Offset	GND	Measure	IIH	IIL

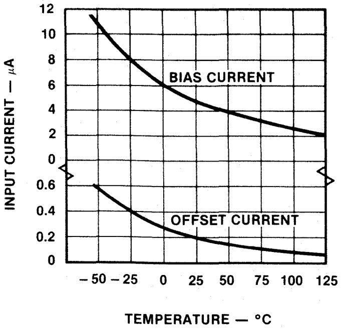
2. Parameters are guaranteed over the temperature range unless otherwise specified.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$

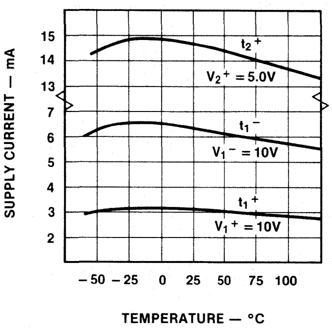
PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Transient response	$V_{IN} = \pm 100mV$ step				
Propagation delay time					
t_{PLH}			12	22	ns
t_{PHL}			10	20	ns
Delay between output A and B			2	5	ns
Strobe delay time					
t_{ON} turn-on time			6		ns
t_{OFF} turn-off time			6		ns

TYPICAL PERFORMANCE CHARACTERISTICS

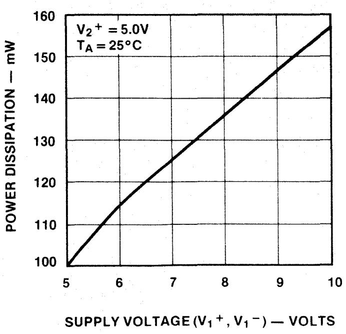
INPUT CURRENTS vs TEMPERATURE



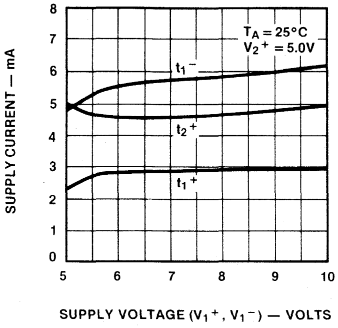
SUPPLY CURRENT vs TEMPERATURE



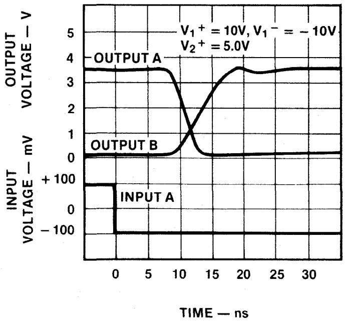
POWER DISSIPATION vs SUPPLY VOLTAGE



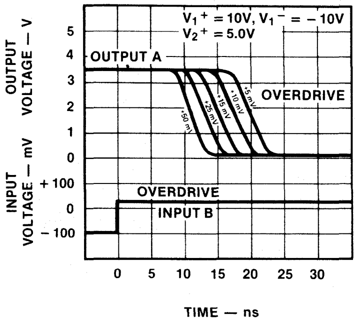
SUPPLY CURRENT vs SUPPLY VOLTAGE



OUTPUT PROPAGATION DELAYS



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



VOLTAGE COMPARATOR NE/SE529

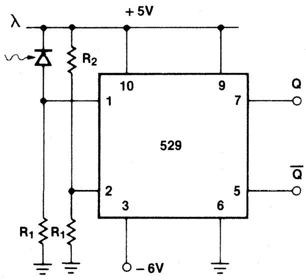
APPLICATIONS

One of the main features of the device is that supply voltages (V1+, V1-) need not be balanced, as indicated in the following diagrams. For proper operation, however, negative supply (V1-) should always be at least six volts more negative than the ground terminal (pin 6). Input Common Mode range should be limited to values of two volts less than the supply voltages (V1+ and V1-) up to a maximum of ±6 volts as supply voltages are increased.

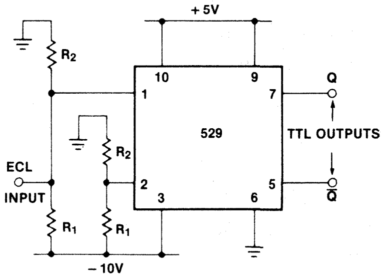
It is also important to note that Output A is in phase with Input A and Output B is in phase with Input B.

TYPICAL APPLICATIONS

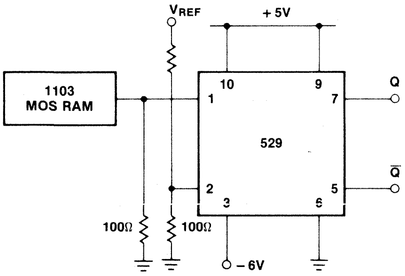
PHOTODIODE DETECTOR



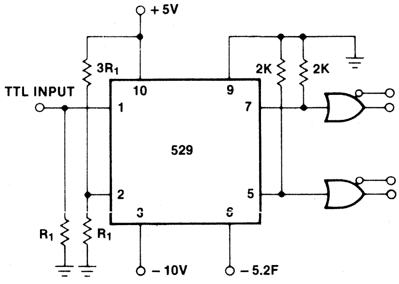
ECL TO TTL INTERFACE



MOS MEMORY SENSE AMP



TTL TO ECL INTERFACE



Section 9
Interface Products

INDEX

Section 9 — Interface Products

DUAL LINE RECEIVER

DS7820/DS8820

DESCRIPTION

The DS7820, specified from -55°C to 125°C, and the DS8820, specified from 0°C to 70°C, are digital line receivers with two completely independent units fabricated on a single silicon chip. Intended for use with digital systems connected by twisted pair lines, they have a differential input designed to reject large common mode signals while responding to small differential signals. The output is directly compatible with RTL, DTL or TTL integrated circuits.

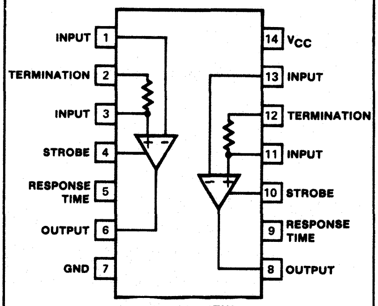
The response time can be controlled with an external capacitor to eliminate noise spikes, and the output state is determined for open inputs. Termination resistors for the twisted pair line are also included in the circuit. Both the DS7820 and the DS8820 are specified, worst case, over their full operating temperature range, for ±10-percent supply voltage variations and over the entire input voltage range.

FEATURES

- **Operation from a single +5V logic supply**
- **Input voltage range of ±15V**
- **Independent channel strobing**
- **High input resistance**
- **Fanout of two with DTL or TTL**
- **Output can be wire OR'ed**
- **DS7820 Mil std 883A,B,C available**

PIN CONFIGURATION

F,N PACKAGE



TOP VIEW

ORDER NUMBERS

DS7820N	DS8820N
DS7820F	DS8820F

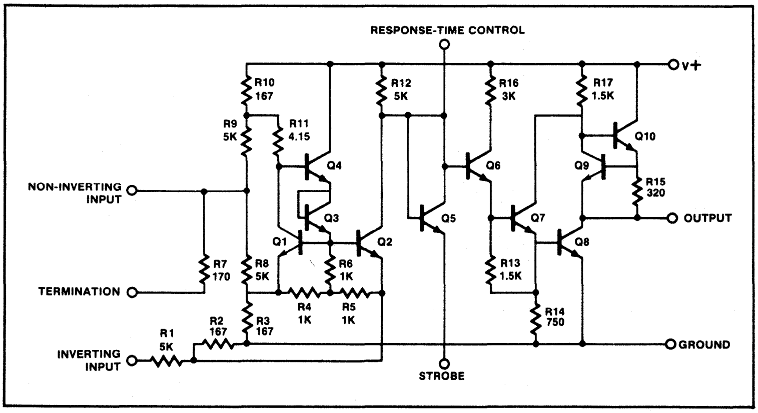
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	8.0	V
Input voltage	±20	V
Differential input voltage	±20	V
Strobe voltage	8.0	V
Output sink current	25	mA
Power dissipation	600	mW
Operating temperature range		
DS7820	-55 to +125	°C
DS8820	0 to 70	°C
Lead temperature		
(soldering, 10sec)	300	°C

NOTE

"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

CIRCUIT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS

Specifications apply for 4.5V ≤ V_{CC} ≤ 5.5, -15V ≤ V_{CM} ≤ 15V and -55°C ≤ T_A ≤ +125°C for the DS7820 or 0°C ≤ T_A ≤ +70°C for the DS8820 unless otherwise specified. Typical values given are for V_{CC} = 5.0V, T_A = 25°C and V_{CM} = 0V unless stated differently.[1,2,3]

PARAMETER		TEST CONDITIONS	DS7820			DS8820			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{TH}	Input threshold	V_{IN} = 0V	-0.5	0	0.5	-0.5	0	0.5	V
V_{TH}	Input threshold	-15V ≤ V_{IN} ≤ 15V	-1.0	0	1.0	-1.0	0	1.0	V
V_{OH}	High output level	I_{OUT} ≤ -0.2mA	2.5		5.5	2.5		5.5	V
V_{OL}	Low output level	I_{SINK} ≤ 3.5mA	0		0.4	0		0.4	V
R_{IN} -	Inverting input resistance		3.6	5.0		3.6	5.0		kΩ
R_{IN} +	Noninverting input resistance		1.8	2.5		1.8	2.5		kΩ
R_T	Line termination resistance		120	170	250	120	170	250	Ω
I_{ST}	Strobe current	V_{Strobe} = 0.4V		1.0	1.4		1.0	1.4	mA
I_{ST}	Strobe current	V_{Strobe} = 5.5V			-5			-5	μA
I_{CC}	Supply current[3]	V_{IN} = 15V		3.2	6.0		3.2	6.0	mA
I_{CC}	Supply current[3]	V_{IN} = 0V		5.8	10.2		5.8	10.2	mA
I_{CC}	Supply current[3]	V_{IN} = -15V		8.3	15.0		8.3	15.0	mA
I_{IN} +	Noninverting input current	V_{IN} = 15V		3.0	7.0		5.0	7.0	mA
I_{IN} +	Noninverting input current	V_{IN} = 0V	-1.6	-1.0		-1.6	-1.0		mA
I_{IN} +	Noninverting input current	V_{IN} = -15V	-9.8	-7.0		-9.8	-7.0		mA
I_{IN} -	Inverting input current	V_{IN} = 15V		3.0	4.2		3.0	4.2	mA
I_{IN} -	Inverting input current	V_{IN} = 0V		0	-0.5		0	-0.5	mA
I_{IN} -	Inverting input current	V_{IN} = -15V	-4.2	-3.0		-4.2	-3.0		mA

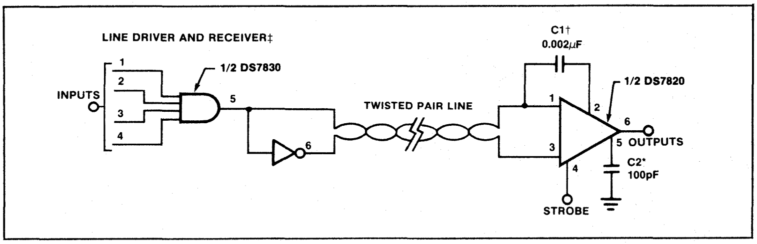
NOTES

1. All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.
2. Only one output at a time should be shorted.
3. The specifications and curves given are for one side only. Therefore, the total package dissipation and supply currents will be double the values given when both receivers are operated under identical conditions.

AC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	DS7820			DS8820			UNIT
		Min	Typ	Max	Min	Typ	Max	
T_R Response time	C_{delay} = 0		40			40		ns
T_R Response time	C_{delay} = 100pF		150			150		ns

DS7820-DS8820 TYPICAL APPLICATION



†Exact value depends on line length

‡V_{CC} is 4.5V to 5.5V for both the DS7820 and DS7830

*Optional to control response time

DUAL LINE RECEIVER DS7820A/DS8820A

DESCRIPTION

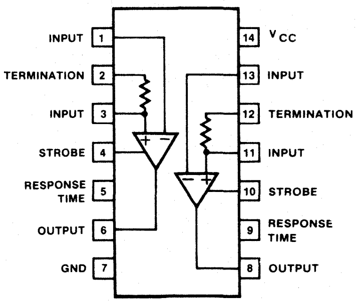
The DS7820A and the DS8820A are improved performance digital line receivers with two completely independent units fabricated on a single silicon chip. Intended for use with digital systems connected by twisted pair lines, they have a differential input designed to reject large common mode signals while responding to small differential signals. The output is directly compatible with RTL, DTL or TTL integrated circuits.

The response time can be controlled with an external capacitor to reject input noise spikes. The output state is a logic "1" for both inputs open. Termination resistors for the twisted pair line are also included in the circuit. Both the DS7820A and the DS8820A are specified, worst case, over their full operating temperature range (-55°C to 125°C and 0°C to 70°C respectively), over the entire input voltage range, for ±10% supply voltage variations.

FEATURES

- **Operation from a single +5V logic supply**
- **Input voltage range of ±15V**
- **Strobe low forces output to "1" state**
- **High input resistance**
- **Fanout of ten with either DTL or TTL integrated circuits**
- **Outputs can be wire OR'ed**
- **Series 54/74 compatible**

PIN CONFIGURATION



TOP VIEW

ORDER NUMBERS
DS7820AN, DS7820AF
DS8820AN, DS8820AF

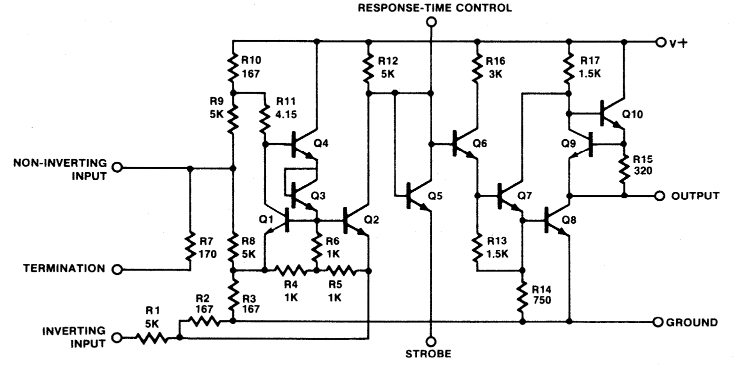
ABSOLUTE MAXIMUM RATINGS*

PARAMETER	RATING	UNIT
Supply voltage	8.0	V
Input voltage	±20	V
Differential input voltage	±20	V
Strobe voltage	8.0	V
Output sink current	50	mA
Power dissipation	600	mW
Operating temperature range		
DS7820A	-55 to +125	°C
DS8820A	0 to +70	°C
Lead temperature (soldering, 60sec)	300	°C

*NOTE

"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS

T_A = 25°C unless otherwise specified.[1,2,3,4]

PARAMETER		TEST CONDITIONS	DS7820A/DS8820A			UNIT
			Min	Typ	Max	
V_{TH}	Differential threshold voltage	I_{OUT} = -400μA -3V ≤ V_{CM} ≤ +3V		0.06	0.5	V
		V_{OUT} ≥ 2.5V -15V ≤ V_{CM} ≤ +15V		0.06	1.0	V
		I_{OUT} = +16mA -3V ≤ V_{CM} ≤ +3V		-0.08	-0.5	V
		V_{OUT} ≤ 0.4V -15V ≤ V_{CM} ≤ +15V		-0.08	-1.0	V
R_I^-	Inverting input resistance	-15V ≤ V_{CM} ≤ +15V	3.6	5		kΩ
R_I^+	Non-inverting input resistance	-15V ≤ V_{CM} ≤ +15V	1.8	2.5		kΩ
R_T	Line termination resistance		120	170	250	Ω
I_I^-	Inverting input current	V_{CM} = 15V		3.0	4.2	mA
		V_{CM} = 0V		0	-0.5	mA
		V_{CM} = -15V		-3.0	-4.2	mA
I_I^+	Non-inverting input current	V_{CM} = 15V		5.0	7.0	mA
		V_{CM} = 0V		-1.0	-1.6	mA
		V_{CM} = -15V		-7.0	-9.8	mA
I_{CC}	Power supply current	V_{DIFF} = -1V, V_{CM} = 15V		3.9	6.0	mA
		I_{OUT} = Logical "0" V_{CM} = -15V		9.2	14.0	mA
		V_{DIFF} = -0.5V, V_{CM} = 0V		6.5	10.2	mA
V_{OH}	Logical "1" output voltage	I_{OUT} = -400μA, V_{DIFF} = 1V	2.5	4.0	5.5	V
V_{OL}	Logical "0" output voltage	I_{OUT} = +16mA, V_{DIFF} = -1V	0	0.22	0.4	V
V_{SH}	Logical "1" strobe input voltage	I_{OUT} = +16mA, V_{OUT} ≤ 0.4V, V_{DIFF} = -3V	2.1			V
V_{SL}	Logical "0" strobe input voltage	I_{OUT} = -400μA, V_{OUT} ≥ 2.5V, V_{DIFF} = -3V			0.9	V
I_{SH}	Logical "1" strobe input current	V_{STROBE} = 5.5V, V_{DIFF} = 3V		0.01	5.0	μA
I_{SL}	Logical "0" strobe input current	V_{STROBE} = 0.4V, V_{DIFF} = -3V		-1.0	-1.4	mA
I_{SC}	Output short circuit current	I_{OUT} = 0V, V_{CC} = 5.5V, V_{STROBE} = 0V	-2.8	-4.5	-6.7	mA

NOTES

1. These specifications apply for 4.5V ≤ V_{CC} ≤ 5.5V, -15V ≤ V_{CM} ≤ 15V and -55°C ≤ T_A ≤ +125°C for the DS7820A or 0°C ≤ T_A ≤ +70°C for the DS8820A unless otherwise specified. Typical values given are for V_{CC} = 5.0V, T_A = 25°C and V_{CM} = 0V unless stated differently.
2. All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.
3. Only one output at a time should be shorted.
4. The specifications and curves given are for one side only. Therefore, the total package dissipation and supply currents will be double the values given when both receivers are operated under identical conditions.

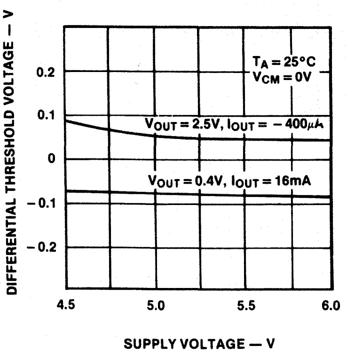
AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 5V unless otherwise specified.

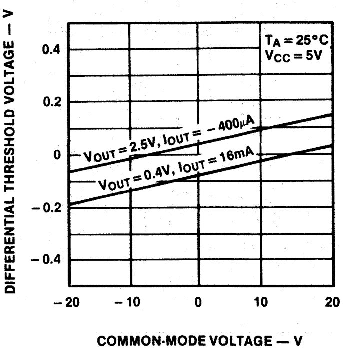
PARAMETER		TEST CONDITIONS	DS7820A/DS8820A			UNIT
			Min	Typ	Max	
t_{PD0}	Propagation delay, differential input to "0" output			30	45	ns
t_{PD1}	Propagation delay, differential input to "1" output			27	40	ns
t_{PD0}	Propagation delay, strobe input to "0" output			16	25	ns
t_{PD1}	Propagation delay, strobe input to "1" output			18	30	ns

DUAL LINE RECEIVER DS7820A/DS8820A

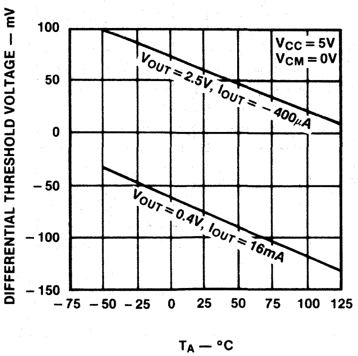
TYPICAL PERFORMANCE CHARACTERISTICS



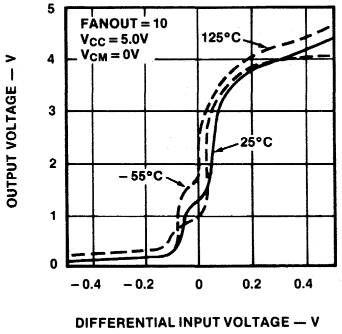
SUPPLY VOLTAGE SENSITIVITY



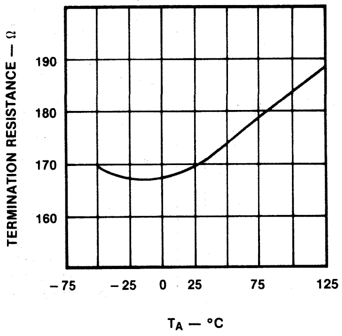
COMMON-MODE VOLTAGE SENSITIVITY



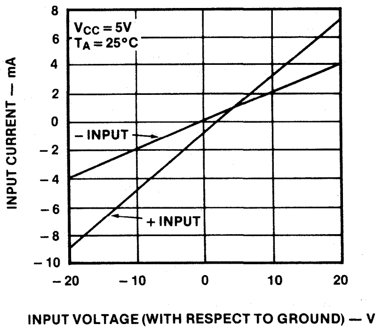
TEMPERATURE SENSITIVITY



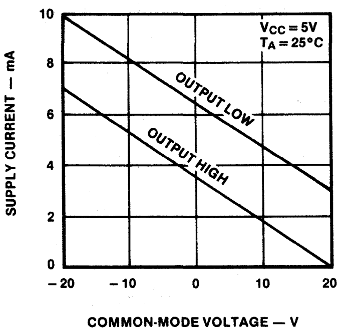
TRANSFER FUNCTION



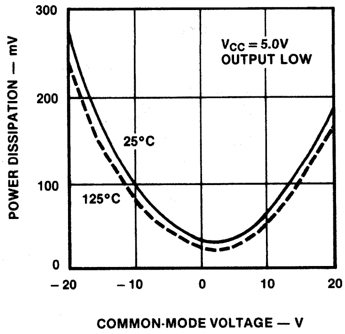
TERMINATION RESISTANCE



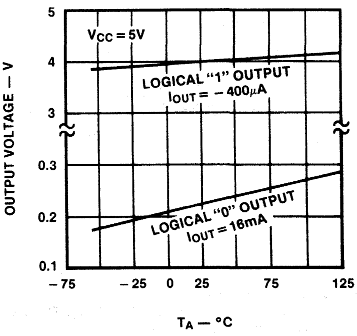
INPUT CHARACTERISTICS



POWER SUPPLY CURRENT



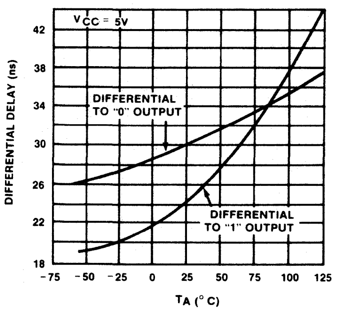
INTERNAL POWER DISSIPATION



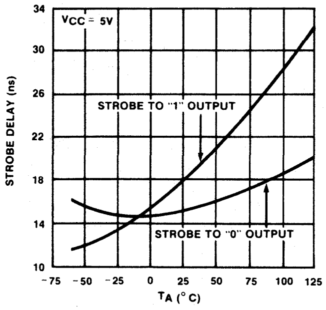
OUTPUT VOLTAGE LEVELS

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

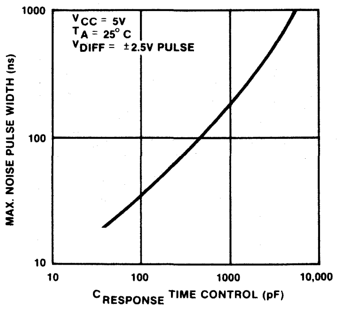
DIFFERENTIAL INPUT DELAYS



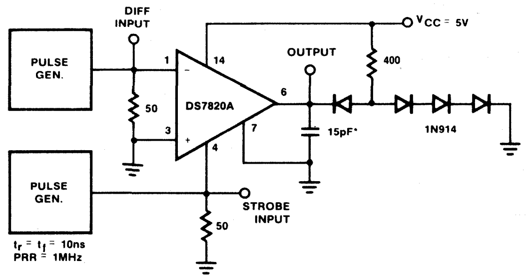
STROBE DELAYS



NOISE REJECTION

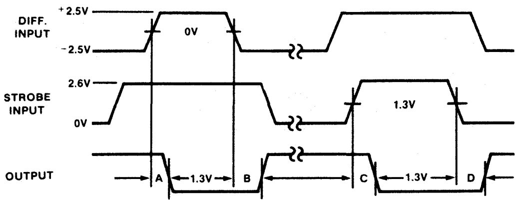


AC TEST CIRCUIT



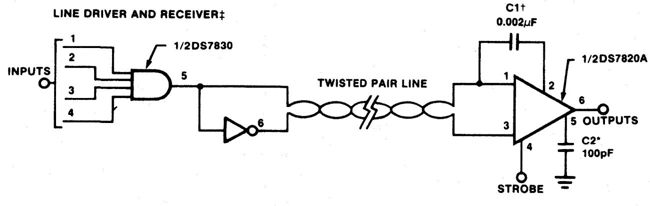
*Includes Jig and Probe

VOLTAGE WAVEFORM



A = Differential input to "0" output
B = Differential input to "1" output
C = Strobe input to "0" output
D = Strobe input to "1" output

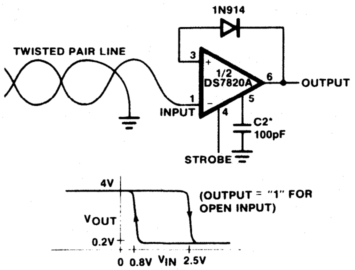
TYPICAL APPLICATIONS



NOTES

†Exact value depends on line length
‡VCC is 4.5V to 5.5V for both the DS7820 and DS7830
*Optional to control response time

SINGLE ENDED (EIA-RS232C) RECEIVER WITH HYSTERESIS



DUAL DIFFERENTIAL LINE DRIVER

DS7830/DS8830

DESCRIPTION

The DS7830/DS8830 is a dual differential line driver that also performs the dual four-input NAND or dual four-input AND function.

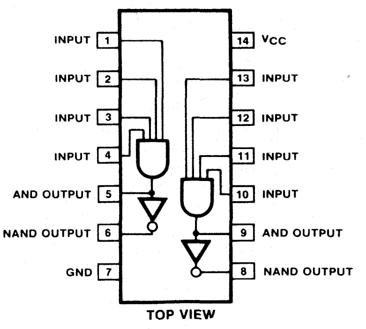
TTL (Transistor-Transistor-Logic) multiple emitter inputs allow this line driver to interface with standard TTL or DTL systems. The differential outputs are balanced and are designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines with characteristic impedances of 50Ω to 500Ω. The differential feature of the output eliminates troublesome ground-loop errors normally associated with single-wire transmissions.

FEATURES

- **Single 5 volt power supply**
- **High speed**
- **Diode protected outputs for termination of positive and negative voltage transients**
- **Diode protected inputs to prevent line ringing**
- **Short circuit protection**
- **DS7830 Mil std 883A,B,C available**

PIN CONFIGURATION

F,N PACKAGE

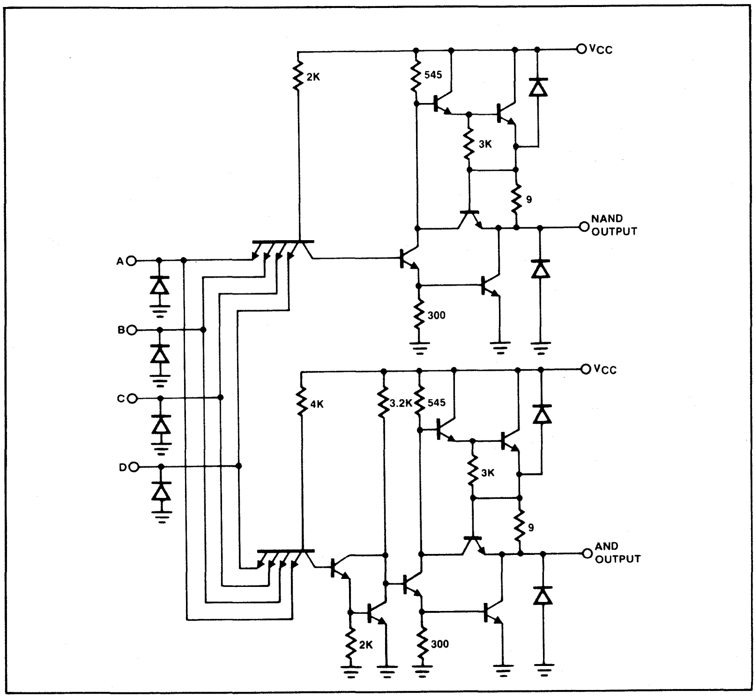


ORDER NUMBERS
DS7830N, DS7830F
DS8830N, DS8830F

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V_{CC}	7.0	V
Input voltage	5.5	V
Operating temperature range		
DS7830	-55 to +125	°C
DS8830	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 10sec)	300	°C

EQUIVALENT SCHEMATIC



DUAL DIFFERENTIAL LINE DRIVER

DS7830/DS8830

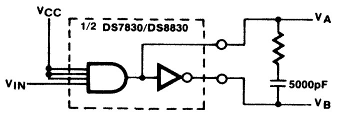
ELECTRICAL CHARACTERISTICS $T_A = 25°C$ $V_{CC} = 5V$ unless otherwise specified.[1,2]

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Logical "1" input voltage		2.0			V
Logical "0" input voltage				0.8	V
Logical "1" output voltage	$V_{IN} = 0.8V$ $I_{OUT} = -0.8mA$	2.4			V
Logical "1" output voltage	$V_{IN} = 0.8V$ $I_{OUT} = -40mA$	1.8	2.9		V
Logical "0" output voltage	$V_{IN} = 2.0V$ $I_{OUT} = +32mA$		0.2	0.4	V
Logical "0" output voltage	$V_{IN} = 2.0V$ $I_{OUT} = +40mA$		0.22	0.5	V
Logical "1" input current	$V_{IN} = +2.4V$			120	μA
Logical "1" input current	$V_{IN} = 5.5V$			2	mA
Logical "0" input current	$V_{IN} = 0.4V$			4.8	mA
Output short circuit current[2]	$V_{CC} = 5.0V$	-40	-100	-120	mA
Supply current	$V_{CC} = 5.0V$ $V_{IN} = 5.0V$ (Each driver)		11	18	mA
Propagation delay AND gate $t_{pd}1$	$T_A = 25°C$		8	12	ns
$t_{pd}0$	$V_{CC} = 5.0V$		11	18	ns
Propagation delay NAND gate $t_{pd}1$	$C_L = 15pF$		8	12	ns
$t_{pd}0$	See Figure 1		5	8	ns
Differential delay t_1	Load, 100Ω and 5000pF		12	16	ns
Differential delay t_2	See Figure 2		12	16	ns

NOTES

1. Specifications apply for DS7830 -55°C ≤ T_A ≤ +125°C, V_{CC} = +5V ±10%, DS8830 0°C ≤ T_A ≤ 70°C, V_{CC} = +5V ±5% unless otherwise specified.
2. Applies for T_A = +125°C, only one output at a time to be shorted.

AC TEST CIRCUIT



†VCC is 4.5V to 5.5V for both the DS7820 and DS7830

†Exact value depends on transmission rate

*Optional to control response time

SWITCHING TIME WAVEFORMS

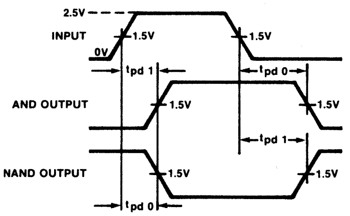


Figure 1

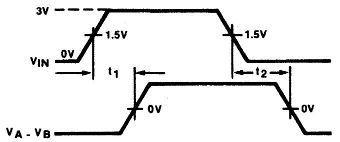
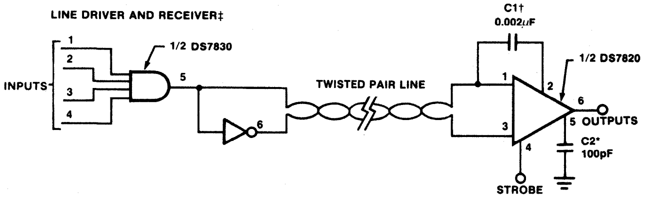


Figure 2

TYPICAL APPLICATION



†Exact value depends on line length

‡VCC is 4.5V to 5.5V for the DS7820 and DS7830

*Optional to control response time

QUAD LINE DRIVER

MC1488

DESCRIPTION

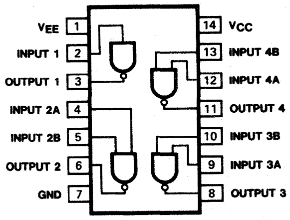
The MC1488 is a quad line driver which converts standard DTL/TTL input logic levels through one stage of inversion to output levels which meet EIA Standard No. RS-232C and CCITT Recommendation V.24.

FEATURES

- **Current limited output: ±10mA Typ**
- **Power-off source impedance: 300Ω Min**
- **Simple slew rate control with external capacitor**
- **Flexible operating supply range**
- **Inputs are DTL/TTL compatible**

PIN CONFIGURATION

F,N PACKAGE



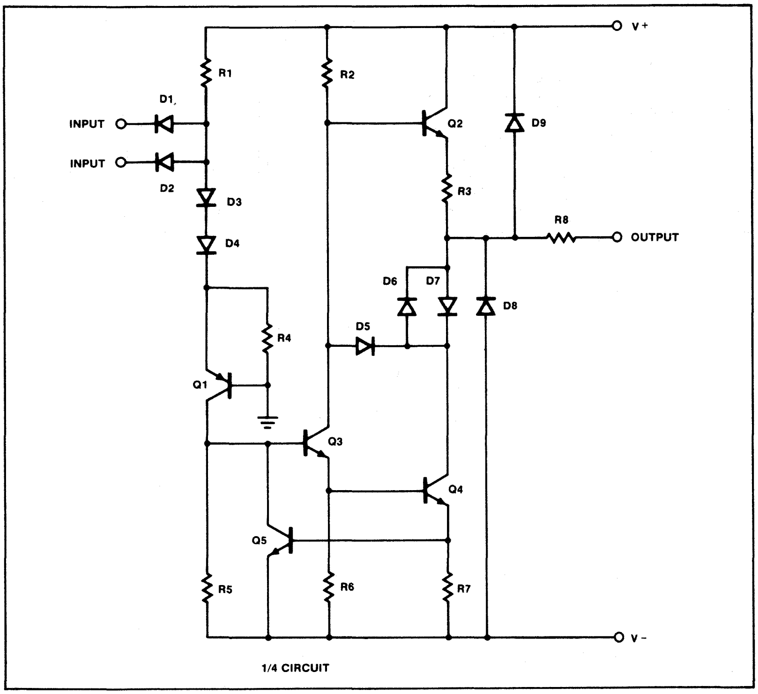
TOP VIEW

ORDER NUMBERS
MC1488F, MC1488N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage V+	+15	V
V-	-15	V
Input voltage (V_{IN})	$-15 \leq V_{IN} \leq 7.0$	V
Output voltage	±15	V
Power dissipation:		
F package	1000	mW
N package	800	mW
Operating temperature range	0 to +75	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 10sec)	300	°C

CIRCUIT SCHEMATIC



QUAD LINE DRIVER MC1488

DC ELECTRICAL CHARACTERISTICS

V+ = +9.0V ± 1%, V- = -9.0V ± 1%, T_A = 0°C to +75°C unless otherwise specified.
All typicals are for V+ = 9.0V, V- = -9.0V, and T_A = 25°C.*

PARAMETER	TEST CONDITIONS		LIMITS			UNIT
			Min	Typ	Max	
Logic "0" input current	V_{IN} = 0V			-1.0	-1.6	mA
Logic "1" input current	V_{IN} = +5.0V			.005	10.0	μA
High level output voltage	R_L = 3.0kΩ V_{IN} = 0.8V	V+ = 9.0V V- = -9.0V	6.0	7.0		V
		V+ = 13.2V V- = -13.2V	9.0	10.5		V
Low level output voltage	R_L = 3.0kΩ V_{IN} = 1.9V	V+ = 9.0V V- = -9.0V	-6.0	-6.8		V
		V+ = 13.2V V- = -13.2V	-9.0	-10.5		V
High level output Short-circuit current	V_{OUT} = 0V V_{IN} = 0.8V		-5.0	-10.0	-12.0	mA
Low level output Short-circuit current	V_{OUT} = 0V V_{IN} = 1.9V		6.0	10.0	12.0	mA
Output resistance	V+ = V- = 0V V_{OUT} = ±2V		300			Ω
Positive supply current (output open)	V_{IN} = 1.9V	V+ = 9.0V, V- = -9.0V		15.0	20.0	mA
		V+ = 12V, V- = -12V		19.0	25.0	mA
		V+ = 15V, V- = -15V		25.0	34.0	mA
	V_{IN} = 0.8V	V+ = 9.0V, V- = -9.0V		4.5	6.0	mA
		V+ = 12V, V- = -12V		5.5	7.0	mA
		V+ = 15V, V- = -15V		8.0	12.0	mA
Negative supply current (output open)	V_{IN} = 1.9V	V+ = 9.0V, V- = -9.0V		-13.0	-17.0	mA
		V+ = 12V, V- = -12V		-18.0	-23.0	mA
		V+ = 15V, V- = -15V		-25.0	-34.0	mA
	V_{IN} = 0.8V	V+ = 9.0V, V- = -9.0V		-1	-15	μA
		V+ = 12V, V- = -12V		-1	-15	μA
		V+ = 15V, V- = -15V		-.01	-2.5	mA
Power dissipation	V+ = 9.0V, V- = -9.0V			252	333	mW
	V+ = 12V, V- = -12V			444	576	mW
Propagation delay to "1" (t_{pd1})	R_L = 3.0kΩ, C_L = 15pF, T_A = 25°C			275	560	ns
Propagation delay to "0" (t_{pd0})	R_L = 3.0kΩ, C_L = 15pF, T_A = 25°C			70	175	ns
Rise time (t_r)	R_L = 3.0kΩ, C_L = 15pF, T_A = 25°C			75	100	ns
Fall time (t_f)	R_L = 3.0kΩ, C_L = 15pF, T_A = 25°C			40	75	ns

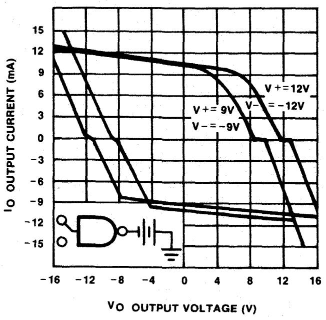
NOTE

*Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.

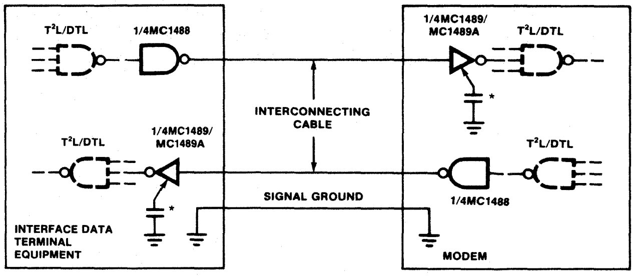
QUAD LINE DRIVER MC1488

TYPICAL PERFORMANCE CHARACTERISTICS

OUTPUT VOLTAGE AND CURRENT-LIMITING CHARACTERISTICS



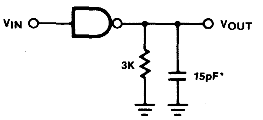
RS232C DATA TRANSMISSION



NOTE

*Optional for noise filtering

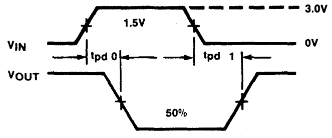
AC LOAD CIRCUIT



NOTE

$^{*}C_L$ includes probe and jig capacitance.

SWITCHING WAVEFORMS



NOTE

t_r and t_f are measured between 10% and 90% of the output waveform

APPLICATIONS

By connecting a capacitor to each driver output the slew rate can be controlled utilizing the output current limiting characteristics of the MC1488. For a set slew rate the appropriate capacitor value may be calculated using the following relationship

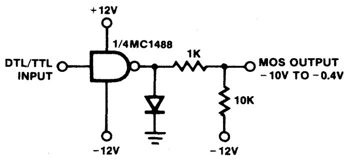
$$C = I_{SC} (\Delta T/\Delta V)$$

where C is the required capacitor, I_{SC} is the short circuit current value, and $\Delta V/\Delta T$ is the slew rate.

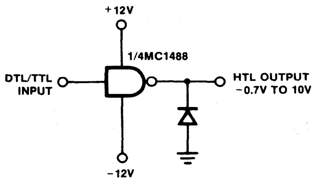
RS232C specifies that the output slew rate must not exceed 30V per microsecond. Using the worst case output short circuit current of 12mA in the above equation, calculations result in a required capacitor of 400pF connected to each output.

TYPICAL APPLICATIONS

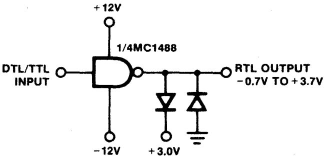
DTL/TTL-TO-MOS TRANSLATOR



DTL/TTL-TO-HTL TRANSLATOR



DTL/TTL-TO-RTL TRANSLATOR



QUAD LINE RECEIVERS

MC1489/MC1489A

DESCRIPTION

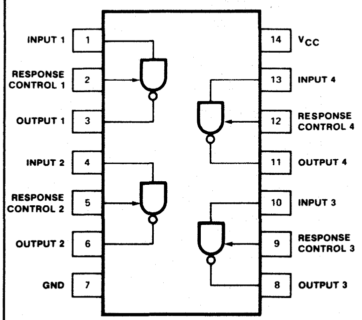
The MC1489/MC1489A are quad line receivers designed to interface data terminal equipment with data communications equipment. They are constructed on a single monolithic silicon chip. These devices satisfy the specifications of EIA standard No. RS232C.

FEATURES

- **Four totally separate receivers per package**
- **Programmable threshold**
- **Built-in input threshold hysteresis**
- **"Fail safe" operating mode**
- **Inputs withstand ±30V**

PIN CONFIGURATION

F,N PACKAGE



TOP VIEW

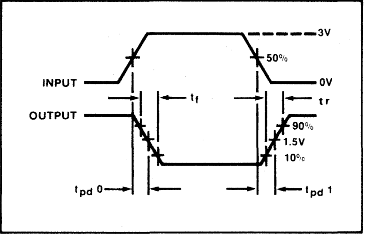
ORDER NUMBERS

MC1489F, MC1489AF, MC1489N, MC1489AN

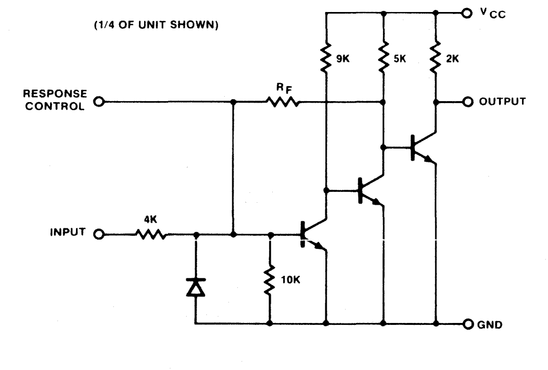
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Power supply voltage	10	V
Input voltage range	±30	V
Output load current	20	mA
Power dissipation:		
F package	1	W
N package	800	mW
Operating temperature range	0 to +75	°C
Storage temperature range	-65 to +150	°C

VOLTAGE WAVEFORMS

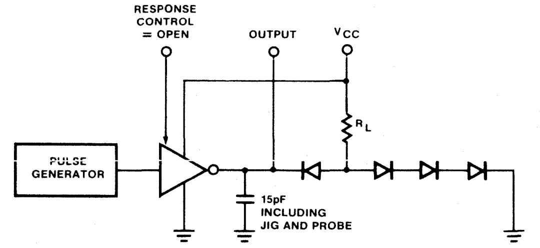


EQUIVALENT SCHEMATIC



MC1489: RF = 10k
MC1489A: RF = 2k

AC TEST CIRCUIT



QUAD LINE RECEIVERS MC1489/MC1489A

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ± 1%, 0°C ≤ T_A ≤ +75°C unless otherwise specified.[1,2]

PARAMETER	TEST CONDITIONS	MC1489			MC1489A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input high threshold voltage	T_A = 25°C, V_{OUT} ≤ 0.45V, I_{OUT} = 10mA	1.0		1.5	1.75		2.25	V
Input low threshold voltage	T_A = 25°C, V_{OUT} ≤ 2.5V, I_{OUT} = -0.5mA	0.75		1.25	0.75		1.25	V
	V_{IN} = +25V	+3.6	+5.6	+8.3	+3.6	+5.6	+8.3	mA
	V_{IN} = -25V	-3.6	-5.6	-8.3	-3.6	-5.6	-8.3	
Input current	V_{IN} = +3V	+0.43	+0.53		+0.43	+0.53		mA
	V_{IN} = -3V	-0.43	-0.53		-0.43	-0.53		
Output high voltage	V_{IN} = 0.75V, I_{OUT} = -0.5mA	2.6	3.8	5.0	2.6	3.8	5.0	V
	Input = Open, I_{OUT} = -0.5mA	2.6	3.8	5.0	2.6	3.8	5.0	V
Output low voltage	V_{IN} = 3.0V, I_{OUT} = 10mA		0.33	0.45		0.33	0.45	V
Output short circuit current	V_{IN} = 0.75V		3.0			3.0		mA
Supply current	V_{IN} = 5.0V		20	26		20	26	mA
Power dissipation	V_{IN} = 5.0V		100	130		100	130	mW

NOTES

1. Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
2. These specifications apply for response control pin = open.

AC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ± 1%, T_A = 25°C unless otherwise specified.[1,2]

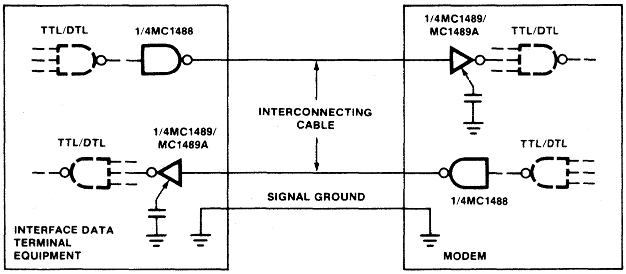
PARAMETER	TEST CONDITIONS	MC1489			MC1489A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input to output "high" Propagation delay (t_{pd1})	R_L = 3.9kΩ (AC test circuit)		25	85		25	85	ns
Input to output "low" Propagation delay (t_{pd0})	R_L = 390Ω (AC test circuit)		20	50		20	50	ns
Output rise time	R_L = 3.9kΩ (AC test circuit)		110	175		110	175	ns
Output fall time	R_L = 390Ω (AC test circuit)		9	20		9	20	ns

NOTES

1. Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
2. These specifications apply for response control pin = open.

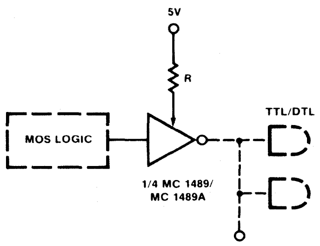
TYPICAL APPLICATIONS

RS232C DATA TRANSMISSION



*Optional for noise filtering

MOS TO TTL/DTL TRANSLATOR



ADDRESSABLE PERIPHERAL DRIVERS NE590/NE591

DESCRIPTION

The NE590/591 addressable peripheral drivers are high current latched drivers, similar in function to the 9334 address decoder. The device has 8 Darlington power outputs, each capable of 250mA load current. The outputs are turned on or off by respectively loading a logic high or logic low into the device data input. The required output is defined by a 3-bit address. The device must be enabled by a $\overline{CE}$ input line which also serves the function of further address decoding. A common clear input, $\overline{CLR}$, turns all outputs off when a logic low is applied.

The NE590 has 8 open collector Darlington outputs which sink current to ground. The device is packaged in a 16-pin molded or cerdip package.

The NE591 has 8 open emitter Darlington outputs which source current to an external load from a common collector line, V_S. This V_S line need not necessarily be the same as the 5 volt V_{CC} supply. The device is packaged in an 18-pin molded or cerdip package.

FEATURES

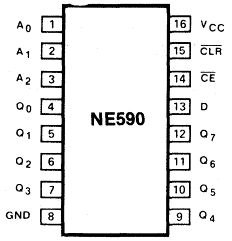
- **8 high current outputs**
- **Low-loading bus compatible inputs**
- **Power-on clear ensures safe operation**
- **NE590 will operate in addressable or demultiplex mode**
- **Allows random (addressed) data entry**
- **Easily expandable**
- **NE590 is pin compatible with 9334**

APPLICATIONS

- **Relay driver**
- **Indicator lamp driver**
- **Triac trigger**
- **LED display digit driver**
- **Stepper motor driver**

PIN CONFIGURATION

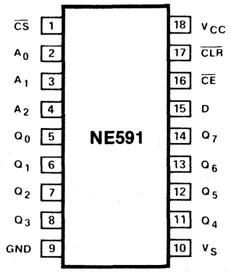
F,N PACKAGE



TOP VIEW

ORDER NUMBERS
NE590N,F

F,N PACKAGE



TOP VIEW

ORDER NUMBERS
NE591N,F

PIN DESIGNATION

590 PIN NO.	591 PIN NO.	SYMBOL	NAME & FUNCTION
1-3	2-4	A_0-A_2	A 3-bit binary address on these pins defines which of the 8 output latches is to receive the data.
4-7, 9-12	5-8, 11-14	Q_0-Q_7	The 8 device outputs. The NE590 has open collector Darlington outputs. The NE591 has open emitter follower outputs.
13	15	D	The data input. When the chip is enabled, this data bit is transferred to the defined output such that: "1" turns output switch "ON" "0" turns output switch "OFF" Thus in logic terms, the NE590 inverts data to the relevant output. The NE591 retains true data at the output.
14	16	$\overline{CE}$	The chip enable. When this input is low, the output latches will accept data. When $\overline{CE}$ goes high, all outputs will retain their existing state, regardless of address or data input conditions.
15	17	$\overline{CLR}$	The clear input. When $\overline{CLR}$ goes low all output switches are turned "OFF". On the NE590, a high data input will override the clear function on the addressed latch. On the NE591, $\overline{CLR}$ low will override any other condition.
—	1	$\overline{CS}$	The chip select input provides for an additional level of address decoding.
—	10	V_S	The V_S line provides the power to all 8 output devices. It is connected to the collectors of all 8 output transistors. This pin may be connected to the V_{CC} or another supply.

ADDRESSABLE PERIPHERAL DRIVERS

NE590/NE591

TRUTH TABLE (NE590)

INPUTS						OUTPUTS								MODE
$\overline{CLR}$	$\overline{CE}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
L	H	X	X	X	X	H	H	H	H	H	H	H	H	Clear
L	L	L	L	L	L	H	H	H	H	H	H	H	H	Demultiplex
L	L	H	L	L	L	L	H	H	H	H	H	H	H	
L	L	L	H	L	L	H	H	H	H	H	H	H	H	
L	L	H	H	L	L	H	L	H	H	H	H	H	H	
L	L	L	H	H	H	H	H	H	H	H	H	H	H	
L	L	H	H	H	H	H	H	H	H	H	H	H	L	
H	H	X	X	X	X	Q_{N-1} ⟶								Memory
H	L	L	L	L	L	H	Q_{N-1} ⟶							Addressable Latch
H	L	H	L	L	L	L	Q_{N-1} ⟶							
H	L	L	H	L	L	Q_{N-1}	H	Q_{N-1} ⟶						
H	L	H	H	L	L	Q_{N-1}	L	Q_{N-1}						
H	L	L	H	H	H	Q_{N-1} ⟶							H	
H	L	H	H	H	H	Q_{N-1} ⟶							L	

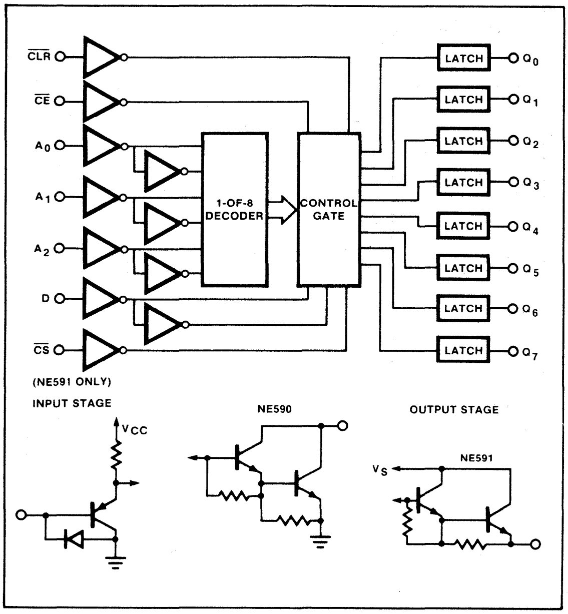
X = Don't care condition
Q_{N-1} = Previous output state
L = Low voltage level/"ON" output state
H = High voltage level/"OFF" output state

(NE591)

INPUTS							OUTPUTS								MODE
$\overline{CLR}$	CE	$\overline{CS}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
L	X	X	X	X	X	X	L	L	L	L	L	L	L	L	Clear
H	H	H	X	X	X	X	Q_{N-1} ⟶								Memory
H	H	L	X	X	X	X	Q_{N-1} ⟶								
H	L	H	X	X	X	X	Q_{N-1} ⟶								
H	L	L	L	L	L	L	L	Q_{N-1} ⟶							Addressable Latch
H	L	L	H	L	L	L	H	Q_{N-1} ⟶							
H	L	L	L	H	L	L	Q_{N-1}	L	Q_{N-1} ⟶						
H	L	L	H	H	L	L	Q_{N-1}	H	Q_{N-1} ⟶						
H	L	L	L	H	H	H	Q_{N-1} ⟶							L	
H	L	L	H	H	H	H	Q_{N-1} ⟶							H	

X = Don't care
Q_{N-1} = Previous output state
L = Low voltage level/"OFF" output state
H = High voltage level/"ON" output state

ADDRESSABLE PERIPHERAL DRIVERS NE590/NE591



ABSOLUTE MAXIMUM RATINGS

$T_A = 25°C$ unless otherwise specified.

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7	V
V_{IN}	Input voltage	-0.5 to +15	V
V_{OUT}	Output voltage		V
	NE590	0 to +7	
	NE591	0 to V_{CC}	
V_S	Source bus voltage		V
	NE591 only	-0.5 to +7	
V_S-V_{CC}	Source/supply differential voltage		V
	NE591 only	-5 to +2	
I_{OUT}	Output current		mA
	Each output	300	
	All outputs	1000	
P_D	Power dissipation[1]	1	W
	Temperature range		°C
T_A	Ambient	0 to +70	
T_J	Junction	150	
T_{STG}	Storage	-65 to +150	
T_{sold}	Lead soldering temperature (10sec max)	300	°C

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 4.75$ to $5.25V$, $0°C \leq T_A \leq 70°C$ unless otherwise specified.[2,3]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IH}	High		2.0			
V_{IL}	Low				0.8	
	Output voltage					V
V_{OL}	Low (NE590 only)	$I_{OL} = 250mA$, $T_A = 25°C$		1.0	1.3	
		Over temperature			1.5	
V_{OH}	High (NE591 only)	$I_{OH} = -250mA$, $V_{CC} = V_S = 5V$	2.9			
	Input current					μA
I_{IH}	High	$V_{in} = V_{CC}$		0.1	10	
I_{IL}	Low	$V_{in} = 0V$				
	$\overline{CE}$ input			-25	-60	
	All other inputs			-15	-50	
	Supply current[4]	$V_S = V_{CC} = 5V$				mA
I_{CCL}	All outputs low					
	NE590			33	50	
	NE591			15	50	
I_{CCH}	All outputs high					
	NE590			15	50	
	NE591			30	50	

NOTES

1. Derate power dissipation as indicated above threshold ambient temperature:
   NE590N at 95°C/W above 55°C
   NE590F at 100°C/W above 50°C
   NE591N at 90°C/W above 60°C
   NE591F at 93°C/W above 57°C
2. All typical values are at $V_{CC} = 5V$ and $T_A = 25°C$.
3. For the NE591, $V_S = V_{CC}$ in all tests.
4. Supply current for the NE591 is measured with no output load.

ADDRESSABLE PERIPHERAL DRIVERS

NE590/NE591

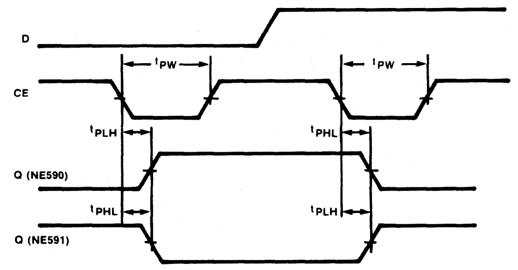
SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

PARAMETER	TO	FROM	NE590			NE591			UNIT
			Min	Typ	Max	Min	Typ	Max	
Propagation delay time									ns
t_{PLH} Low to high[5]	Output	$\overline{CE}$		100			70		
t_{PHL} High to low[5]				130			80		
t_{PLH} Low to high[6]	Output	Data		80			60		
t_{PHL} High to low[6]				100			70		
t_{PLH} Low to high[7]	Output	Address		125			70		
t_{PHL} High to low[7]				115			70		
t_{PLH} Low to high[8]	Output	$\overline{CLR}$		80					
t_{PHL} High to low[8]							60		
t_{PLH} Low to high[5]	Output	$\overline{CS}$					70		
t_{PHL} High to low[5]							80		
SWITCHING SET-UP REQUIREMENTS									
$t_{s(H)}$[9]	Chip enable	High data		120			50		ns
$t_{s(L)}$[9]	Chip enable	Low data		120			70		ns
$t_{s(A)}$[10]	Chip enable	Address		-60			-10		ns
$t_{h(H)}$[9]	Chip enable	High data		-60			-60		ns
$t_{h(L)}$[9]	Chip enable	Low data		-60			-20		ns
$t_{s(CS)}$[9]	Chip enable	Low chip select					70		ns
$t_{pw(E)}$ Chip enable pulse width[5]				150			80		ns

NOTES

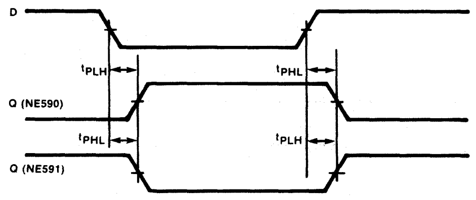
5. See Turn-On and Turn-Off Delays, Enable to Output and Enable Pulse Width timing diagram.
6. See Turn-On and Turn-Off Delays, Data to Output timing diagram.
7. See Turn-On and Turn-Off Delays, Address to Output timing diagram.
8. See Turn-Off Delay, Clear to Output timing diagram.
9. See Setup and Hold Time, Data to Enable timing diagram.
10. See Setup Time, Address to Enable timing diagram.

TURN-ON AND TURN-OFF DELAYS, ENABLE TO OUTPUT AND ENABLE PULSE WIDTH



Other Inputs: $\overline{CLR}$ = H, A = Stable, $\overline{CS}$ = L

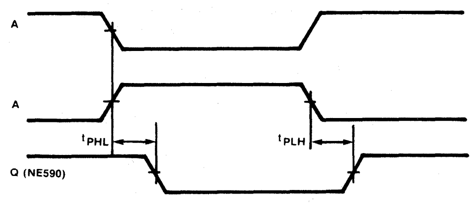
TURN-ON AND TURN-OFF DELAYS, DATA TO OUTPUT



Other Inputs: $\overline{CE}$ = $\overline{CS}$ = L, $\overline{CLR}$ = H, A = Stable

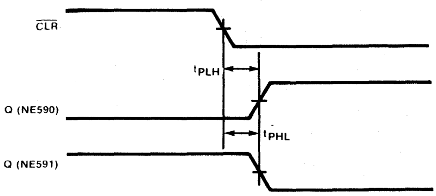
ADDRESSABLE PERIPHERAL DRIVERS NE590/NE591

TURN-ON AND TURN-OFF DELAYS, ADDRESS TO OUTPUT



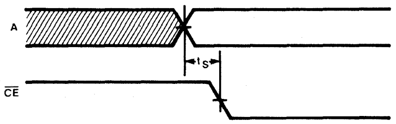
Other Inputs: $\overline{CE}$ = L, $\overline{CLR}$ = L, D = H

TURN-OFF DELAY, CLEAR TO OUTPUT



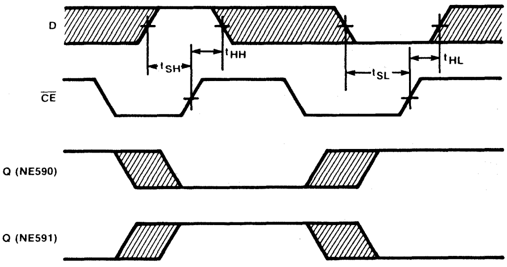
Other Inputs: $\overline{CE}$ = H, $\overline{CS}$ = H

SETUP TIME, ADDRESS TO ENABLE



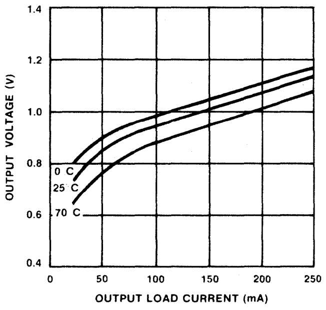
Other Inputs: $\overline{CLR}$ = H, $\overline{CS}$ = L

SETUP AND HOLD TIME, DATA TO ENABLE

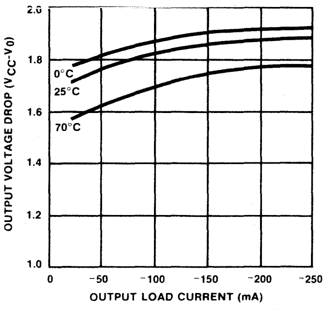


Other Inputs: $\overline{CLR}$ = H, A = Stable, $\overline{CS}$ = L

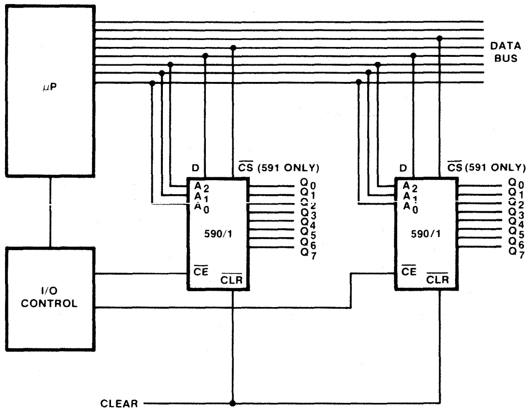
OUTPUT VOLTAGE VS LOAD CURRENT(NE590)



OUTPUT VOLTAGE DROP VS LOAD CURRENT(NE591)



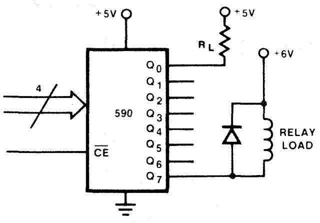
INTERFACING THE 590/591 WITH A MICROPROCESSOR SYSTEM



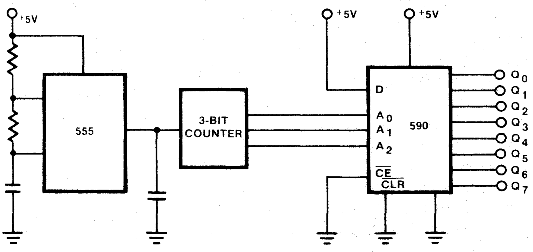
A_0, A_1, A_2, and $\overline{CS}$ may be connected to the address bus if permitted by system design.

TYPICAL APPLICATIONS (Cont'd)

NE590 DRIVING SIMPLE LOADS



NE590 OPERATING IN DEMULTIPLEX MODE



ADDRESSABLE RELAY DRIVER NE/SE5090

Preliminary

DESCRIPTION

The NE/SE5090 addressable relay driver is a high current latched driver, similar in function to the 9934 address decoder. The device has 8 open collector Darlington power outputs, each capable of 150mA load current. The outputs are turned on or off by respectively loading a logic "1" or logic "0" into the device data input. The required output is defined by a 3 bit address. The device must be enabled by a CE input line which also serves the function of further address decoding. A common clear input, CLR, turns all outputs off when a logic "0" is applied. The device is packaged in a 16 pin plastic or CERDIP package.

FEATURES

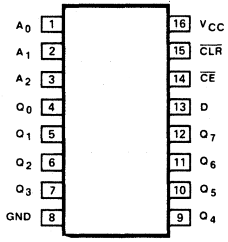
- **8 high current outputs**
- **Low-loading bus compatible inputs**
- **Power-on clear ensures safe operation**
- **Will operate in addressable or demultiplex mode**
- **Allows random (addressed) data entry**
- **Easily expandable**
- **Pin compatible with 9334**

APPLICATIONS

- **Relay driver**
- **Indicator lamp driver**
- **Triac trigger**
- **LED display digit driver**
- **Stepper motor driver**

PIN CONFIGURATION

F, N PACKAGE



TOP VIEW

ORDER NUMBERS

NE5090N
NE5090F
SE5090F

PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION
1-3	A0-A2	A 3-bit binary address on these pins defines which of the 8 output latches is to receive the data.
4-7, 9-12	Q0-Q7	The 8 device outputs.
13	D	The data input. When the chip is enabled, this data bit is transferred to the defined output such that: "1" turns output switch "ON" "0" turns output switch "OFF"
14	$\overline{CE}$	The chip enable. When this input is low, the output latches will accept data. When $\overline{CE}$ goes high, all outputs will retain their existing state, regardless of address or data input conditions.
15	$\overline{CLR}$	The clear input. When $\overline{CLR}$ goes low all output switches are turned "OFF". The high data input will override the clear function on the addressed latch.

TRUTH TABLE $-55 \leq T_A \leq +125°C, V_{CC} = 4.5V$

INPUTS						OUTPUTS								MODE
$\overline{CLR}$	$\overline{CE}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
L	H	X	X	X	X	H	H	H	H	H	H	H	H	Clear
L	L	L	L	L	L	H	H	H	H	H	H	H	H	Demultiplex
L	L	H	L	L	L	L	H	H	H	H	H	H	H	
L	L	L	H	L	L	H	H	H	H	H	H	H	H	
L	L	H	H	L	L	H	L	H	H	H	H	H	H	
L	L	L	H	H	H	H	H	H	H	H	H	H	H	
L	L	H	H	H	H	H	H	H	H	H	H	H	L	
H	H	X	X	X	X	Q_{N-1} →								Memory
H	L	L	L	L	L	H	Q_{N-1} →							Addressable Latch
H	L	H	L	L	L	L	Q_{N-1} →							
H	L	L	H	L	L	Q_{N-1}	H	Q_{N-1} →						
H	L	H	H	L	L	Q_{N-1}	L	Q_{N-1}						
H	L	L	H	H	H	Q_{N-1} →							H	
H	L	H	H	H	H	Q_{N-1} →							L	

X = Don't care condition
Q_{N-1} = Previous output state
L = Low voltage level/"ON" output state
H = High voltage level/"OFF" output state

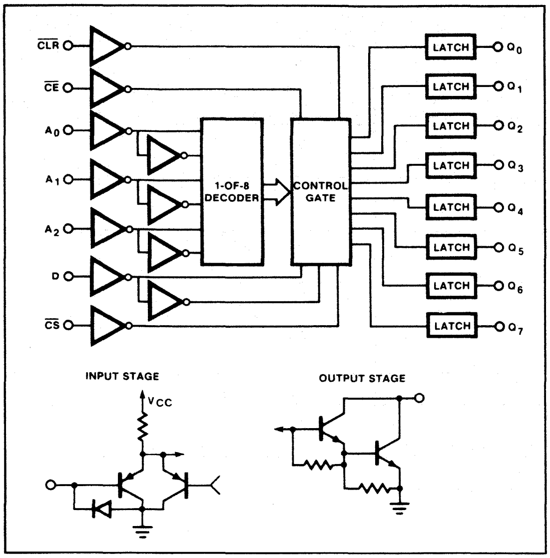
ANALOG DIVISION MARCH 1982

ADDRESSABLE RELAY DRIVER

NE/SE5090

Preliminary

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

$T_A = 25°C$ unless otherwise specified.

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7	V
V_{IN}	Input voltage	−0.5 to +15	V
V_{OUT}	Output voltage	0 to +30	V
I_{GND}	Ground current	500	mA
I_{OUT}	Output current Each output	200	mA
P_D	Power dissipation[1]	1	W
Ambient temperature range			°C
T_A	SE5090	−55 to +125	
T_A	NE5090	0 to +70	
T_J	Junction	150	
T_{STG}	Storage	−65 to +150	
T_{sold}	Lead soldering temperature (10 sec max)	300	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5V to 5.5V, −55°C ≤ T_A ≤ 125°C unless otherwise specified (SE5090)[2].
V_{CC} = 4.75V to 5.25V, 0°C ≤ T_A ≤ 70°C unless otherwise specified (NE5090)[2].

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IH}	High		2.0			
V_{IL}	Low				0.8	
	Output voltage					V
V_{OL}	Low	I_{OL} = 150mA, T_A = 25°C		1.05	1.30	
		Over temperature			1.50	
	Input current					μA
I_{IH}	High	$V_{IN} = V_{CC}$		<1.0	10	
I_{IL}	Low	V_{IN} = 0V		−3.0	−250	
I_{OH}	Leakage current	V_{OUT} = 28V,		5	250	μA
	Supply current	V_{CC} = 5.5V SE5090				mA
I_{CCL}	All outputs low	= 5.25V NE5090		35	60	
I_{CCH}	All outputs high			22	50	

NOTES

1. Derate power dissipation as indicated above threshold ambient temperature
   NE/SE5090 N at 95°C/W above 55°C
   NE/SE5090 F at 100°C/W above 50°C
2. All typical values are at V_{CC} = 5V and T_A = 25°C

ADDRESSABLE RELAY DRIVER NE/SE5090

Preliminary

SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$, $V_{OUT} = 5V$, $I_{OUT} = 100mA$, $V_{IL} = 0.8V$, $V_{IH} = 2.0V$

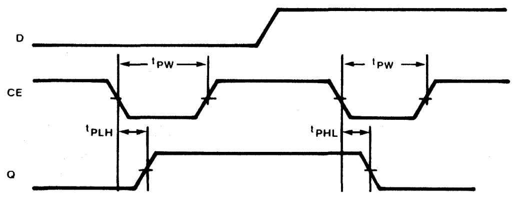
PARAMETER		TO	FROM	Min	Typ	Max	UNIT
 t_{PLH} t_{PHL}	Propagation delay time Low to high[1] High to low[1]	Output	$\overline{CE}$		900 130		ns
t_{PLH} t_{PHL}	Low to high[2] High to low[2]	Output	Data		920 130		ns
t_{PLH} t_{PHL}	Low to high[3] High to low[3]	Output	Address		900 130		ns
t_{PLH} t_{PHL}	Low to high[4] High to low[4]	Output	$\overline{CLR}$		920		ns
SWITCHING SETUP REQUIREMENTS							
$t_{s(H)}$[5] $t_{s(L)}$[5]		Chip enable Chip enable	High data Low data		40 40		ns
$t_{s(A)}$[6]		Chip enable	Address		20		ns
$t_{h(H)}$[5] $t_{H(L)}$[5]		Chip enable Chip enable	High data Low data		0 0		ns
$t_{pw(E)}$[1]	Chip enable pulse width[1]				20		ns

NOTES

1. See Turn-On and Turn-Off Delays, Enable to Output and Enable Pulse Width timing diagram.
2. See Turn-On and Turn-Off Delays, Data to Output timing diagram.
3. See Turn-On and Turn-Off Delays, Address to Output timing diagram.
4. See Turn-Off Delay, Clear to Output timing diagram.
5. See Setup and Hold Time, Data to Enable timing diagram.
6. See Setup Time, Address to Enable timing diagram.

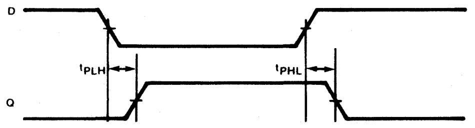
TIMING DIAGRAMS

TURN-ON AND TURN-OFF DELAYS, ENABLE TO OUTPUT AND ENABLE PULSE WIDTH



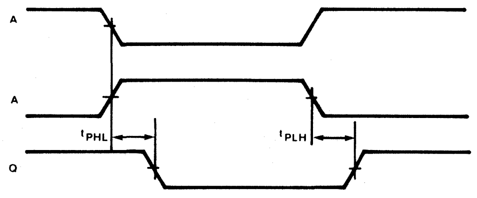
Other Inputs: $\overline{CLR}$ = H, A = Stable,

TURN-ON AND TURN-OFF DELAYS, DATA TO OUTPUT



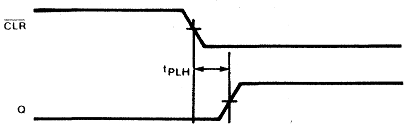
Other Inputs: $\overline{CE}$ = L, $\overline{CLR}$ = H, A = Stable

TURN-ON AND TURN-OFF DELAYS, ADDRESS TO OUTPUT



Other Inputs: $\overline{CE}$ = L, $\overline{CLR}$ = L, D = H

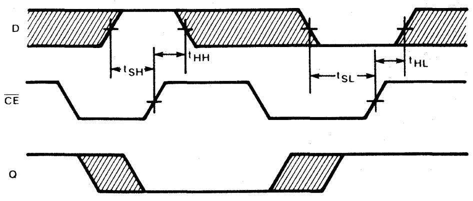
TURN-OFF DELAY, CLEAR TO OUTPUT



Other Inputs: $\overline{CE}$ = H,

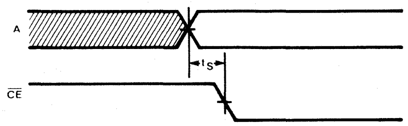
TIMING DIAGRAMS (Cont'd)

SETUP AND HOLD TIME, DATA TO ENABLE



Other Inputs: $\overline{CLR}$ = H. A = Stable.

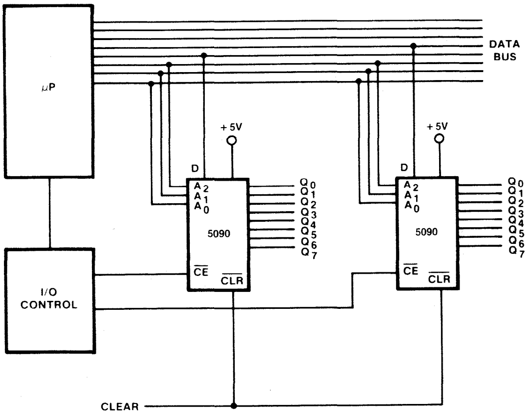
SETUP TIME, ADDRESS TO ENABLE



Other Inputs: $\overline{CLR}$ = H.

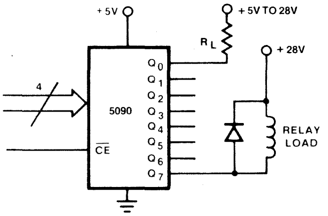
TYPICAL APPLICATIONS

INTERFACING WITH A MICROPROCESSOR SYSTEM

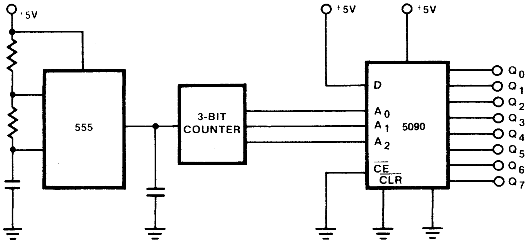


A_0, A_1, A_2, may be connected to the address bus if permitted by system design.

DRIVING SIMPLE LOADS



OPERATING IN DEMULTIPLEX MODE

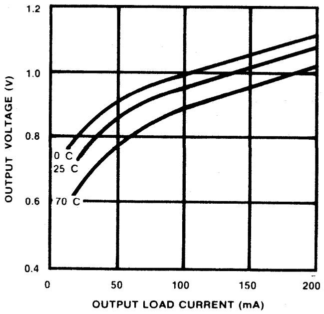


ADDRESSABLE RELAY DRIVER NE/SE5090

Preliminary

TYPICAL PERFORMANCE CHARACTERISTICS

OUTPUT VOLTAGE VS LOAD CURRENT



Section 10
Display Drivers

Signetics

INDEX

Section 10 — Display Drivers

DISPLAY DRIVER—SYMBOLS AND DEFINITIONS

T_A

Ambient temperature range. Range of the surrounding environment of the operating device.

T_J

Junction Temperature. The maximum temperature of the device. 150°C is standard for silicon devices.

T_{STG}

Storage temperature range. Temperature range that the device can be stored in a non-operating condition.

T_{SOLD}

Soldering Temperature. The temperature which can be applied to the lead frame of the device for short periods of time (normally specified for a duration of 10 sec).

Truth Tables

0 is logic level low
1 is logic level high
X - don't care condition - has no effect under circuit conditions listed.

Absolute Maximum Rating

Operating safe zones exceeding these limits could cause permanent damage to the device and are not meant to imply that devices can operate at these limits.

Power Dissipation

The power that the device can safely handle at 25°C. The dissipation must be derated as indicated for the individual package type.

Package Type Designation

See full package designations in Appendix.

V_{CC} ($-V_{CC}$)

Supply Voltage. The range of power supply voltage over which the device will operate safely.

LED

Light Emitting Diode

$\overline{XX}$

Negate Bar-when it appears over a function indicates that the "true" or valid condition of that function is a logic low level.

i.e. LE - would require a logic high level to cause a latch enable.
$\overline{LE}$ - would require a logic low level to cause a latch enable.

I_{SEG}

Segment Current. The amount of current supplied to each segment in a display. Current ratios are generally compared to segment 'b'.

BCD

Binary Coded Decimal

$\overline{BI}$/RBO

Blanking Input or Ripple Blanking Output.

$\overline{RBI}$

Ripple Blanking Input. The maximum clock frequency: the maximum input frequency at a clock input for the predictable performance. Above this frequency the device may cease to function.

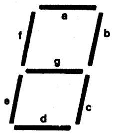
t_{PLH}

Propagation Delay Time. The time between the specified reference points on the input and output waveforms with the output changing from the defined LOW level to the defined HIGH level.

t_{PHL}

Propagation Delay Times. The time between the specified reference points on the input and output waveforms with the output changing from the defined HIGH level to the defined LOW level.

Segment Identification



t_h

Hold Time. The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the current logic level may be released prior to the active transition of the timing pulse and still be recognized.

t_s

Setup Time. The interval immediately preceeding the active transition of the timing pulse (usually the clock pulse) or preceeding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_W

Pulse Width. The time between the specified reference points on the leading and trailing edges of a pulse.

t_{rec}

Recovery Time. The time between the reference point on the trailing edge of an asynchronous input control pulse and the reference point on the activating edge of a synchronous (clock) pulse input such that the device will respond to the synchronous input.

V_S

Source Voltage. A separate V_{CC} line depending on part type.

I_{OH}

Output Current Source the device can supply while maintaining a specified voltage output level.

Typical Value

The typical value of a particular parameter determined by characterization of the device or sampling. Usually indicates that the particular device is not 100% tested for the parameter because it does not vary or can be determined by design and other tested variables. Occasionally typical values are given rather than min-

DISPLAY DRIVER—SYMBOLS AND DEFINITIONS

DISPLAY DRIVER DEFINITIONS (Cont'd)

max values because 100% testing would raise the cost of the product to a prohibitive level. If a typical value must be guaranteed to ensure specific operation, custom testing can often be provided at an additional cost to the user.

I_S

Source Current. Current flowing into the V_S supply terminal of the device with specified operating conditions.

Duty Cycle

Ratio of time on to time off. Generally expressed in percentage.

V_F

Forward voltage drop of a device at a specified current level.

I_B

Input Bias Current Current into an analog circuit input, specified at a particular voltage level.

CLR

Clear. Clear command will preset all internal circuits to a predetermined state.

CE

Chip Enable.

V_{IH}

Input High Voltage. The range of input voltages recognized by the device as a logic high.

V_{IL}

Input Low Voltage. The range of input voltages recognized by the device as a logic low.

V_{OH}

Output High Voltage. The minimum guaranteed High voltage at an output terminal for the specified output current I_{OH} and at the minimum V_{CC} value.

V_{OL}

Output Low Voltage. The maximum guranteed low voltage at an output terminal sinking the specified load current I_{OL}.

V_{BR}

Output Breakdown Voltage. Maximum voltage applied to a disabled (off) output to ensure a leakage current less than the specified value.

V_{IN}

The range of voltage on any input which the device can safely handle or a specified input voltage to the device.

V_{OUT}

The range of voltage on any output which the device can safely handle or a specified output voltage to the device.

$I_{CC}(-I_{CC})$

Supply Current. The current flowing into the $+V_{CC}$ $(-V_{CC})$ supply terminal of the circuit with specified input conditions and open outputs. Input conditions are chosen to guarantee worst case operation unless specified.

I_{IH}

Input High Current. The Current flowing into or out of an input when a specified High level voltage is applied to that input.

I_{IL}

Input Low Current. The current flowing out of an input when a specified Low level voltage is applied to that input.

I_{OL}

Output Low Current. The current flowing into an output when a which is in the Low State.

I_{OS}

Output Short-Circuit Current. The current flowing out of an output which is in the High state when that output is short circuit to the ground.

I_{CEX}

Output Leakage Current. The current flowing out of or into a disabled (off) output with a specified High output voltage applied.

HEX UNIVERSAL DRIVER NE582-1

Preliminary

DESCRIPTION

The NE582-1 is a general interface device comprising a high current output transistor and drive circuitry in each of 6 elements. Each output transistor is individually capable of sinking 400mA with a typical saturation voltage of 0.5V. Input loading is such that direct interfacing with P-MOS, N-MOS, C-MOS or TTL is possible.

The NE582-1 has applications as a LED display driver, low voltage relay/lamp drivers and many others where high current capability without speed constraints is required.

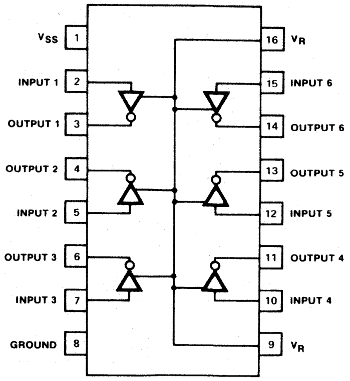
The NE582-1 is supplied in a 16-pin high dissipation dual-in-line plastic package.

FEATURES

- **Low saturation voltage (typically 0.5V) for minimum power dissipation**
- **High output sink current capability—400mA**
- **Low input current loading for MOS compatibility**
- **Low standby power consumption**
- **Suitable for 3 volt battery operation**
- **Inputs/outputs are compatible with 75494**

PIN CONFIGURATION

N PACKAGE



TOP VIEW
ORDER NUMBER
NE582-1N

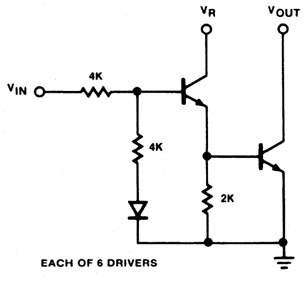
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Input voltage range[1]	-12 to V_{SS}	V
Output voltage[2]	15	V
Output to input voltage differential	10	V
Voltage at V_{SS} (pin 1)	10	V
Output current—each output	400	mA
Output current—all outputs	800	mA
Continuous total power dissipation at or below 25°C[3]	800	mW
Current in V_R (pin 9 or 16)	25	mA
Operating free-air temperature range	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature 1/16 inch from case for 10sec	260	°C

NOTES

1. The inputs are the only pins which may be negative with respect to ground.
2. Voltage values are with respect to ground.
3. Above 25°C, derate power dissipation at 6.25mW/°C.

EQUIVALENT SCHEMATIC



HEX UNIVERSAL DRIVER NE582-1

Preliminary

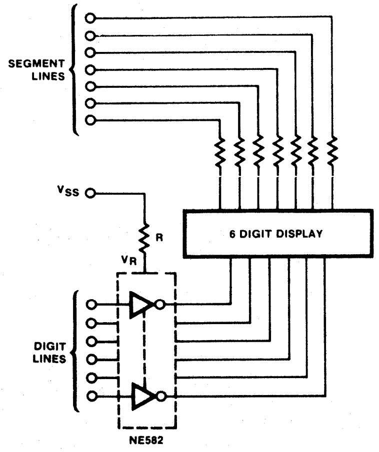
ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $70°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{OL}	Low level output voltage	V_{IN} I_R I_{OL} V mA mA 3.2 6.0 150 $R_{IN} = 1K$ (Series input resistance)		.500	.750	V
I_{OH}	High level output current	$V_{OH} = 15V$, $V_{IN} = 0.1V$			50	μA
I_{IN}	Input current at maximum Input voltage	$V_{IN} = 10V$, $I_{OL} = 20mA$, $I_R = 2mA$		2.2	3.3	mA
V_R		$V_{IN} = 6.5V$, $I_R = 6mA$, $I_{OL} = 80mA$		.9	1.5	V
I_{SS}	Current into pin 1	$V_{SS} = 10V$			100	μA

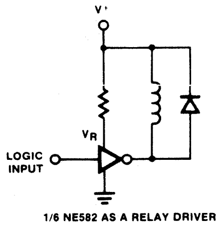
AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
T_{PLH}	Switching characteristics Propagation delay, low to high level input	$R_R = 680\Omega$ $R_L = 39\Omega$ $C_L = 15pF$		600		ns
T_{PHL}	Propagation delay, high to low level input	$V_{IH} = 7.5V$ $V_{IL} = 0V$ $t_r = t_f \leq 10ns$ $t_w = 1\mu s$ PRR = 100kHz		50		ns

TYPICAL APPLICATION FOR DIGIT DRIVING OF AN LED DISPLAY



1/6 NE582 AS A RELAY DRIVER

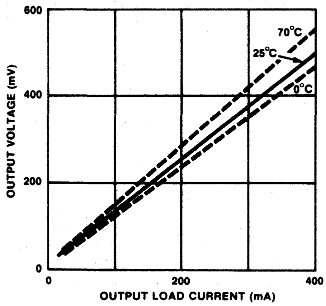


1/6 NE582 AS A RELAY DRIVER

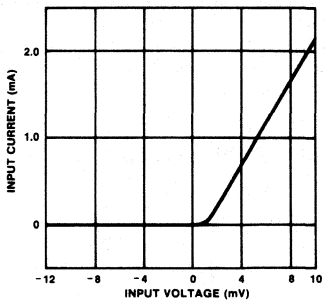
Preliminary

PRELIMINARY SPECIFICATION

OUTPUT SATURATION VOLTAGE AS A FUNCTION OF OUTPUT LOAD CURRENT,
I_R = 25mA
V_{IN} = 6.5 VOLTS



INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE,
I_R = 25mA, V_{SS} = 10V, T_A = 25°C



LED DECODER/DRIVER NE587

DESCRIPTION

The NE587 is a latch/decoder/driver for 7-segment common anode LED displays. The NE587 has a programmable current output up to 50mA which is essentially independent of output voltage, power supply voltage, and temperature. The data (BCD) inputs and $\overline{\text{LE}}$ (latch enable) input are low-loading so that they are compatible with any data bus system. The 7-segment decoding is implemented with a ROM so that alternative fonts can be made available.

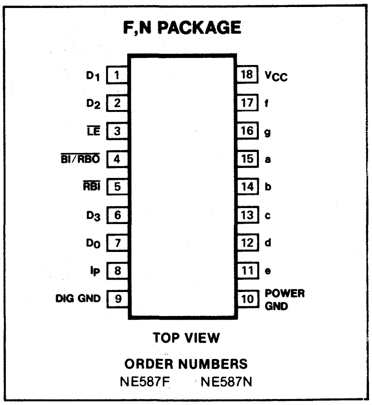
FEATURES

- **Latched BCD inputs**
- **Low loading bus-compatible inputs**
- **Ripple-blanking on leading and/or trailing edge zeros**

APPLICATIONS

- **Digital panel meters**
- **Measuring instruments**
- **Test equipment**
- **Digital clocks**
- **Digital bus monitoring**

PIN CONFIGURATIONS

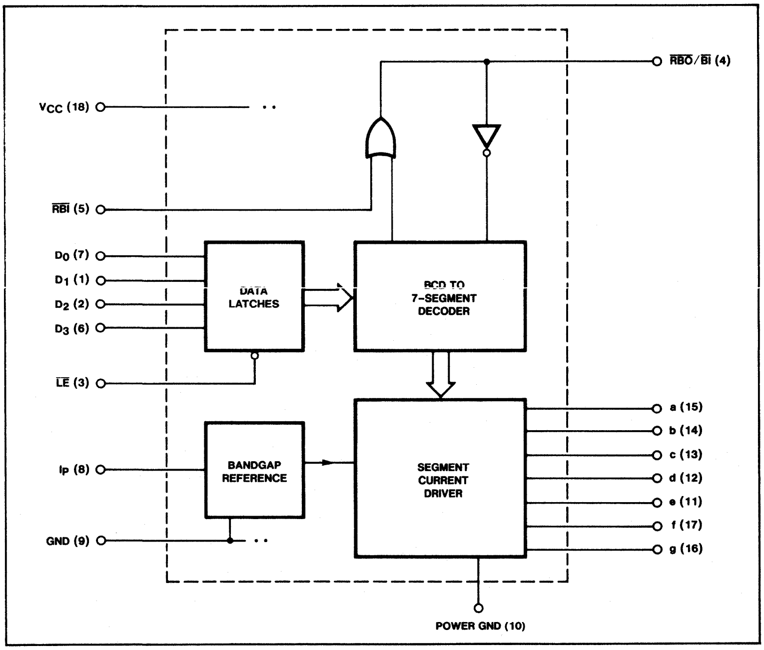


ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise specified

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7	V
V_{IN}	Input voltage (D_0 - D_3, $\overline{\text{LE}}$, $\overline{\text{RBI}}$)	−0.5 to +15	V
V_{OUT}	Output voltage (a-g, RBO)	−0.5 to +7	V
P_D	Power dissipation (25°C)[1]	1000	mW
T_A	Ambient temperature range	0 to 70	°C
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Soldering temperature (10 sec. max)	300	°C

NOTE
Derate power dissipation as indicated
N package - 95°C/watt above 55°C
F package - 100°C/watt above 50°C

BLOCK DIAGRAM



LED DECODER/DRIVER NE587

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 4.75 to 5.25V, 0°C $< T_A <$ 70°C.
Typical values are at V_{CC} = 5V, T_A = 25°C, R_P = 1kΩ (± 1%) unless otherwise stated.

PARAMETER		TEST CONDITIONS	NE587			UNIT
			Min	Typ	Max	
V_{CC}	Operating supply voltage		4.75	5.00	5.25	V
V_{IH}	Input high voltage	All Inputs except $\overline{BI}$	2.0		15	V
		$\overline{BI}$	2.0		5.5	
V_{IL}	Input low voltage				0.8	V
V_{IC}	Input clamp voltage	$I_{IN} = -12mA$, T_A = 25°C			−1.5	V
I_{IH}	Input high current	Inputs $D_0 - D_3$, $\overline{LE}$, $\overline{RBI}$				μA
		V_{IN} = 2.4V		1.0	10	
		V_{IN} = 15V		15	15	
		Input $\overline{BI}$ (pin 4)		10	100	μA
		$\overline{RBI}$ = H				
		$V_{IN} = V_{CC}$ = 5.25V				
I_{IL}	Input low current	V_{IN} = 0.4V, Inputs $D_0 - D_3$		−5		μA
		$\overline{LE}$, $\overline{RBI}$		−200		
		Input $\overline{BI}$		−0.7		
		V_{CC} = 5.25V				
		$\overline{RBI}$ = H, V_{IN} = 0.4V				mA
V_{OL}	Output low voltage	Output $\overline{RBO}$				
		I_{out} = 3.0mA		.2	.5	V
V_{OH}	Output high voltage	Output $\overline{RBO}$				
		$I_{OUT} = -50\mu A$	3.5	4.5		V
		$\overline{RBI}$ = H				
I_{OUT}	Output segment "ON" current	Outputs "a" thru "g" V_{OUT} = 2.0V	20	25	30	mA
ΔI_{OUT}	Output current ratio (all outputs ON)	With reference to "b" segment V_{OUT} = 2.0V	0.90	1.00	1.10	
I_{OFF}	Output segment "OFF" current	Outputs "a" thru "g" V_{OUT} = 5.0V		20	250	μA
I_{CCO}	Supply current	V_{CC} = 5.25V All outputs "ON" $V_{OUT} >$ 1V		33	55	mA
I_{CCI}	Supply current	V_{CC} = 5.25V All outputs blanked		50	70	mA

NOTE
NE587 PROGRAMMING
The NE587 output current can be programmed, provided a program resistor, Rp, be connected between Ip (pin 8) and Ground (pin 9). The voltage at Ip (pin 8) is constant (≈1.3V). Thus, a current through Rp is Ip $\approx \frac{1.3V}{Rp}$, as shown in Figure 5. $\frac{Io}{Ip}$ is 20 in the 15 to 50mA output current range.

LED DECODER/DRIVER NE587

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 5V$ $T_A = 25°C$. $R_L = 130\Omega$, $C_L = 30pF$ including probe capacity.

PARAMETER		TEST CONDITIONS	NE587			UNIT
			Min	Typ	Max	
$t_{D_{av.}}$	Propagation delay Figure 2	From data to output		135		ns
$t_{D_{av.}}$	Propagation delay Figure 3	From $\overline{LE}$ to output		135		ns
t_W	Latch enable pulse width Figure 4		30			ns
t_S	Latch enable setup time Figure 4	From data to $\overline{LE}$	20			ns
t_H	Latch enable hold time Figure 4	From $\overline{LE}$ to data	0			ns

NOTE

$t_{D_{av.}} = ½ (t_{HL} + t_{LH})$

TRUTH TABLE

BINARY INPUT	INPUTS						OUTPUTS								DISPLAY
	$\overline{LE}$	$\overline{RBI}$	D_3	D_2	D_1	D_0	a	b	c	d	e	f	g	$\overline{RBO}$	
–	H	*	X	X	X	X	STABLE							**	STABLE
0	L	L	L	L	L	L	H	H	H	H	H	H	H	L	BLANK
0	L	H	L	L	L	L	L	L	L	L	L	L	H	H	0
1	L	X	L	L	L	H	H	L	L	H	H	H	H	H	1
2	L	X	L	L	H	L	L	L	H	L	L	H	L	H	2
3	L	X	L	L	H	H	L	L	L	L	H	H	L	H	3
4	L	X	L	H	L	L	H	L	L	H	H	L	L	H	4
5	L	X	L	H	L	H	L	H	L	L	H	L	L	H	5
6	L	X	L	H	H	L	L	H	L	L	L	L	L	H	6
7	L	X	L	H	H	H	L	L	L	H	H	H	H	H	7
8	L	X	H	L	L	L	L	L	L	L	L	L	L	H	8
9	L	X	H	L	L	H	L	L	L	L	H	L	L	H	9
10	L	X	H	L	H	L	H	H	H	H	H	H	L	H	-
11	L	X	H	L	H	H	L	H	H	L	L	L	L	H	E
12	L	X	H	H	L	L	H	L	L	H	L	L	L	H	H
13	L	X	H	H	L	H	H	H	H	L	L	L	H	H	L
14	L	X	H	H	H	L	L	L	H	H	L	L	L	H	P
15	L	X	H	H	H	H	H	H	H	H	H	H	H	H	blank
**BI	X	X	X	X	X	X	H	H	H	H	H	H	H	L**	blank

NOTES

H = HIGH voltage level, output is "OFF"

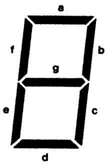
L = LOW voltage level, output is "ON"

X = Don't care

* The $\overline{RBI}$ will blank the display only if a binary zero is stored in the latches.

** $\overline{RBO/BI}$ used as an input overrides all other input conditions.

SEGMENT IDENTIFICATION



NE587 PROGRAMMING

NE587 output current can be programmed by using a programming resistor, R_P, connected between r_P (pin 8) and Gnd (pin 9). The voltage at r_P (pin 8) is constant ($\approx$1.40V). A partial schematic of the voltage reference used in the NE587 is shown in figure 1.

Output current to program current ratio, I_O/I_P, is 20 in the 15mA to 50mA range. Note that I_P must be derived from a resistor (R_P), and not from a high impedance source such as an I_{OUT} DAC used to control display brightness.

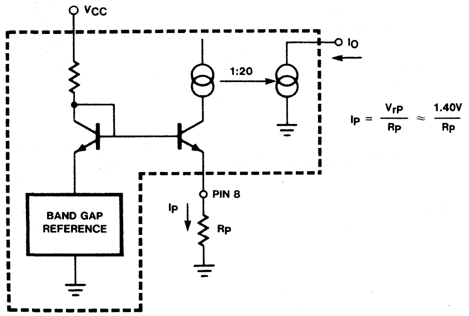


Figure 1

TIMING DIAGRAMS

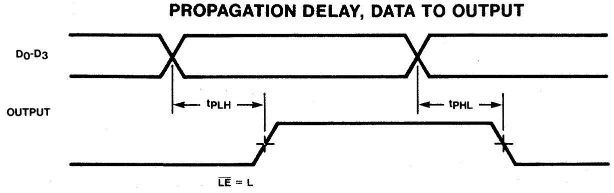


Figure 2

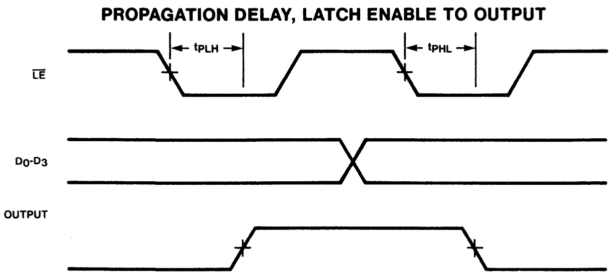


Figure 3

POWER DISSIPATION CONSIDERATIONS

LED displays are power-hungry devices, and inevitably somewhat inefficient in their use of the power supply necessary to drive them. Duty cycle control does afford one way of improving display efficiency, provided that the LEDS are not driven too far into saturation, but the improvement is marginal. Operation at higher peak currents has the added advantage of giving much better matching of light output, both from segment-to-segment and digit-to-digit.

An output current of 10 to 50mA was chosen so that it would be suitable for multiplexed operation of large size LED digits. When designing a display system, particular care must be taken to minimize power dissipation within the IC display driver. Since the output is a constant current source, all the remaining supply voltage, which is not dropped across the LED (and the digit driver, if used), will appear across the output. Thus, the power dissipation will go up sharply if the display power supply voltage rises. Clearly, then, it is good design practice to keep the display supply voltage as low as possible consistent with proper operation of the supply output current sources. Inserting a resistor or diode in series with the display supply is a good way of reducing the power dissipation within the integrated circuit segment driver, although, of course, total system power remains the same.

Power dissipation may be calculated as follows. Referring to figure 6, the two system power supplies are V_{CC} and V_S. In many cases, these will be the same voltage. Necessary parameters are:

V_{CC},	Supply voltage to driver
V_S,	Supply voltage to display
I_{CC},	Quiescent supply current of driver
I_{SEG},	LED segment current
V_F,	LED segment forward voltage at I_{seg}
K_{DC},	% Duty cycle

V_F, the forward LED drop, depends upon the type of LED material (hence the color) and the forward current. The actual forward voltage drops should be obtained from the LED display manufacturer's literature for the peak segment current selected; however, approximate voltages at nominal rated currents are:

Red	1.6 to 2.0V
Orange	2.0 to 2.5V
Yellow	2.2 to 3.5V
Green	2.5 to 3.5V

TIMING DIAGRAMS (Cont'd)

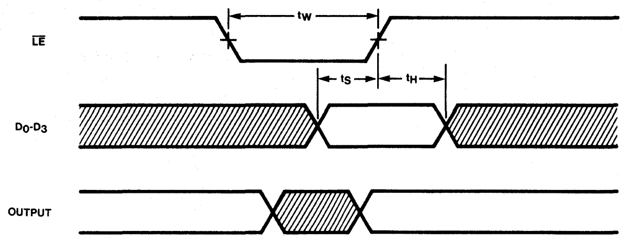


Figure 4

These voltages are all for single diode displays. Some early red displays had 2 series LEDS per segment; hence the forward voltage drop was around 3.5V.

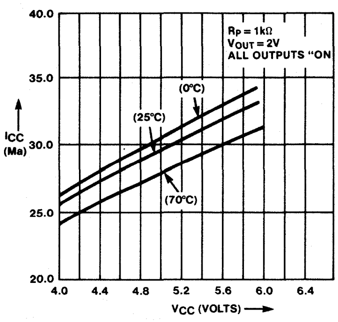
Thus a maximum power dissipation calculation when all segments are on, is:

$P_d = V_{CC} \times I_{CC} + (V_S - V_F) \times 7 \times I_{seg} \times K_{DC}$ mW

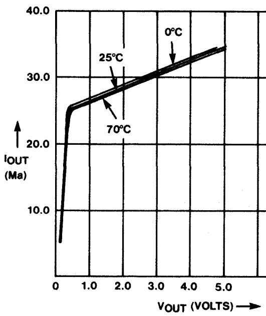
Assuming $V_S = V_{CC} = 5.25V$
$V_F = 2.0V$
$K_{DC} = 100\%$
$P_{d\,max} = 5.25 \times 50 + 3.25 \times 7 \times 30$ mW
$= 945$ mW

TYPICAL PERFORMANCE CURVES

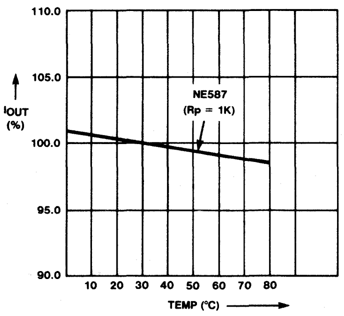
SUPPLY CURRENT VS SUPPLY VOLTAGE
NE587



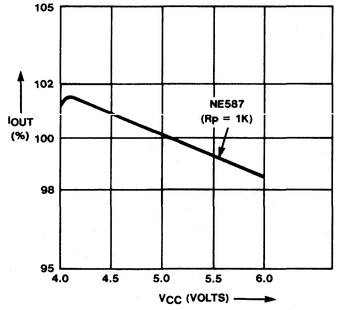
OUTPUT CURRENT VS OUTPUT VOLTAGE
NE587
Rp = 1Kohms



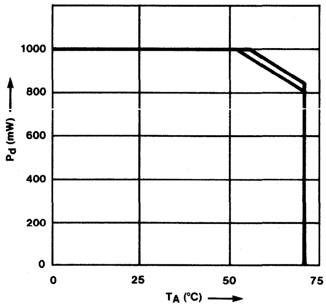
NORMALIZED OUTPUT CURRENT VS TEMPERATURE
$V_{CC} = 5.0V$



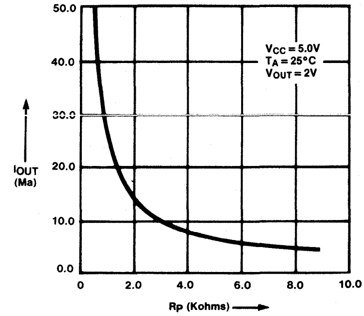
NORMALIZED OUTPUT CURRENT VS SUPPLY VOLTAGE
$V_O = 2V$
$T_A = 25°C$



MAXIMUM POWER DISSIPATION VS TEMPERATURE

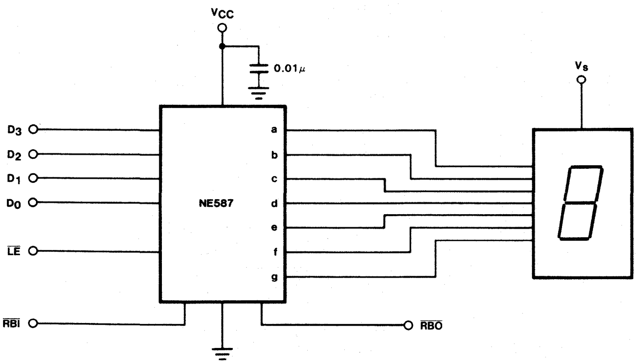


OUTPUT CURRENT VS PROGRAM RESISTOR



TYPICAL APPLICATIONS

DRIVING A SINGLE DIGIT



NOTE
Decoupling capacitor on V_{CC} should be 0.01 µF ceramic

Figure 6

However, the average power dissipation will be considerably less than this. Assuming 5 segments are on (the average for all output code combinations), then

$$P_{d\ av} = 5.0 \times 30 + 3.00 \times 5 \times 25 \text{ mW}$$
$$= 525 \text{ mW}$$

Operating temperature range limitations can be deduced from the power dissipation graph. (See Typical Performance Characteristics).

However, a major portion of this power dissipation ($P_{d\ max}$) is because the current source output is operating with 3.25 V across it. In practice, the outputs operate satisfactorily down to 0.5V, and so the extra voltage may be dropped external to the integrated circuit.

Suppose the worst case V_{CC}/V_S supply is 4.75 to 5.25V, and that the maximum V_E for the LED display is 2.25V. Only 2.75V is required to keep the display active, and hence 2.0V may be dropped externally with a resistor from V_{CC} to V_S. The value of this resistor is calculated by:

$$R_S = \frac{2.0}{7 \times I_{seg}} \simeq 10\Omega \text{ (½ W rating)}$$

assuming worst case I_{seg} of 30 mA

Hence now $P_{d\ max} = V_{CC} \times I_{CC} + (V_S - V_V - R_X \times 7 \times I_{seg}) \times 7 \times X\, I_{seg} \times K_{DC}$
$= 5.25 \times 50 + 1.25 \times 7 \times 30$ mW
$= 525$ mW

and $P_{d\ av} = 5.0 \times 30 + 1.25 \times 5 \times 25$
$= 306$ mW

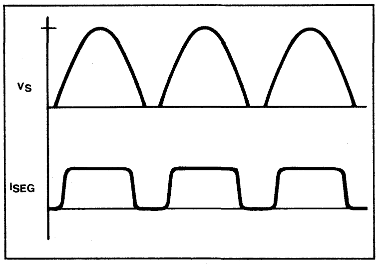
If a diode (or 2) is used to reduce voltage to the display, then the voltage appearing across the display driver will be independent of the number of "ON" segments and will be equal to

$$V_S - V_F - nV_d\,,\ V_D \simeq 0.8V$$

Where n is the number of diodes used, power dissipation can be calculated in a similiar manner.

In a multiplexed display system, the voltage drop across the digit driver must also be considered in computing device power dissipation. It may even be an advantage to use a digit driver which drops an appreciable voltage, rather than the saturating PNP transistors shown in figure 9. For example a darlington PNP or NPN emitter follower may be preferable. Figure 8 shows the NE591 as the digit driver in a multiplexed display system. The NE591 output drops about 1.8V which means that the power dissipation is evenly distributed between the two integrated circuits.

Where V_S and V_{CC} are two different supplies, the V_S supply may be optimized for minimum system power dissipation and/or cost. Clearly, good regulation in the V_S supply is totally unnecessary, and so this supply can be made much cheaper than the regulated 5V supply used in the rest of the system. In fact a simple unsmoothed full-wave rectified sine wave works extremely well if a slight loss in brightness can be tolerated. A transformer voltage of about 3-4.5V rms works well in most LED display systems. Waveforms are shown below:



The duty cycle for this system depends upon V_S, V_F and the output characteristics of the display driver.

With
$V_S = 4.9V$ pk.
$V_F = 2.0V$

The duty cycle is approximately 60%.

TYPICAL APPLICATIONS (Cont'd)

4-DIGIT DISPLAY WITH BRIGHTNESS CONTROL AND LEADING EDGE RIPPLE BLANKING

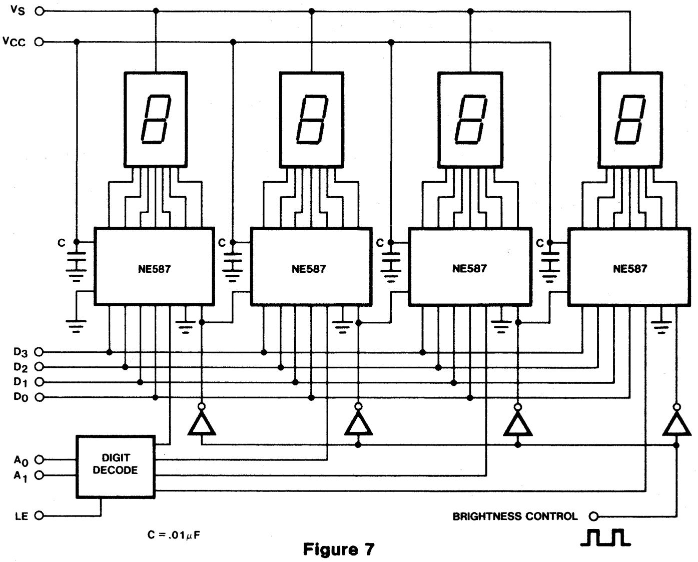


Figure 7

INTERFACING 8-DIGIT LED DISPLAY WITH μP BUS

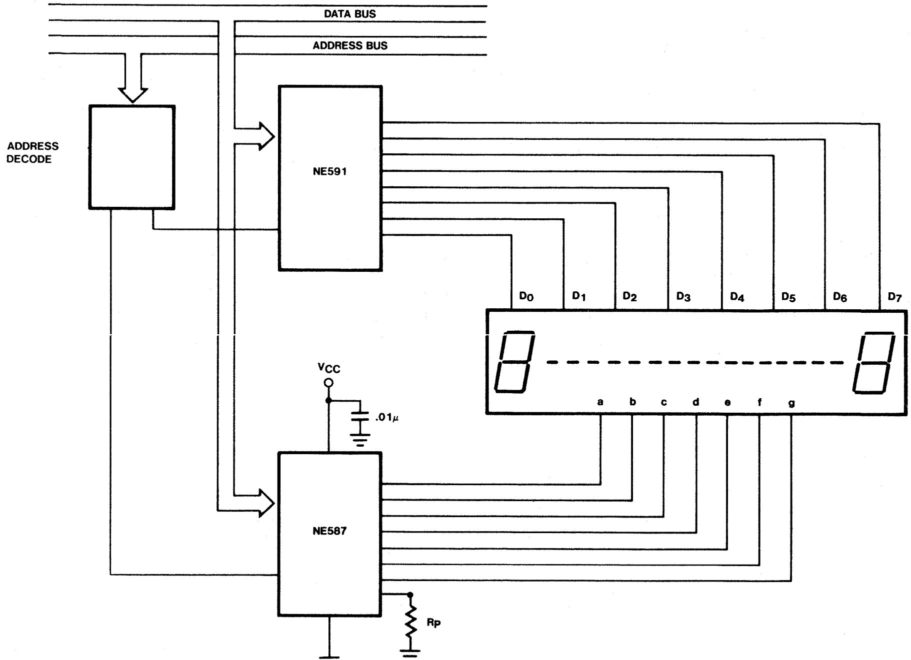


Figure 8

TYPICAL APPLICATIONS (Cont'd)

4-DIGIT MULTIPLEXED LED DISPLAY

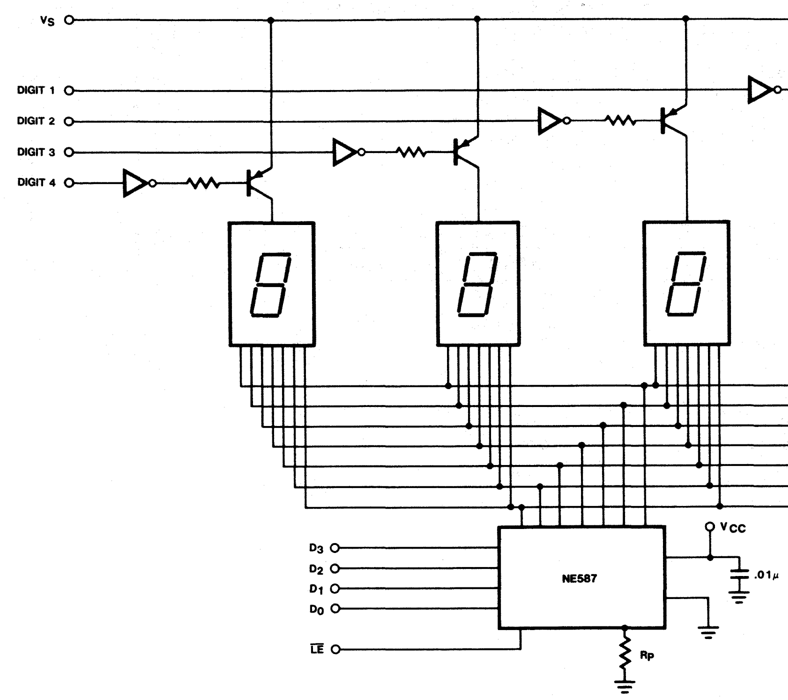


Figure 9

ANALOG DIVISION MARCH 1982

LED DECODER/DRIVER NE589

Preliminary

DESCRIPTION

The NE589 is a latch/decoder/driver for 7-segment common cathode LED displays. The NE589 has a programmable current output up to 50mA which is essentially independent of output voltage, power supply voltage, and temperature. The data (BCD) inputs and $\overline{LE}$ (latch enable) input are low-loading so that they are compatible with any data bus system. The 7-segment decoding is implemented with a ROM so that alternative fonts can be made available.

FEATURES

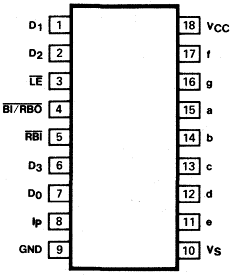
- **Latched BCD inputs**
- **Low loading bus-compatible inputs**
- **Ripple-blanking on leading and/or trailing edge zeros**

APPLICATIONS

- **Digital panel meters**
- **Measuring instruments**
- **Test equipment**
- **Digital clocks**
- **Digital bus monitoring**

PIN CONFIGURATION

F,N PACKAGE



TOP VIEW

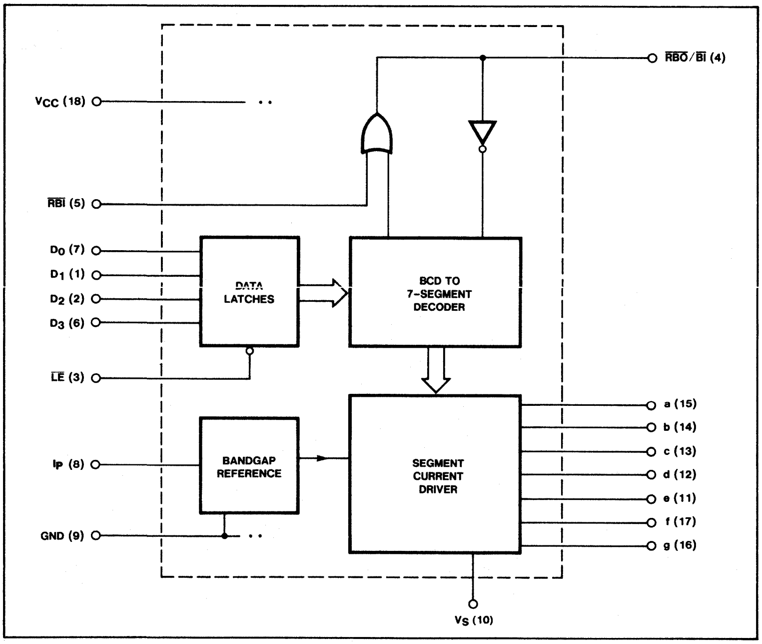
ORDER NUMBERS
NE589F NE589N

ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise specified

PARAMETER		RATING	UNIT
V_{CC}, V_S	Supply voltage	−0.5 to +7	V
V_{IN}	Input voltage (D_0 - D_3, $\overline{LE}$, $\overline{RBI}$)	−0.5 to +15	V
V_{OUT}	Output voltage (a-g, RBO)	−0.5 to +7	V
P_D	Power dissipation (25°C)[1]	1000	mW
T_A	Ambient temperature range	0 to 70	°C
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Soldering temperature (10 sec. max)	300	°C

NOTE
Derate power dissipation as indicated
N package - 95°C/watt above 55°C
F package - 100°C/watt above 50°C

BLOCK DIAGRAM



LED DECODER/DRIVER NE589

Preliminary

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 4.75 to 5.25V, 0°C < T_A < 70°C. Typical values are at $V_{CC} = V_S = 5V$, $T_A = 25°C$, $R_p = 7k\Omega$ (±1%) unless otherwise stated.

PARAMETER	TEST CONDITIONS	NE589			UNIT
		Min	Typ	Max	
V_{CC}, V_S Operating supply voltage		4.75	5.00	5.25	V
V_{IH} Input high voltage	All Inputs except $\overline{BI}$ $\overline{BI}$	2.0 2.0		15 5.5	V
V_{IL} Input low voltage				0.8	V
V_{IC} Input clamp voltage	$I_{IN} = -12mA$, $T_A = 25°C$			−1.5	V
I_{IH} Input high current	Inputs $D_0 - D_3$, $\overline{LE}$, $\overline{RBI}$ V_{IN} = 2.4V V_{IN} = 15V		0.1		µA µA
I_{IH} Input high current	Input $\overline{BI}$ (pin 4) $\overline{RBI}$ = H $V_{IN} = V_{CC}$ = 5.25V		10		µA
I_{IL} Input low current	V_{IN} = 0.4V, Inputs $D_0 - D_3$ $\overline{LE}$, $\overline{RBI}$		−5 −200		µA
I_{IL} Input low current	Input $\overline{BI}$ V_{CC} = 5.25V $\overline{RBI}$ = H, V_{IN} = 0.4V		−0.7		mA
V_{OL} Output low voltage	Output $\overline{RBO}$ I_{OUT} = 3.0mA				V
V_{OH} Output high voltage	Output $\overline{RBO}$ I_{OUT} = −50µA $\overline{RBI}$ = H		4.5		V
I_{OUT} Output segment "ON" current	Outputs "a" thru "g" V_{OUT} = 2.0V	20	25	30	mA
ΔI_{OUT} Output current ratio (all outputs ON)	With reference to "b" segment V_{OUT} = 2.0V	0.90	1.00	1.10	
I_{OFF} Output segment "OFF" current	Outputs "a" thru "g"		20	250	µA
I_{CCO} Supply current	V_{CC} = 5.25V All outputs "ON" $V_{OUT} > 1V$		25		mA
I_{CCI} Supply current	V_{CC} = 5.25V All outputs blanked		30		mA

LED DECODER/DRIVER NE589

Preliminary

AC ELECTRICAL CHARACTERISTICS $V_{CC} = V_S = 5V$ $T_A = 25°C$, $R_L = 130\Omega$, $C_L = 30pF$ including probe capacity.

PARAMETER		TEST CONDITIONS	NE589			UNIT
			Min	Typ	Max	
$t_{Dav.}$	Propagation delay Figure 2	From data to output		135		ns
$t_{Dav.}$	Propagation delay Figure 3	From $\overline{LE}$ to output		135		ns
t_W	Latch enable pulse width Figure 4		85			ns
t_S	Latch enable setup time Figure 4	From data to $\overline{LE}$	75			ns
t_H	Latch enable hold time Figure 4	From $\overline{LE}$ to data	0			ns

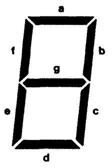
NOTE:
$t_{DAV.} = \max(t_{HL} + t_{LH})$

TRUTH TABLE

BINARY INPUT	INPUTS						OUTPUTS								DISPLAY
	$\overline{LE}$	$\overline{RBI}$	D_3	D_2	D_1	D_0	a	b	c	d	e	f	g	$\overline{RBO}$	
–	H	•	X	X	X	X	STABLE								STABLE
0	L	L	L	L	L	L	L	L	L	L	L	L	L	L	BLANK
0	L	H	L	L	L	L	H	H	H	H	H	H	L	H	0
1	L	X	L	L	L	H	L	H	H	L	L	L	L	H	1
2	L	X	L	L	H	L	H	H	L	H	H	L	H	H	2
3	L	X	L	L	H	H	H	H	H	H	L	L	H	H	3
4	L	X	L	H	L	L	L	H	H	L	L	H	H	H	4
5	L	X	L	H	L	H	H	L	H	H	L	H	H	H	5
6	L	X	L	H	H	L	H	L	H	H	H	H	H	H	6
7	L	X	L	H	H	H	H	H	H	L	L	L	L	H	7
8	L	X	H	L	L	L	H	H	H	H	H	H	H	H	8
9	L	X	H	L	L	H	H	H	H	H	L	H	H	H	9
10	L	X	H	L	H	L	H	H	H	L	H	H	H	H	a
11	L	X	H	L	H	H	L	L	H	H	H	H	H	H	b
12	L	X	H	H	L	L	H	L	L	H	H	H	L	H	c
13	L	X	H	H	L	H	L	H	H	H	H	L	H	H	d
14	L	X	H	H	H	L	H	L	L	H	H	H	H	H	e
15	L	X	H	H	H	H	H	L	L	L	H	H	H	H	f
• •BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L• •	blank

NOTES
H = HIGH voltage level, output is "ON"
L = LOW voltage level, output is "OFF"
X = Don't care
• The $\overline{RBI}$ will blank the display only if a binary zero is stored in the latches.
• • $\overline{RBO/BI}$ used as an input overrides all other input conditions.

SEGMENT IDENTIFICATION



Preliminary

NE589 PROGRAMMING

NE589 output current can be programmed by using a programming resistor, R_P, connected between r_P (pin 8) and Gnd (pin 9). The voltage at r_P (pin 8) is constant ($\approx$ 1.3V). A partial schematic of the voltage reference used in the NE589 is shown in figure 1.

Output current to program current ratio, I_O/I_P, is 120 in the 10mA to 50mA range. Note that I_P must be derived from a resistor (R_P), and not from a high impedance source such as an I_{OUT} DAC used to control display brightness.

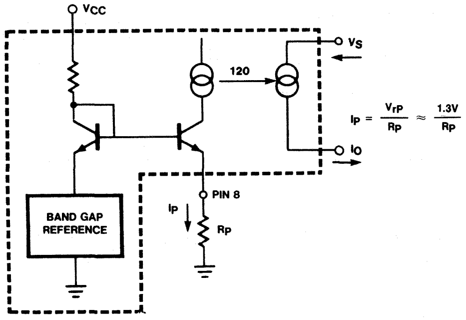


Figure 1

TIMING DIAGRAMS

PROPAGATION DELAY, DATA TO OUTPUT

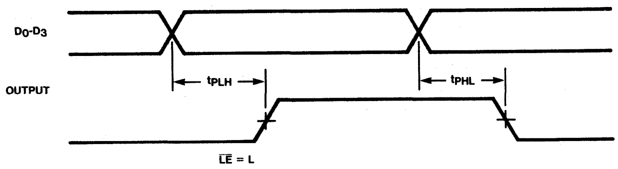


Figure 2

PROPAGATION DELAY, LATCH ENABLE TO OUTPUT

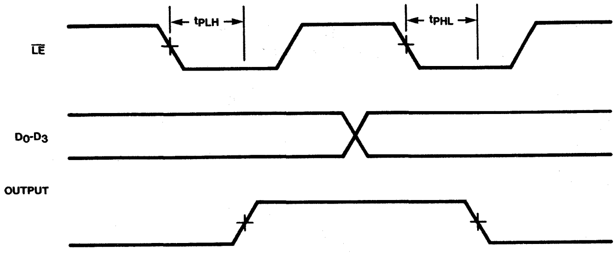


Figure 3

POWER DISSIPATION CONSIDERATIONS

LED displays are power-hungry devices, and inevitably somewhat inefficient in their use of the power supply necessary to drive them. Duty cycle control does afford one way of improving display efficiency, provided that the LEDS are not driven too far into saturation, but the improvement is marginal. Operation at higher peak currents has the added advantage of giving much better matching of light output, both from segment-to-segment and digit-to-digit.

An output current of 10 to 50mA was chosen so that it would be suitable for multiplexed operation of large size LED digits. When designing a display system, particular care must be taken to minimize power dissipation within the IC display driver. Since the output is a constant current source, all the remaining supply voltage, which is not dropped across the LED (and the digit driver, if used), will appear across the output. Thus, the power dissipation will go up sharply if the display power supply voltage rises. Clearly, then, it is good design practice to keep the display supply voltage as low as possible consistent with proper operation of the supply output current sources. Inserting a resistor or diode in series with the display supply is a good way of reducing the power dissipation within the integrated circuit segment driver, although, of course, total system power remains the same.

Power dissipation may be calculated as follows. Referring to figure 5, the two system power supplies are V_{CC} and V_S. In many cases, these will be the same voltage. Necessary parameters are:

V_{CC},	Supply voltage to driver
V_S,	Supply voltage to display
I_{CC},	Quiescent supply current of driver
I_{SEG},	LED segment current
V_F,	LED segment forward voltage at I_{seg}
K_{DC},	% Duty cycle

V_F, the forward LED drop, depends upon the type of LED material (hence the color) and the forward current. The actual forward voltage drops should be obtained from the LED display manufacturer's literature for the peak segment current selected; however, approximate voltages at nominal rated currents are:

Red	1.6 to 2.0V
Orange	2.0 to 2.5V
Yellow	2.2 to 3.5V
Green	2.5 to 3.5V

LED DECODER/DRIVER NE589

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TIMING DIAGRAMS (Cont'd)

LATCH ENABLE PULSE WIDTH, SET-UP AND HOLD TIMES

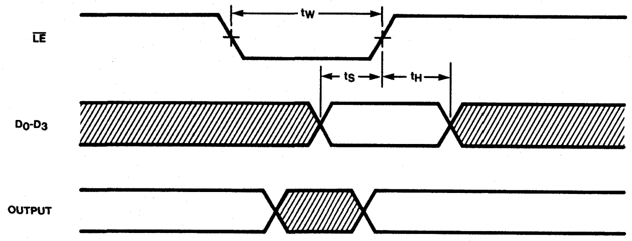


Figure 4

These voltages are all for single diode displays. Some early red displays had 2 series LEDS per segment; hence the forward voltage drop was around 3.5V.

Thus a maximum power dissipation calculation when all segments are on, is:

$P_d = V_{CC} \times I_{CC} + (V_S - V_F) \times 7 \times I_{seg} \times K_{DC}$ mW

Assuming $V_S = V_{CC} = 5.25V$

$V_F = 2.0V$

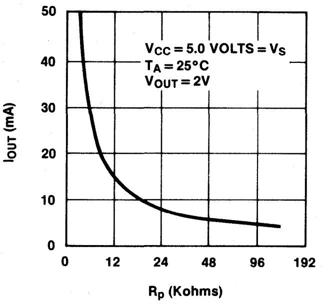
$K_{DC} = 100\%$

$P_{d\ max} = 5.25 \times 50 + 3.25 \times 7 \times 30$ mW

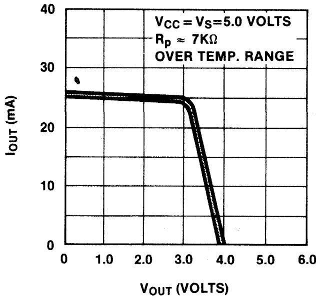
$= 945$ mW

TYPICAL PERFORMANCE CURVES

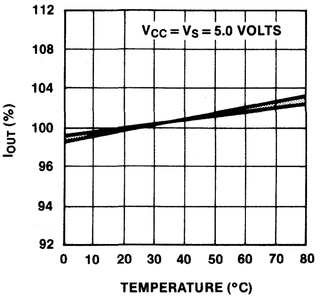
OUTPUT CURRENT VS PROGRAM RESISTOR



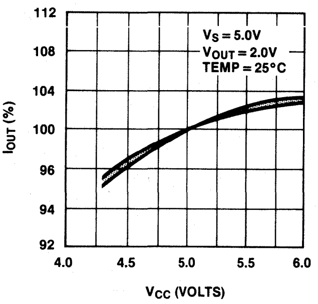
OUTPUT CURRENT VS OUTPUT VOLTAGE



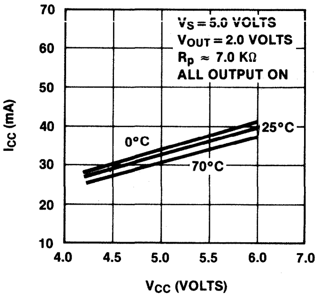
NORMALIZED OUTPUT CURRENT VS TEMPERATURE



NORMALIZED OUTPUT CURRENT VS SUPPLY VOLTAGE



SUPPLY CURRENT VS SUPPLY VOLTAGE



LED DECODER/DRIVER NE589

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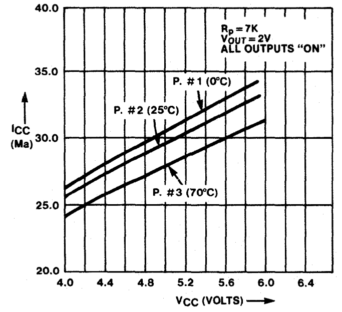
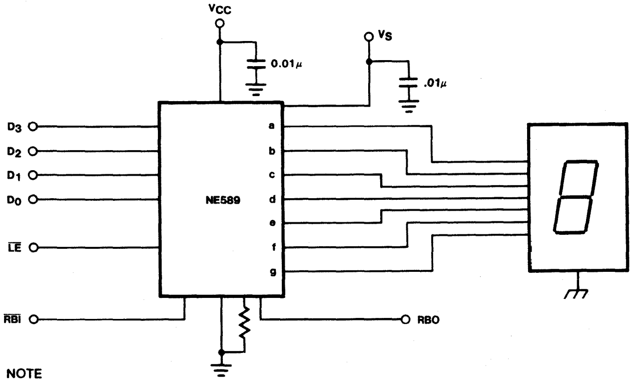
TYPICAL PERFORMANCE CURVES (Cont'd)

SUPPLY CURRENT VS SUPPLY VOLTAGE
NE589



TYPICAL APPLICATIONS

DRIVING A SINGLE DIGIT



NOTE
Decoupling capacitor on V_{CC} should be 0.01 µF ceramic

Figure 5

However, the average power dissipation will be considerably less than this. Assuming 5 segments are on (the average for all output code combinations), then

$P_{d\ av}$ = 5.0 × 30 + 3.00 × 5 × 25 mW
= 525 mW

Operating temperature range limitations can be deduced from the power dissipation graph in figure 9.

However, a major portion of this power dissipation ($P_{d\ max}$) is because the current source output is operating with 3.25 V across it. In practice, the outputs operate satisfactorily down to 0.5V, and so the extra voltage may be dropped external to the integrated circuit.

Suppose the worst case V_{CC}/V_S supply is 4.75 to 5.25V, and that the maximum V_E for the LED display is 2.25V. Only 2.75V is required to keep the display active, and hence 2.0V may be dropped externally with a resistor from V_{CC} to V_S. The value of this resistor is calculated by:

$$R_S = \frac{2.0}{7 \times I_{seg}} \simeq 10\Omega \text{ (½ W rating)}$$

assuming worst case I_{seg} of 30 mA

Hence now $P_{d\ max}$ = $V_{CC} \times I_{CC} + (V_S - V_V - R_X \times 7 \times I_{seg}) \times 7 \times X\ I_{seg} \times K_{DC}$
= 5.25 × 50 + 1.25 × 7 × 30 mW
= 525 mW

and $P_{d\ av}$ = 5.0 × 30 + 1.25 × 5 × 25
= 306 mW

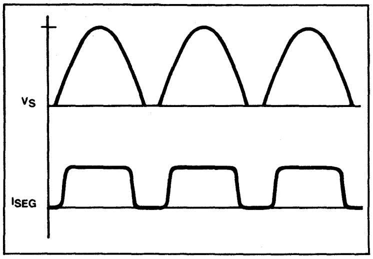
If a diode (or 2) is used to reduce voltage to the display, then the voltage appearing across the display driver will be independent of the number of "ON" segments and will be equal to

$V_S - V_F - nV_d$, $V_D \simeq 0.8V$

Where n is the number of diodes used, power dissipation can be calculated in a similiar manner.

In a multiplexed display system, the voltage drop across the digit driver must also be considered in computing device power dissipation. It may even be an advantage to use a digit driver which drops an appreciable voltage, rather than the saturating PNP transistors shown in figure 8. For example a darlington PNP or NPN emitter follower may be preferable. Figure 7 shows the NE591 as the digit driver in a multiplexed display system. The NE591 output drops about 1.8V which means that the power dissipation is evenly distributed between the two integrated circuits.

Where V_S and V_{CC} are two different supplies, the V_S supply may be optimized for minimum system power dissipation and/or cost. Clearly, good regulation in the V_S supply is totally unnecessary, and so this supply can be made much cheaper than the regulated 5V supply used in the rest of the system. In fact a simple unsmoothed full-wave rectified sine wave works extremely well if a slight loss in brightness can be tolerated. A transformer voltage of about 3-4.5V rms works well in most LED display systems. Waveforms are shown below:



The duty cycle for this system depends upon V_S, V_F and the output characteristics of the display driver.

With
V_S = 4.9V pk.
V_F = 2.0V

The duty cycle is approximately 60%.

Preliminary

TYPICAL APPLICATIONS (Cont'd)

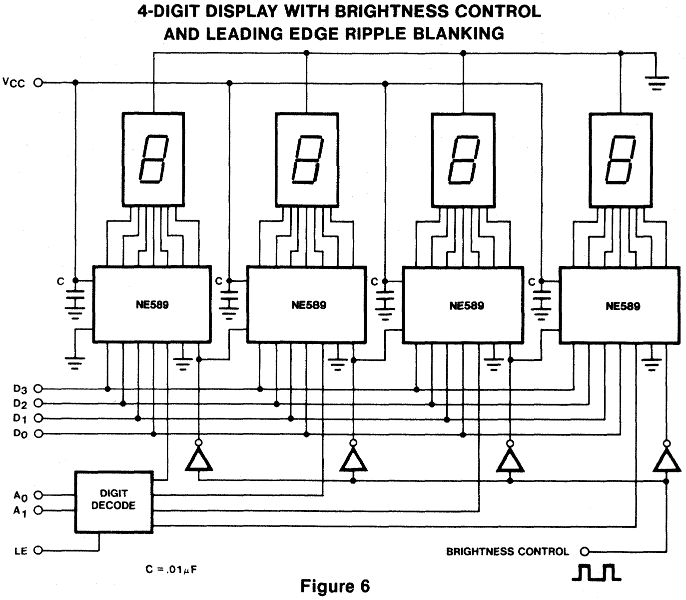


Figure 6

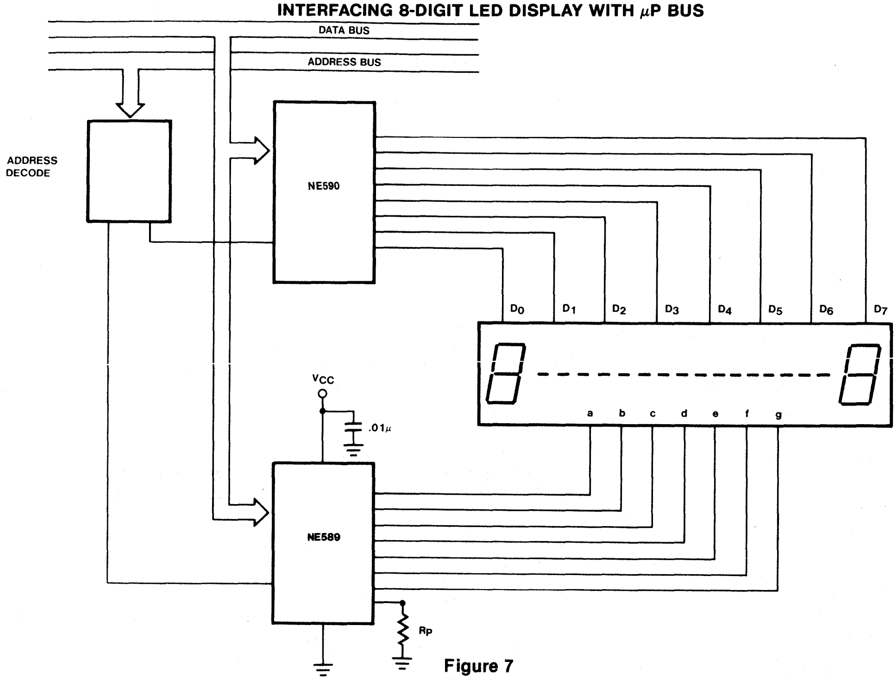


Figure 7

Preliminary

TYPICAL APPLICATIONS (Cont'd)

4-DIGIT MULTIPLEXED LED DISPLAY

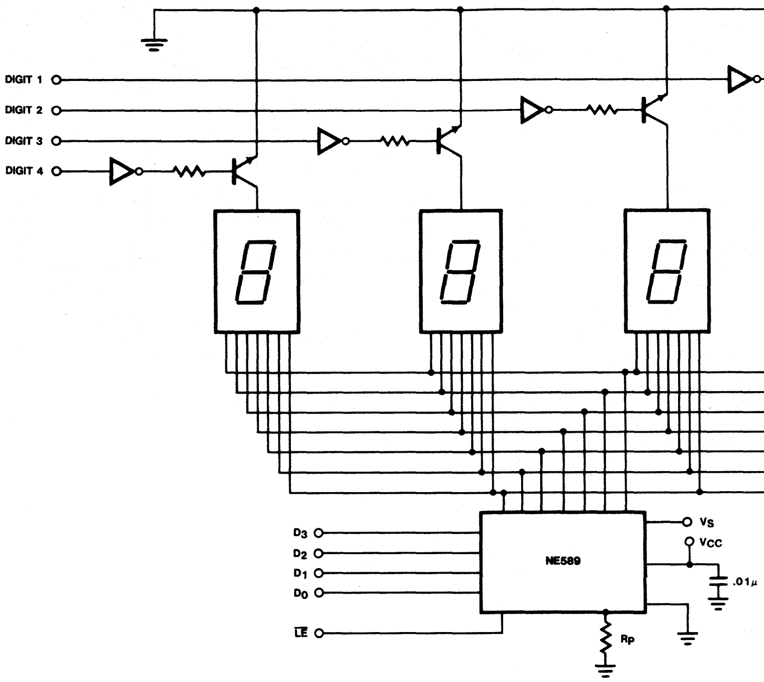


Figure 8

VACUUM FLUORESCENT DISPLAY DRIVER NE/SA594

DESCRIPTION

The NE/SA594 is a display driver interface for vacuum fluorescent displays. The device is comprised of 8 drivers and a bias network and is capable of driving the digits and/or segments of most vacuum fluorescent displays.

The inputs are designed to be compatible with TTL, DTL, NMOS, PMOS or CMOS output circuitry.

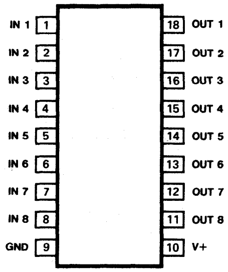
There is an active pull-down circuit on each output so that display ghosting is minimized and no external components are required for most fluorescent display applications.

FEATURES

- **Digit and/or segment drivers**
- **Active output pull-down circuitry**
- **High output breakdown voltage**
- **Low supply voltage**
- **Input compatible with all logic outputs**

PIN CONFIGURATION

N, F PACKAGE



TOP VIEW

ORDER NUMBERS
NE/SA594N NE/SA594F

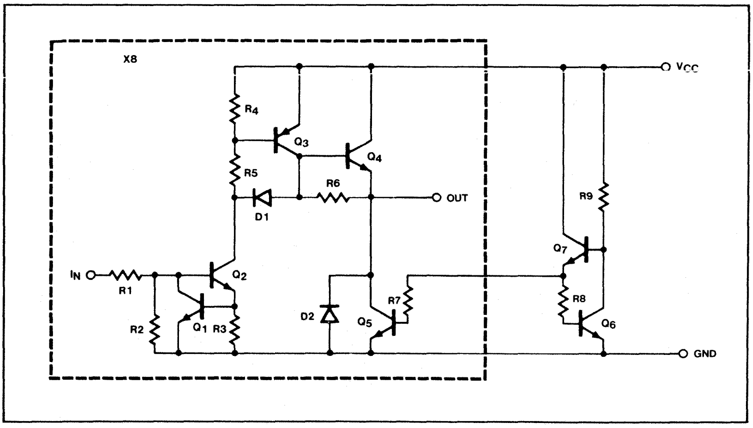
ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise noted)

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	45	V
V_{OUT}	Output voltage	V_{CC}	
V_{IN}	Input voltage	−0.3, +20	V
I_{OUT}	Output current		
	Each output	50	mA
	All outputs	200	mA
Pd	Power dissipation* (at 25°C)	800	mW
T_A	Operating temperature range		
	NE	0 to 70	°C
	SA	−40 to +85	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_J	Maximum junction temperature	150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

NOTE

*Derate N (Plastic) Package above 38°C at 7.14 mW/°C.
Derate F (Ceramic) Package above 75°C at 10.8 mW/°C.

EQUIVALENT SCHEMATIC



VACUUM FLUORESCENT DISPLAY DRIVER NE/SA594

DC ELECTRICAL CHARACTERISTICS V_{CC} = +4.75 to +40V, T_A (NE) = 0 to 70°C, T_A (SA) = −40 to +85°C unless otherwise stated.

SA594	PARAMETER	TEST CONDITIONS				UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage range		4.75	35	40	V
I_{CCH}	Supply current (all outputs high)	V_{CC} = 40V V_{IN} = 3.5V		3	6	mA
I_{CCL}	Supply current (all outputs low)	V_{CC} = 40V V_{IN} = 0.4V		0.4	1	mA
V_{IN}	Input voltage range		0		15	V
V_{IH}	Input voltage to ensure logic '1'		2.6			V
V_{IL}	Input voltage to ensure logic '0'				0.8	V
I_{IH}	Input current to ensure logic '1'		100			µA
I_{IL}	Input current to ensure logic '0'				10	µA
I_{IN}	Input current	V_{IN} = 2.6V		60	130	µA
		V_{IN} = 5.0V		180	330	µA
		V_{IN} = 15.0V		.68	1.3	mA
V_{OH}	Output high voltage	V_{IN} = 3.5V, T_A = 25°C	V_{CC}−1.5	V_{CC}−1.1		V
		I_{OUT} = −25mA, Over Temp.	V_{CC} −2	V_{CC}−1.3		V
		V_{OUT} with respect to V_{CC}				
V_{OH}	Output high, *no load* voltage	V_{IN} = 3.5V I_{OUT} = 0, T_A=25°C V_{OUT} with respect to V_{CC}	V_{CC}−1	V_{CC}−0.8		V
V_{OFF}	Output 'OFF' voltage level	V_{IN} = 0.8V I_{OUT} = 0		10	200	mV
I_{OH}	Available output current	V_{CC} = 35V V_{IN} = 3.5V V_{OUT} = 30V T_A = 25°C	−35			mA
I_{OUT}	Output pulldown current	V_{CC} = V_{OUT} = 35V Inputs open	100	200	400	µA
I_{CEX}	Output leakage current	T_A = 25°C V_{IN} = 0.4V		−1		µA
		V_{CC} = 40V, V_{OUT} = 0V		−1		

AC ELECTRICAL CHARACTERISTICS[1] V_{CC} = 35V, T_A = 25°C

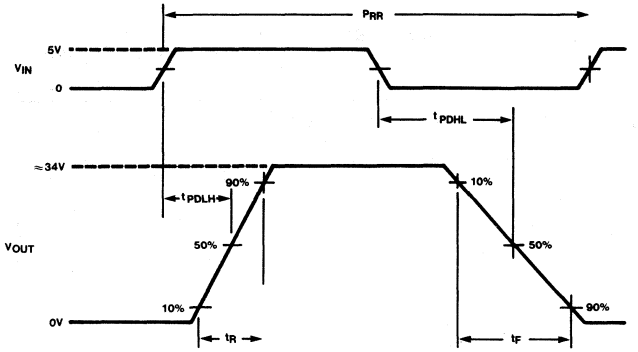
	PARAMETER	TEST CONDITIONS	NE/SA594			UNIT
			Min	Typ	Max	
t_{PdLH}	Propagation delay - low to high output transition.	50% V_{IN} to 50% V_{OUT}		1	5	µS
t_{PdHL}	Propagation delay - high to low output transition.	50% V_{IN} to 50% V_{OUT}		3	10	µS
t_R	Output rise time	10% V_{OUT} to 90% V_{OUT}		0.5	3	µS
t_F	Output fall time	90% V_{OUT} to 10% V_{OUT}		1.5	5	µS

NOTE

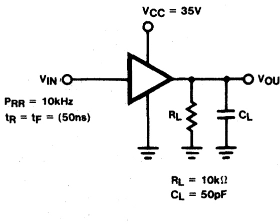
1. See figure 1

SWITCHING TIMES OF DRIVERS

VOLTAGE WAVEFORMS



TEST CIRCUIT

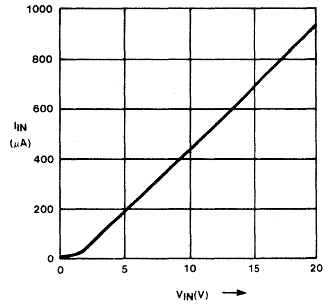


INCLUDES PROBE AND FIXTURE CAPACITANCE

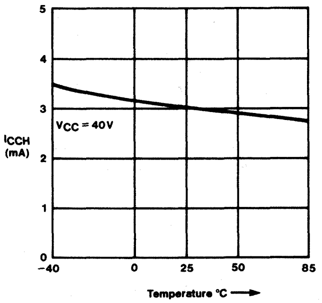
Figure 1

TYPICAL PERFORMANCE CHARACTERISTICS

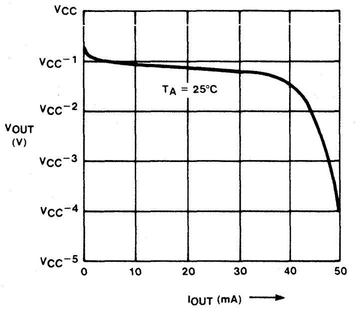
I_{IN} VS V_{IN}



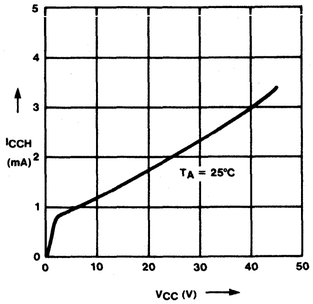
I_{CCH} VS TEMPERATURE



OUTPUT VOLTAGE VS OUTPUT CURRENT



I_{CC} VS V_{CC} (ALL INPUTS HIGH)



VACUUM FLUORESCENT DISPLAY DRIVER NE/SA594

TYPICAL APPLICATION DIGITAL CLOCK WITH ALARM

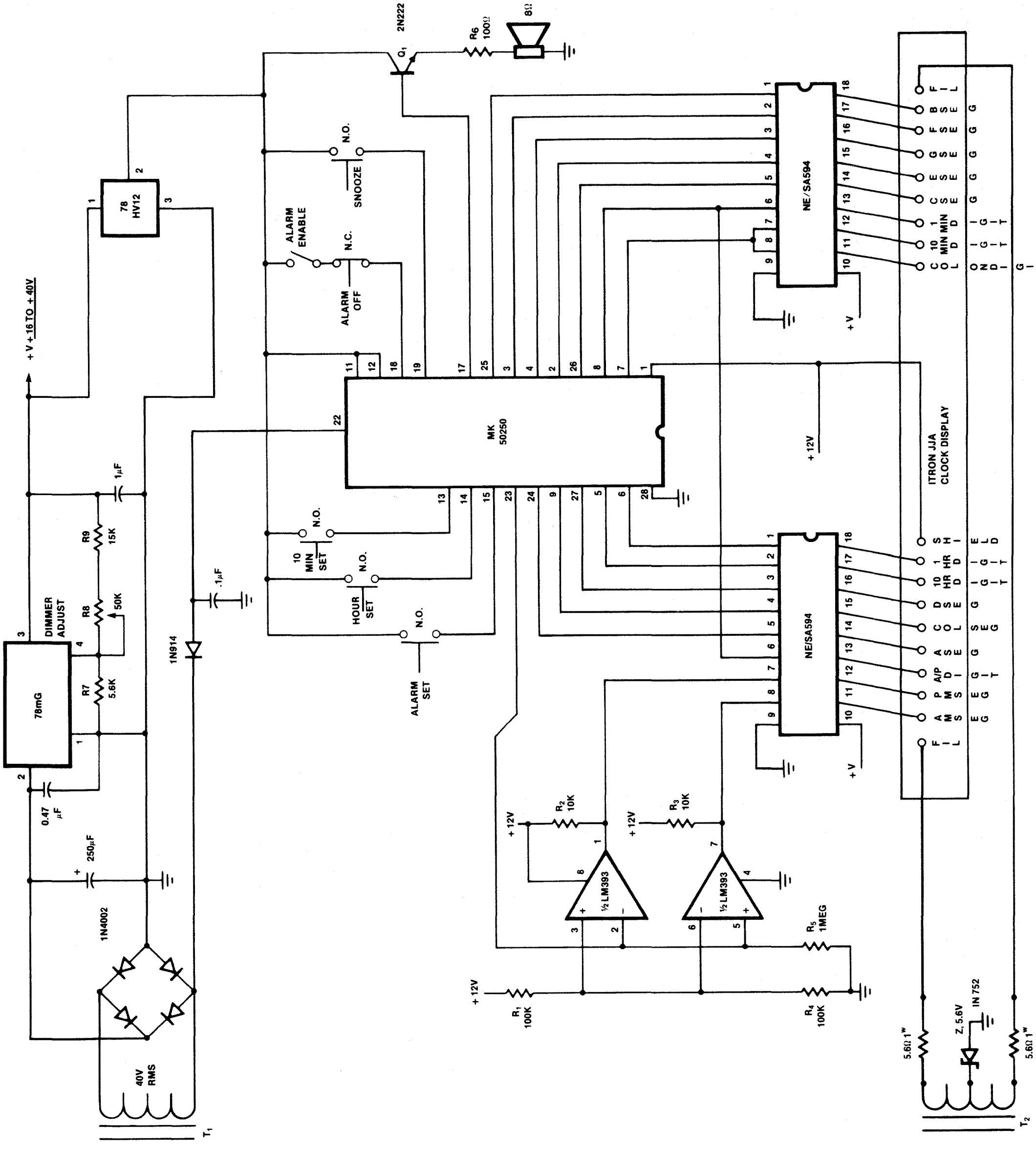


Figure 2

Section 11
A/D and D/A Converters

INDEX

Section 11 — A/D and D/A Converters

A/D AND D/A CONVERTERS—SYMBOLS AND DEFINITIONS

T_A

Ambient temperature range. Range of the surrounding environment of the operating device.

T_J

Junction Temperature. The maximum temperature of the device. 150°C is standard for silicon devices.

T_{STG}

Storage temperature range. Temperature range that the device can be stored in a non-operating condition.

T_{SOLD}

Soldering Temperature. The temperature which can be applied to the lead frame of the device for short periods of time (normally specified for a duration of 10 sec).

Truth Tables

0 is logic level low
1 is logic level high
X - don't care condition - has no effect under circuit conditions listed.

Absolute Maximum Rating

Operating safe zones exceeding these limits could cause permanent damage to the device and are not meant to imply that devices can operate at these limits.

Power Dissipation

The power that the device can safely handle at 25°C. The dissipation must be derated as indicated for the individual package type.

Package Type Designation

See full package designations in Appendix.

V_{CC} ($-V_{CC}$)

Supply Voltage. The range of power supply voltage over which the device will operate safely.

Accuracy

The maximum deviation of the DAC output relative to an ideal straight line drawn from zero to full scale.

Monotonicity

For a 1 LSB increase of input code, the output of a DAC either increases or remains the same.

Differential Linearity

The incremental error from an ideal 1 LSB analog output change when the digital input is changed 1 LSB; guaranteed monotonicity requires the differential linearity error be less than 1 LSB.

Absolute Accuracy

Error of a D/A converter output is the difference between the analog output expected and the actual output with a given code applied. Error of an A/D converter is the difference between the theoretical analog output required to produce a given output code and the actual input required to produce a given output code and the actual input required to produce that same code. The actual input is a range and the measured value is the midpoint of the measured band and the theoretical midpoint.

Resolution

The number of bits on the input or output of an A/D or D/A converter. The number of discrete steps or states is equal to 2^n when n is the resolution of the converter. However, n bits of resolution does not guarantee n bits of accuracy.

Quantizing Error

In an A/D converter, there is an infinite number of possible input voltages, but only 2^n output codes (n = number of bits). Therefore, there will be an error as great as 1/2LSB because of this quantizing effect and the greatest error will occur at the transition voltage where the output changes state.

No Missing Codes

This is a property of an A/D converter that is related to, but is more stringent than monotonicity. If a converter is guaranteed to have no missing codes, there will be no output digital state that will be skipped when the input voltage is varied over the entire range.

Most Significant Bit (MSB)

The highest-order bit or the bit with the greatest weight.

Least Significant Bit (LSB)

The lowest-order bit or the bit with the least weight.

Gain Error

The error in the input-to-output ratio, usually expressed in percent of full scale range.

Offset Error

This is an error in the reference point of the transfer function. It appears as a constant amplitude error signal at a DAC output or an ADC input. It also appears as a constant frequency shift in the output of a V/F converter. It is nulled prior to adjusting gain error by setting the input to the most-negative input and adjusting the output to the proper value.

Settling Time

The time delay in a D/A converter between a change of input digital code and the effected change in the output signal. It is usually expressed in terms of how long it takes the output to settle to, and remain within, a certain error band around the final value and is usually specified for full-scale range changes.

Conversion Time

Time required for a complete conversion cycle of an A/D converter. Conversion time is a function of the number of bits (resolution) and the clock frequency.

Full Scale Tempco

The change in DAC full scale current or voltage with change in temperature expressed in ppm/°C.

Differential Non-Linearity Tempco

The non-linearity specification over a specified range of temperatures. This specification generally appears as the range of temperatures that the device is monotonic (DAC) or has no missing codes (ADC).

Leakage Current

In a current output D/A converter, there is a digital input code that ideally yields zero output current. If current flows with that input code, it is called leakage current. It is analogous to output voltage offset in a voltage-output D/A converter.

Power Supply Sensitivity

The change in DAC output current or voltage with changes in power supply voltage.

A/D AND D/A CONVERTERS—SYMBOLS AND DEFINITIONS

Output Voltage Compliance

The range of allowable voltage levels at the output of a D/A converter that does not degrade accuracy.

Compliance Voltage Range

For a current output DAC, the maximum range of voltage for which the current source will maintain its specified values.

NOTE

Refer to Section 5 (Interface Circuits) of the 1979 Analog Applications Manual for an in-depth explanation of Converters and their applications

SE/NE 5018 DAC

COMPETITION	INDUSTRY VALUE	KEY PARAMETER	SIGNETICS AVAILABLE VALUE	SIGNETICS ORIGINATED DEVICES	QR&A		COMMENTS
					SURE II	SUPR II	
AMD* Analog Devices* Datel Fairchild* Harris* Precision Monolithics National*	8	Resolution (Bits)	8 Bits	NE5018 SE5018 NE5019 SE5019	Yes Yes Yes Yes	Yes Yes Yes Yes	*Not pin for pin replacement. Do not have total capability of the NE5018 μP compatible series.
	19	Linearity	0.1 %				
	2- 300 μ sec	Settling Time ½ LSB	2 μsec				
	10-50	Gain TC	20 PPM/°C				
	0-4	Current (Output)	mA	NE/SE 5118 NE/SE 5119	Yes Yes	Yes Yes	
	−10 to +18	Voltage (Output)	0-10 ±5 Volts	NE5018 SE5019	Yes Yes	Yes Yes	

8-BIT HIGH SPEED MULTIPLYING D/A CONVERTER

DAC-08 SERIES

FORMERLY: NE5007/5008-F,N
SE5008-F

DESCRIPTION

The DAC-08 series of 8-bit monolithic multiplying Digital-to-Analog Converters provide very high speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85ns settling times with very low glitch and at low power consumption. Monotonic multiplying performance is attained over a wide 20 to 1 reference current range. Matching to within 1 LSB between reference and full scale currents eliminates the need for full scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

Dual complementary outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. True high voltage compliance outputs allow direct output voltage conversion and eliminate output op amps in many applications.

All DAC-08 series models guarantee full 8-bit monotonicity and linearities as tight as 0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the ±4.5V to ±18V power supply range, with 33mW power consumption attainable at ±5V supplies.

The compact size and low power consumption make the DAC-08 attractive for portable and military/aerospace applications.

FEATURES

- **Fast settling output current—85ns**
- **Full scale current prematched to ±1 LSB**
- **Direct interface to TTL, CMOS, ECL, HTL, PMOS**
- **Relative accuracy to 0.1% maximum over temperature range**
- **High output compliance −10V to +18V**
- **True and complemented outputs**
- **Wide range multiplying capability**
- **Low FS current drift—±10ppm/°C**
- **Wide power supply range—±4.5V to ±18V**
- **Low power consumption—33mW at ±5V**

APPLICATIONS

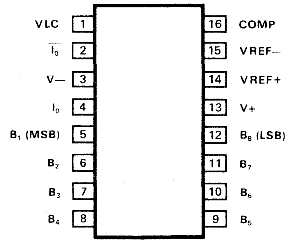
- **8-bit, 1μs A-to-D converters**
- **Servo-motor and pen drivers**
- **Waveform generators**
- **Audio encoders and attenuators**
- **Analog meter drivers**
- **Programmable power supplies**
- **CRT display drivers**
- **High speed modems**
- **Other applications where low cost, high speed and complete input/output versatility are required**

ORDERING INFORMATION

RELATIVE ACCURACY	0 to 70°C	−55 to 125°C
0.39% FS	DAC-08CN DAC-08CF DAC-08EN	
0.19% FS	DAC-08EF DAC-08ED	DAC-08F
0.1% FS	DAC-08HF DAC-08HC	DAC-08AF

PIN CONFIGURATION

F,N PACKAGE

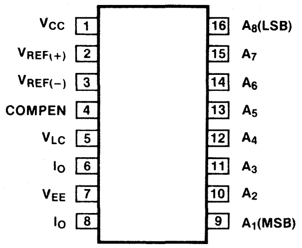


TOP VIEW

ORDER NUMBER

DAC-08AF	SE5009F
DAC-08F	SE5008F
DAC-08HF,N	NE5009F,N
DAC-08CF,N	NE5007F,N

D PACKAGE



TOP VIEW

ORDER NUMBER

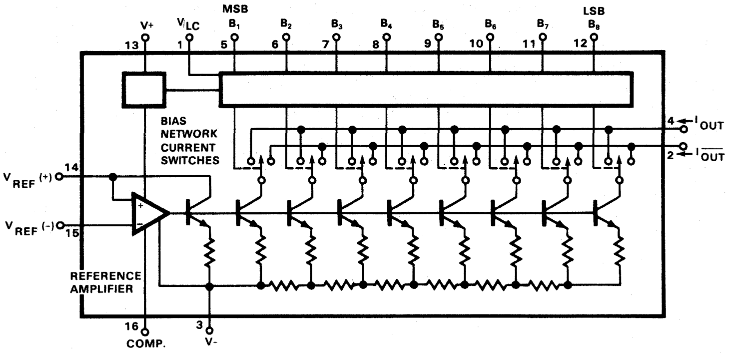
DAC-08ED

ABSOLUTE MAXIMUM RATINGS

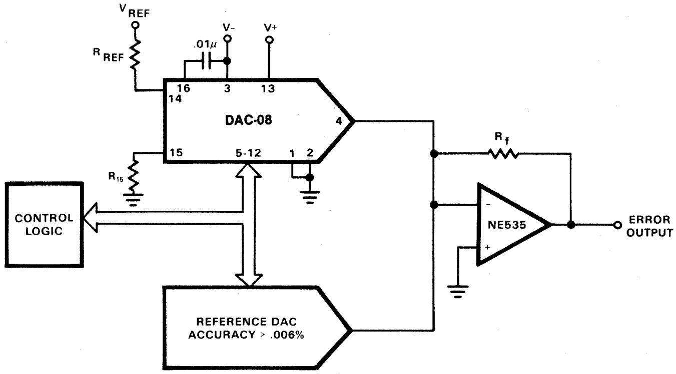
$T_A = 25°C$ unless otherwise noted

PARAMETER		RATING	UNIT
T_A	Operating temperature range		°C
	DAC-08, DAC-08A	-55 to +125	
	DAC-08C,E	0 to +70	
t_{stg}	Storage temperature	-65 to +150	°C
P_D	Power dissipation	500	mW
	Lead soldering temperature (60sec)	300	°C
	V+ to V- supply	36	V
	Logic inputs	V- to V- plus 36V	
V_{LC}	Logic threshold control	V- to V+	
	Analog current outputs	See output current or output voltage performance curve	
V_{14}, V_{15}	Reference inputs	V- to V+	
V_{14} to V_{15}	Reference input differential voltage	±18	V
I_{14}	Reference input current	5.0	mA

BLOCK DIAGRAM



TEST CIRCUIT



8-BIT HIGH SPEED MULTIPLYING D/A CONVERTER DAC-08 SERIES

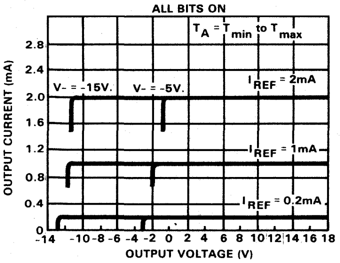
ELECTRICAL CHARACTERISTICS Pin 3 must be at least 3V more negative than the potential to which R_{15} is returned. $V_{CC} = \pm 15V$, $I_{REF} = 2.0mA$, Output characteristics refer to both IOUT and IOUT unless otherwise noted. DAC-08C, E, H: $T_A = 0°C$ to 70°C. DAC-08/08A: $T_A = -55°C$ to 125°C.

PARAMETER		TEST CONDITIONS	DAC-08C			DAC-08E DAC-08			DAC-08H DAC-08A			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	8	8	8	Bits
	Monotonicity*		8	8	8	8	8	8	8	8	8	Bits
	Relative accuracy Differential nonlinearity	Over temperature range			±0.39 ±0.39			±0.19 ±0 19			± 0.1 ±0.19	%FS %FS
t_s	Settling time	To ±1/2 LSB, all bits switched on or off, $T_A = 0°C$		70	135		70	135		70	135	ns
 t_{PLH} t_{PHL}	Propagation delay Low-to-high High-to-low	T_A=25°C, each bit. All bits switched		35	60		35	60		35	60	ns
TCI_{FS}	Full scale tempco			±10			±10			±10	± 50	ppm/°C
V_{OC}	Output voltage compliance	Full scale current change <½ LSB	-10		+18	-10		+18	-10		+18	V
I_{FS4}	Full scale current	V_{REF}=10.000V, R_{14}, R_{15}=5.000kΩ,	1.94	1.99	2.04	1.94	1.99	2.04	1.984	1.992	2.000	mA
I_{FSS}	Full scale symmetry	$I_{FS4}-I_{FS2}$		±2.0	±16		±1.0	±8.0		±1.0	± 4.0	μA
I_{ZS}	Zero scale current			0.2	4.0		0.2	2.0		0.2	1.0	μA
I_{FSR}	Full scale output current range	$R_{14} R_{15} = 5.000kΩ$ $V_{REF} = +15.0V$, $V- = -10V$ $V_{REF} = +25.0V$, $V- = -12V$	 2.1 4.2			 2.1 4.2			 2.1 4.2			mA
 V_{IL} V_{IH}	Logic input levels Low High	V_{LC}=0V	 2.0		 0.8	 2.0		 0.8	 2.0		 0.8	V
 I_{IL} I_{IH}	Logic input current Low High	V_{LC}=0V V_{IN}=-10V to +0.8V V_{IN}=2.0V to 18V		 -2.0 0.002	 -10 10		 -2.0 0.002	 -10 10		 -2.0 0.002	 -10 10	μA
V_{IS}	Logic input swing	V-=-15V	-10		+18	-10		+18	-10		+18	V
V_{THR}	Logic threshold range	V_S=±15V	-10		+13.5	-10		+13.5	-10		+13.5	V
I_{15}	Reference bias current			-1.0	-3.0		-1.0	-3.0		-1.0	-3.0	μA
dl/dt	Reference input slew rate		4.0	8.0		4.0	8.0		4.0	8.0		mA/μs
 $PSSI_{FS+}$ $PSSI_{FS-}$	Power supply sensitivity Positive Negative	I_{REF}=1mA V+=4.5 to 5.5V, V-=-15V; V+=13.5 to 16.5V, V-=-15V V-=-4.5 to -5.5V, V+=+15V; V-=-13.5 to -16.5, V+=+15V		 0.0003 0.002	 0.01 0.01		 0.0003 0.002	 0.01 0.01		 0.0003 0.002	 0.01 0.01	%FS/%VS
 I+ I-	Power supply current Positive Negative	V_S=±5V, IREF=1.0mA		 2.3 -4.3	 3.8 -5.8		 2.3 -4.3	 3.8 -5.8		 2.3 -4.3	 3.8 -5.8	mA
I+ I-	Positive Negative	V_S=+5V, -15V, I_{REF}=2.0mA		2.4 -6.4	3.8 -7.8		2.4 -6.4	3.8 -7.8		2.4 -6.4	3.8 -7.8	
I+ I-	Positive Negative	V_S=±15V, I_{REF}=2.0mA		2.5 -6.5	3.8 -7.8		2.5 -6.5	3.8 -7.8		2.5 -6.5	3.8 -7.8	
P_D	Power dissipation	±5V, I_{REF}=1.0mA +5V, -15V, I_{REF}=2.0mA ±15V, I_{REF}=2.0mA		33 108 135	48 136 174		33 108 135	48 136 174		33 108 135	48 136 174	mW

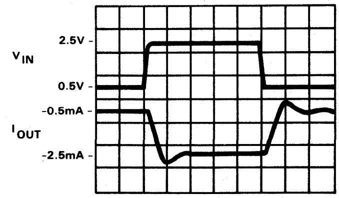
NOTE *NE5007 must have a minimum reference current of .8μA.

TYPICAL PERFORMANCE CHARACTERISTICS

OUTPUT CURRENT vs OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE)

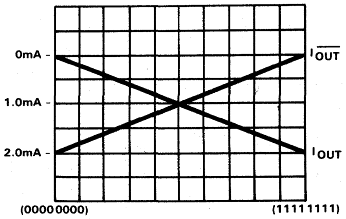


FAST PULSED REFERENCE OPERATION

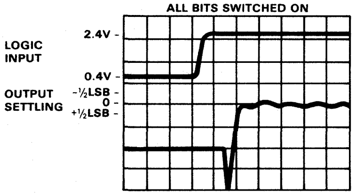


200ns/division
R_{EQ} = 200Ω, R_L = 100Ω, CC = O

TRUE AND COMPLEMENTARY OUTPUT OPERATION



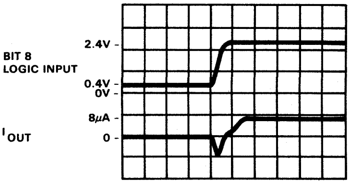
FULL SCALE SETTLING TIME



50ns/division

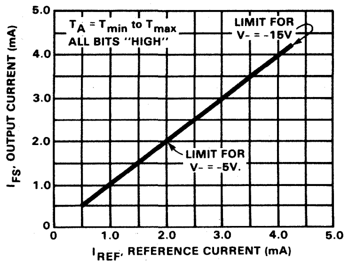
IFS = 2mA, R_L = 1kΩ ½ LSB = 4μA

LSB SWITCHING

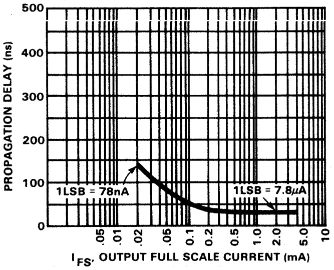


50ns/division

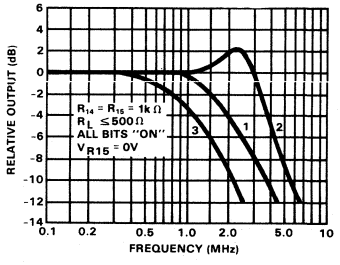
FULL SCALE CURRENT vs REFERENCE CURRENT



LSB PROPAGATION DELAY vs IFS



REFERENCE INPUT FREQUENCY RESPONSE

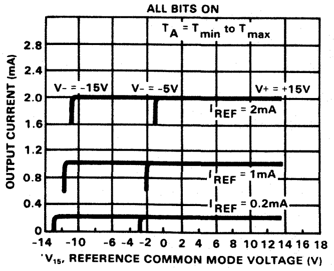


Curve 1: CC = 15pF, V_{IN} = 2.0V p-p centered at +1.0V.
Curve 2: CC = 15pF, V_{IN} = 50mV p-p centered at +200mV.
Curve 3: CC = 0pF, V_{IN} = 100mV p-p centered at 0V and applied thru 50Ω connected to pin 14. +2.0V applied to R_{14}.

8-BIT HIGH SPEED MULTIPLYING D/A CONVERTER DAC-08 SERIES

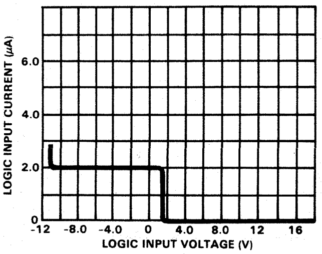
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

REFERENCE AMP COMMON MODE RANGE

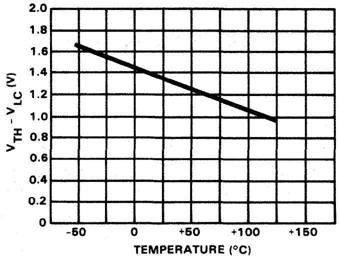


Positive common mode range is always (V+) - 1.5V

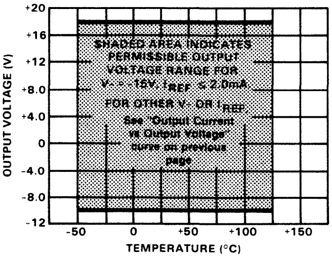
LOGIC INPUT CURRENT vs INPUT VOLTAGE



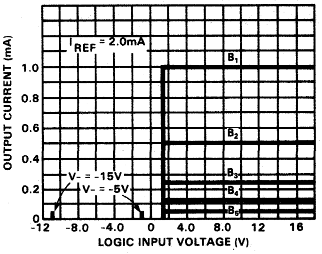
V_{TH} - V_{LC} vs TEMPERATURE



OUTPUT VOLTAGE COMPLIANCE vs TEMPERATURE



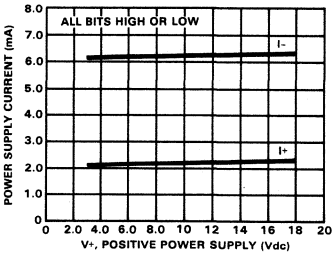
BIT TRANSFER CHARACTERISTICS



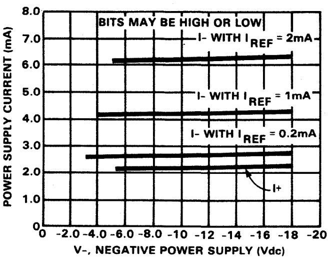
NOTE

B_1 through B_8 have identical transfer characteristics. Bits are fully switched, with less than ½ LSB error, at less than ±100mV from actual threshold. These switching points are guaranteed to lie between 0.8 and 2.0 volts over the operating temperature range (VLC = 0.0V).

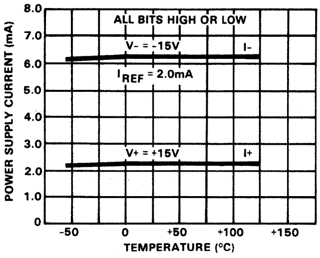
POWER SUPPLY CURRENT vs V+



POWER SUPPLY CURRENT vs V-

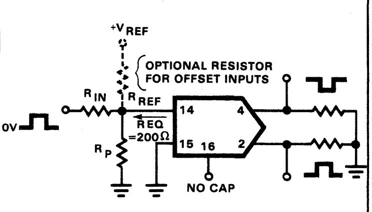


POWER SUPPLY CURRENT vs TEMPERATURE



TYPICAL APPLICATION

PULSED REFERENCE OPERATION



TYPICAL VALUES

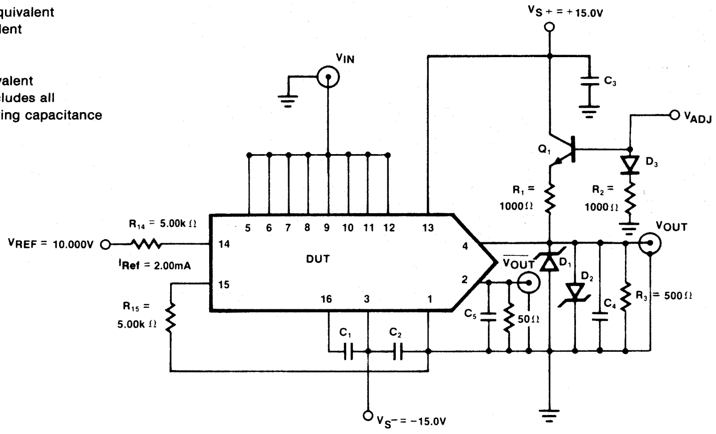
R_{IN} = 5K

$+V_{IN}$ = 10V

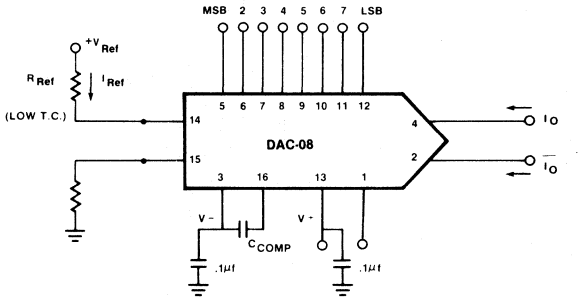
8-BIT HIGH SPEED MULTIPLYING D/A CONVERTER DAC-08 SERIES

SETTLING TIME AND PROPAGATION DELAY

D_1, D_2 = IN6263 or equivalent
D_3 = IN914 or equivalent
C_1 = 0.01µf
C_2, C_3 = 0.1µf
Q_1 = 2N3904 or equivalent
C_4, C_5 = 15pf and includes all
probe and fixturing capacitance

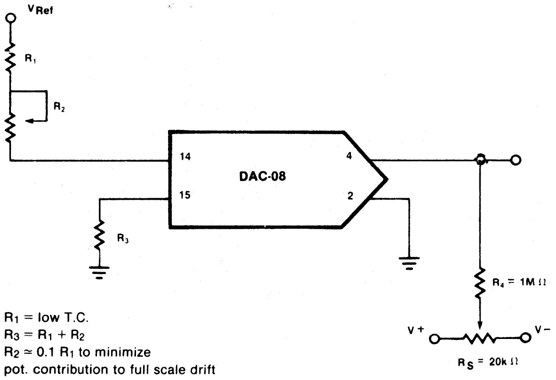


BASIC 5008/5009 CONFIGURATION



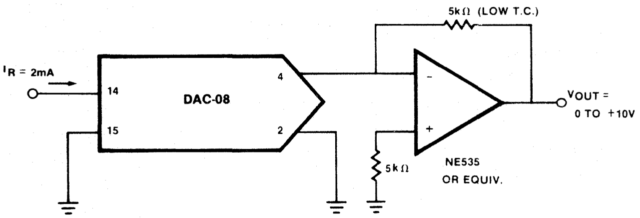
$I_{FS} \approx \frac{+V_{Ref}}{R_{Ref}} \times \frac{255}{256}$; $I_O + \overline{I_O} = I_{FS}$ for all logic states

RECOMMENDED FULL SCALE AND ZERO SCALE ADJ.



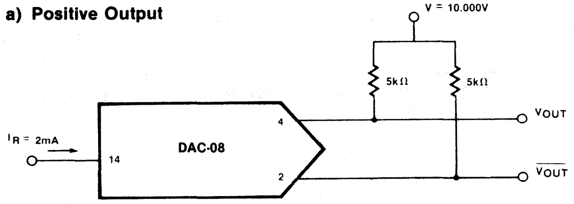
R_1 = low T.C.
$R_3 = R_1 + R_2$
$R_2 \simeq 0.1\ R_1$ to minimize
pot. contribution to full scale drift

UNIPOLAR VOLTAGE OUTPUT FOR LOW IMPEDANCE OUTPUT

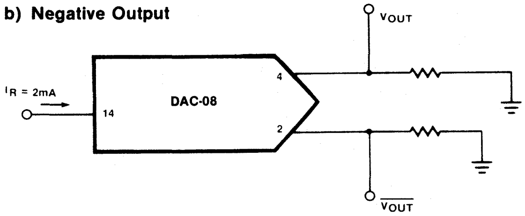


UNIPOLAR VOLT OUTPUT FOR HIGH IMPEDANCE OUTPUT

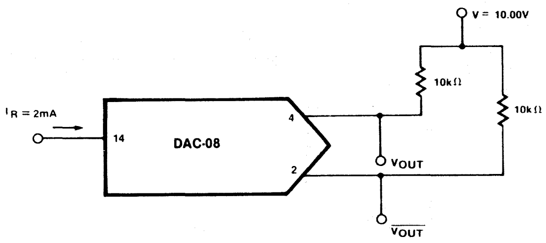
a) Positive Output



b) Negative Output



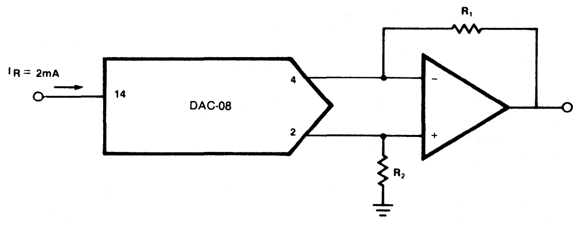
BASIC BIPOLAR OUTPUT OPERATION (OFFSET BINARY)



CODE CHART

	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	V_{OUT}	$\overline{V_{OUT}}$
POS full scale	1	1	1	1	1	1	1	1	- 9.920V	+10.000
POS f.s. - 1LSB	1	1	1	1	1	1	1	0	- 9.840V	+9.920
+ Zero scale + 1LSB	1	0	0	0	0	0	0	1	- 0.080V	+0.160
Zero scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero scale - 1LSB	0	1	1	1	1	1	1	1	0.080	0.000
Neg full scale - 1LSB	0	0	0	0	0	0	0	1	+ 9.920	-9.840
Neg full scale	0	0	0	0	0	0	0	0	+10.000	-9.920

SYMMETRICAL OFFSET BINARY (BIPOLAR)



VOUT = 0 to ±V*

±V *Range:
±5V for R1 = R2 = 2.5K
±10V for R1 = R2 = 5.0K

3 DIGIT BCD CONVERTER

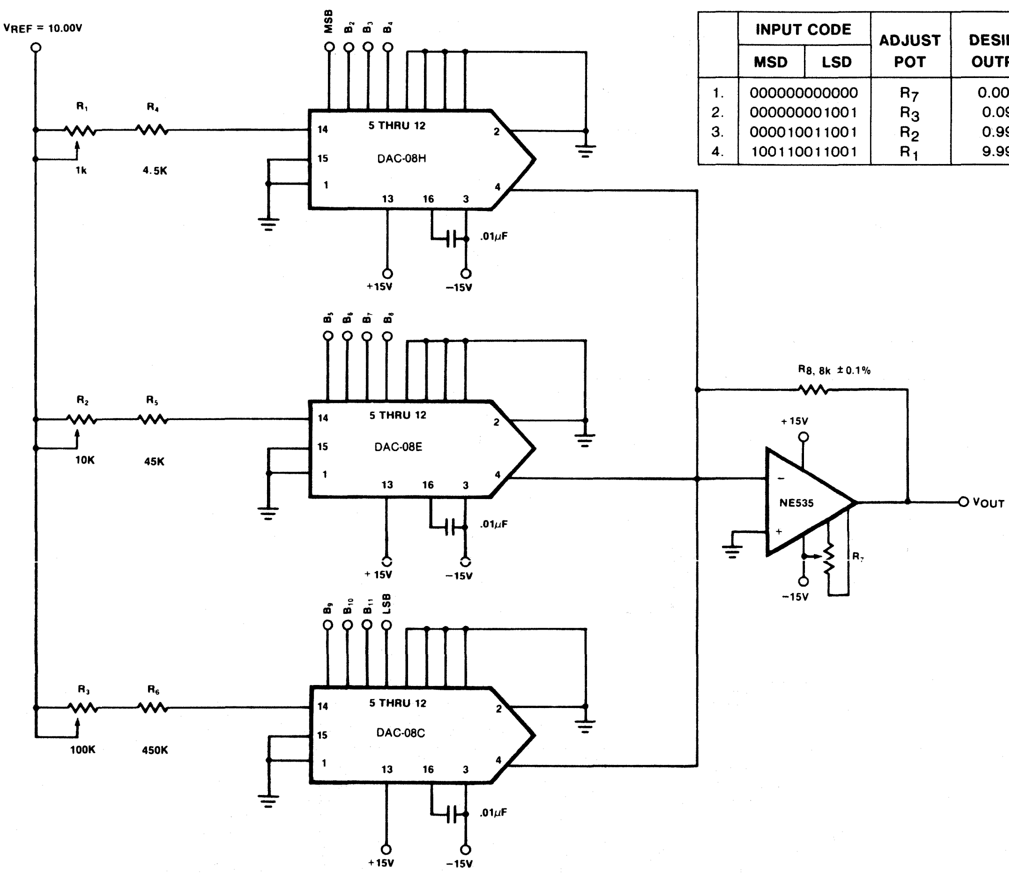
A 3 digit BCD converter, using inexpensive 8-bit binary DACs, can achieve ±0.1% accuracy. The circuit shown in Figure 20 utilizes three DACs, one for each decade, to provide 0 to 999 output steps. DAC 1 contains the first four significant digits controlling the hundreds digit; DAC 2 controls the tens digit and DAC 3 steps 0 to 9. The feedback resistor (R_7) sets the zero scale at 0.00V.

The input coding is the popular 8-4-2-1 coding; i.e. the weighting ratios are 8, 4, 2 and 1. The full scale (999) BCD code is input code 100110011001.

Full scale adjustment procedure.

In the sequence below, switch on the following code combinations and adjust the indicated potentiometer for the proper output.

3 DIGIT BCD CONVERTER WITH ±0.1% ACCURACY



	INPUT CODE		ADJUST POT	DESIRED OUTPUT
	MSD	LSD		
1.	000000000000		R_7	0.000V
2.	000000001001		R_3	0.09V
3.	000010011001		R_2	0.99V
4.	100110011001		R_1	9.99V

8-BIT MULTIPLYING D/A CONVERTER MC1508-8/1408-8/1408-7

DESCRIPTION

The MC1508/MC1408 series of 8-bit monolithic digital-to-analog converters provide high speed performance with low cost. They are designed for use where the output current is a linear product of an 8-bit digital word and an analog reference voltage.

FEATURES

- **Fast settling time—70ns (typ)**
- **Relative accuracy ±0.19% (max error)**
- **Non-inverting digital inputs are TTL and CMOS compatible**
- **High speed multiplying rate 4.0mA/µs (input slew)**
- **Output voltage swing +.5V to -5.0V**
- **Standard supply voltages + 5.0V and -5.0V to -15V**
- **Military qualifications pending**

APPLICATIONS

- **Tracking A-to-D converters**
- **2½-digit panel meters and DVM's**
- **Waveform synthesis**
- **Sample and hold**
- **Peak detector**
- **Programmable gain and attenuation**
- **CRT character generation**
- **Audio digitizing and decoding**
- **Programmable power supplies**
- **Analog-digital multiplication**
- **Digital-digital multiplication**
- **Analog-digital division**
- **Digital addition and subtraction**
- **Speech compression and expansion**
- **Stepping motor drive**

CIRCUIT DESCRIPTION

The MC1508/MC1408 consists of a reference current amplifier, and R-2R ladder, and 8 high speed current switches. For many applications, only a reference resistor and reference voltage need be added.

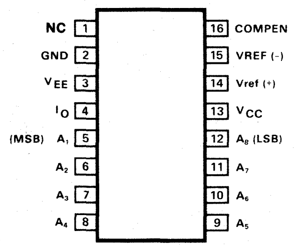
The switches are non-inverting in operation; therefore, a high state on the input turns on the specified output current component.

The switch uses current steering for high speed, and a termination amplifier consisting of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching, and provides a low impedance termination of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binarily-related components, which are fed to the switches. Note that there is always a remainder current which is equal to the least significant bit. This current is shunted to ground, and the maximum output current is 255/256 of the reference amplifier current, or 1.992mA for a 2.0mA reference amplifier current if the NPN current source pair is perfectly matched.

PIN CONFIGURATION

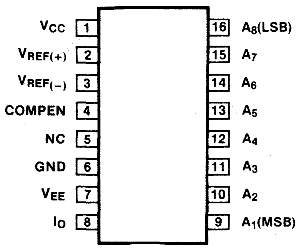
F,N PACKAGE



TOP VIEW

ORDER NUMBERS
MC1508-8F MC1408-7N
MC1408-7F

D PACKAGE



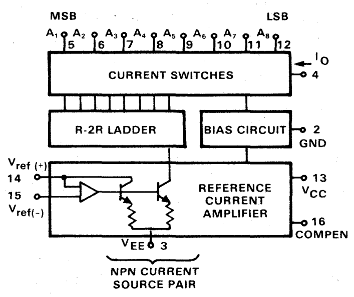
TOP VIEW

ORDER NUMBER
MC 1408-8D

ABSOLUTE MAXIMUM RATNGS T_A = +25°C unless otherwise specified

	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage		V
V_{EE}	Positive	+5.5	
V_5-V_{12}	Negative	-16.5	
V_O	Digital input voltage	+5.5, 0	V
I_{14}	Applied output voltage	+0.5, -5.2	V
V_{14},V_{15}	Reference current	5.0	mA
	Reference amplifier inputs	V_{CC}, V_{EE}	V
P_D	Power dissipation (package limitation)		mW
	Ceramic package	1000	
	Plastic package	800	
T_A	Operating temperature range		°C
	MC1508	-55 to +125	
	MC1408	0 to +75	
T_{stg}	Storage temperature range	-65 to +70	°C

BLOCK DIAGRAM



8-BIT MULTIPLYING D/A CONVERTER

MC1508-8/1408-8/1408-7

DC ELECTRICAL CHARACTERISTICS[1]

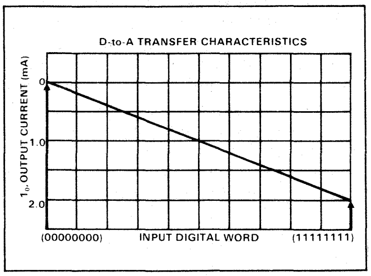
Pin 3 must be 3V more negative than the potential to which R_{15} is returned.
$V_{CC} = +5.0Vdc$, $V_{EE} = -15Vdc$, $\frac{V_{ref}}{R_{14}} = 2.0mA$
unless otherwise specified.
MC1508: $T_A = -55°C$ to $125°C$. MC1408: $T_A = 0°C$ to $75°C$

PARAMETER	TEST CONDITIONS	MC1508-8			MC1408-8			MC1408-7			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
E_r Relative accuracy	Error relative to full scale I_O, Figure 3			±0.19			±0.19			±0.39	%
t_s Setting time[1]	To within 1/2 LSB, includes t'PLH, T'A = +25°C, Figure 4		70			70			70		ns
Propagation delay time											ns
t_{PLH} Low-to-high t_{PHL} High-to-low	T_A = +25°C, Figure 4		30	100		30	100		30	100	
TCI_O Output full scale current drift			-20			-20			-20		PPM/°C
Digital input logic level (MSB)											Vdc
V_{IH} High	Figure 5	2.0			2.0			2.0			
V_{IL} Low				0.8			0.8			0.8	
Digital input current (MSB)	Figure 5										mA
I_{IH} High	V_{IH} = 5.0V		0	0.04		0	0.04		0	0.04	
I_{IL} Low	V_{IL} = 0.8V		-0.4	-0.8		-0.4	-0.8		-0.4	-0.8	
I_{15} Reference input bias current	Pin 15, Figure 5		-1.0	– 5.0		-1.0	– 5.0		-1.0	– 5.0	μA
I_{OR} Output current range	Figure 5										mA
	V_{EE} = –5.0V	0	2.0	2.1	0	2.0	2.1	0	2.0	2.1	
	V_{EE} = –7.0V to –15V	0	2.0	4.2	0	2.0	4.2	0	2.0	4.2	
I_O Output current	Figure 5 V_{ref} = 2.000V, R14 = 1000Ω	1.9	1.99	2.1	1.9	1.99	2.1	1.9	1.99	2.1	mA
$I_{O(min)}$ Off-state	All bits low		0	4.0		0	4.0		0	4.0	μA
V_O Output voltage compliance	E_r≤0.19% at T_A = +25°C, Figure 5										Vdc
	V_{EE} = -5V			-0.55, +0.5			-0.55, +0.5			-0.55, +0.5	
	V_{EE} below -10V			-5.0, +0.5			-5.0, +0.5			-5.0, +0.5	
SRI_{ref} Reference current slew rate	Figure 6		4.0			4.0			4.0		mA/μs
$PSRR_{(-)}$ Output current power supply sensitivity	I_{ref} = 1mA		0.5	2.7		0.5	2.7		0.5	2.7	μA/V
Power supply current											mA
I_{CC} Positive	All bits low,		+13.5	+22		+13.5	+22		+13.5	+22	
I_{EE} Negative	Figure 5		-7.5	-13		-7.5	-13		-7.5	-13	
Power supply voltage range											Vdc
V_{CCR} Positive	T_A = +25°C,	+4.5	+5.0	+5.5	+4.5	+5.0	+5.5	+4.5	+5.0	+5.5	
V_{EER} Negative	Figure 5	-4.5	-15	-16.5	-4.5	-15	-16.5	-4.5	-15	-16.5	
P_D Power dissipation	All bits low, Figure 5										mW
	V_{EE} = –5.0Vdc		105	170		105	170		105	170	
	V_{EE} = –15Vdc		190	305		190	305		190	305	
	All bits high, Figure 5										
	V_{EE} = –5.0Vdc		90			90			90		
	V_{EE} = –15Vdc		160			160			160		

NOTES

1. All bits switched

TYPICAL PERFORMANCE CHARACTERISTICS



FUNCTIONAL DESCRIPTION

Reference Amplifier Drive and Compensation

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current (I_{14}) must always flow into pin 14 regardless of the setup method or reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 1. The reference voltage source supplies the full current I_{14}. For bipolar reference signals, as in the multiplying mode, R_{15} can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R_{15} with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R_{14} to maintain proper phase margin; for R_{14} values of 1.0, 2.5 and 5.0kΩ, minimum capacitor values are 15, 37, and 75pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection.

A negative reference voltage may be used if R_{14} is grounded and the reference voltage is applied to R_{15} as shown in Figure 2. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 3.0V above the V_{EE} supply. Bipolar input signals may be handled by connecting R_{14} to a positive reference voltage equal to the peak positive input level at pin 15.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5.0V logic supply is not recommended as a reference voltage. If a well regulated 5.0V supply which drives logic is to be used as the reference, R_{14} should be decoupled by connecting it to +5.0V through another resistor and bypassing the junction of the 2 resistors with 0.1μF to ground. For reference voltages greater than 5.0V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high inpedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

Output Voltage Range

The voltage on pin 4 is restricted to a range of −0.55 to +0.5V at +25°C, due to the current switching methods employed in the MC1508/MC1408. When a current switch is turned off, the positive voltage on the output terminal can turn on the output diode and increase the output current level. When a current switch is turned on, the negative output voltage range is restricted. The base of the termination circuit Darlington transistor is 1 diode voltage below ground when pin 1 is grounded, so a negative voltage below ground when pin 1 is grounded, so a negative voltage below the specified safe level will drive the low current device of the Darlington into saturation, decreasing the output current level.

The negative output voltage compliance of the MC1508/MC1408 may be extended to -5.0V by opening the circuit at pin 1. The negative supply voltage must be more negative than -10V. Using a full scale current of 1.992mA and load resistor of 2.5kΩ between pin 4 and ground will yield a voltage output of 256 levels between 0 and -4.980V. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500Ω do not significantly affect performance, but 2.5kΩ load increases worst case settling time to 1.2μs (when all bits are switched on). Refer to the subsequent text section on settling time for more details on output loading.

If a power supply value between -5.0V and -10V is desired, a voltage of between 0 and -5.0V may be applied to pin 1. The value of this voltage will be the maximum allowable negative output swing.

Output Current Range

The output current maximum rating of 4.2mA may be used only for negative supply voltages more negative than -7.0V, due to the increased voltage drop across the resistors in the reference current amplifier.

Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full scale current. The relative accuracy of the MC1508/MC1408 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the MC1508/MC1408 has a very low full scale current drift with temperature.

The MC1508/±MC1408 series is guaranteed accurate to within ±1/2 LSB at +25°C at a full scale output current of 1.992mA. This corresponds to a reference amplifier output current drive to the ladder network of 2.0mA, with the loss of 1 LSB = 8.0μA which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown in Figure 3. The 12-bit converter is calibrated for a full scale output current of 1.992mA. This is an optional step since the MC1508/MC1408 accuracy is essentially the same between 1.5 and 2.5mA. Then the MC1508/MC1408 circuits' full scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accurate D-to-A converter. Sixteen-bit accuracy implies a total error ±1/2 of 1 part in 65,536, or ±0.00076%, which is much more accurate than the ±0.19% specification provided by the MC1508/MC1408.

Multiplying Accuracy

The MC1508/MC1408 may be used in the multiplying mode with 8-bit accuracy when the reference current is varied over a range of 256:1. The major source of error is the bias current of the termination amplifier. Under worst case conditions, these 8 amplifiers can contribute a total of 1.6μA extra current at the output terminal. If the reference current in the multiplying mode ranges from 16μA to 4.0mA, the 1.6μA contributes an error of 0.1 LSB. This is well within 8-bit accuracy.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the MC1508/MC1408 is monotonic for all values of reference current above 0.5mA. The recommended range for operation with a dc reference current is 0.5 to 4.0mA.

Settling Time

The worst case switching condition occurs when all bits are switched on, which corresponds to a low-to-high transition for all bits. This time is typically 70ns for settling to within ±1/2 LSB for 8-bit accuracy and 200ns to 1/2 LSB for 7-bit accuracy. The turnoff is typically under 100ns. These times apply when $R_L \leq 500\Omega$ and $C_O \leq 25pF$.

The slowest single switch is the least significant bit, which turns on and settles in 65ns and truns off in 80ns. In applications where the D-to-A converter functions in a positive going ramp mode, the worst case switching condition does not occur, and a settling time of less than 70ns may be realized. Bit A7 turns on in 50ns and off in 35ns, while bit A6 turns on in 60ns and off in 80ns.

The test circuit of Figure 4 requires a smaller voltage swing for the current switches due to internal voltage clamping in MC1508/MC1408. A 1.0kΩ load resistor from pin 4 to ground gives a typical settling time of 400ns. Thus, it is voltage swing and not the output R_C time constant that determines settling time for most applications. Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100μF supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

TEST CIRCUITS

POSITIVE Vref

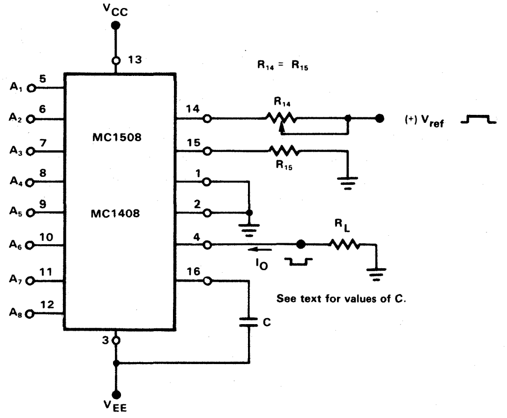


Figure 1

NEGATIVE Vref

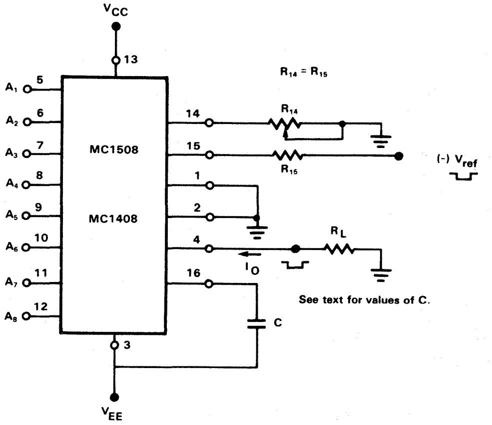


Figure 2

TEST CIRCUITS (Cont'd)

RELATIVE ACCURACY

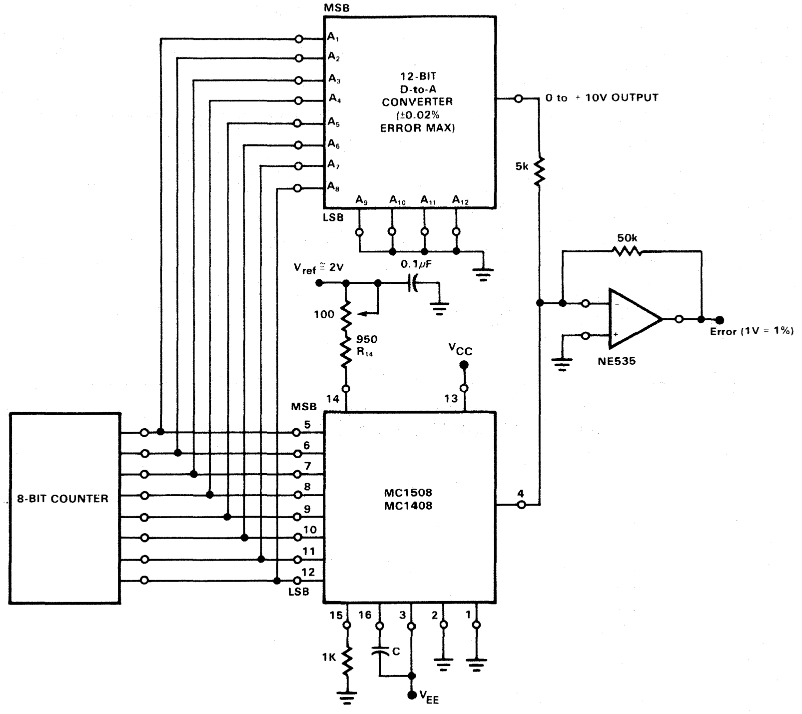


Figure 3

TRANSIENT RESPONSE AND SETTLING TIME

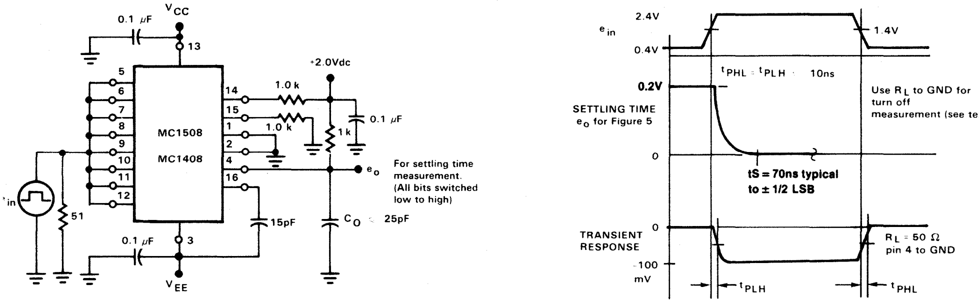
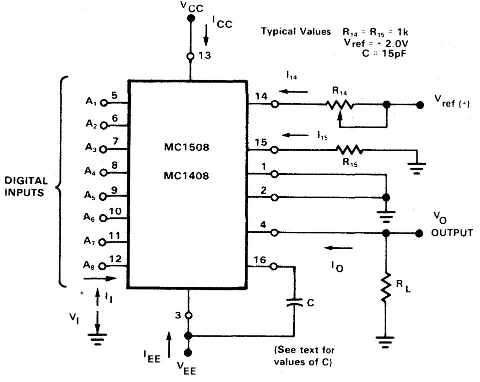


Figure 4

TEST CIRCUITS (Cont'd)

NOTATION DEFINITIONS



Typical Values $R_{14} = R_{15} = 1k$
$V_{ref} = +2.0V$
$C = 15pF$

(See text for values of C)

V_I and I_I apply to inputs A_1 thru A_8

The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

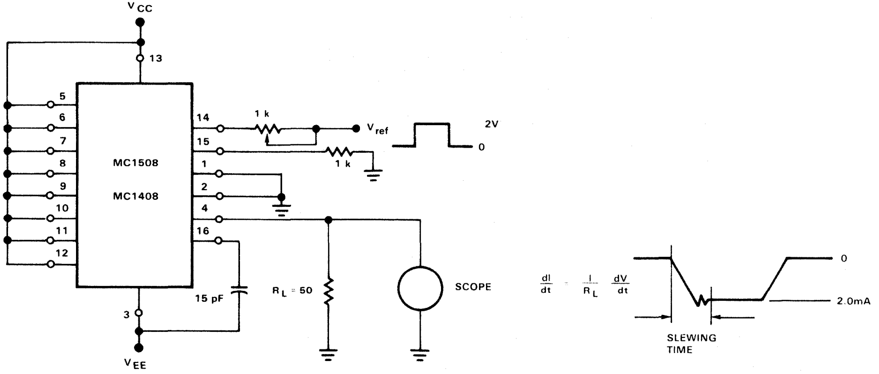
$$I_O = K\left\{\frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} + \frac{A_6}{64} + \frac{A_7}{128} + \frac{A_8}{256}\right\}$$

where $K \cong \frac{V_{ref}}{R_{14}}$

and $A_N = $ "1" if A_N is at high level
$A_N = $ "0" if A_N is at low level

Figure 5

REFERENCE CURRENT SLEW RATE MEASUREMENT



$$\frac{dI}{dt} = \frac{I}{R_L}\frac{dV}{dt}$$

Figure 6

8-BIT μP-COMPATIBLE D/A CONVERTER SE/NE5018

DESCRIPTION

The NE5018 is a complete 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most micro-processors.

The chip also comprises a stable voltage reference (5V nominal) and a high slew rate buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

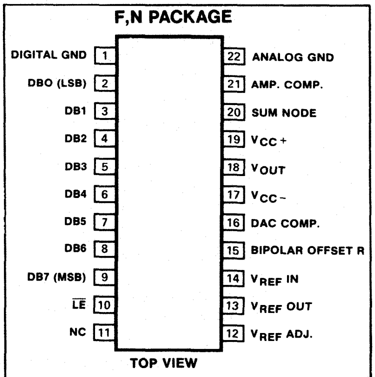
FEATURES

- **8-bit resolution**
- **Input latches**
- **Low-loading data inputs**
- **On-chip voltage reference**
- **Output buffer amplifier**
- **Accurate to ± 1/2 LSB (.19%)**
- **Monotonic to 8 bits**
- **Amplifier and reference both short-circuit protected**
- **Compatible with 8085, 6800 and many other μP's**

APPLICATIONS

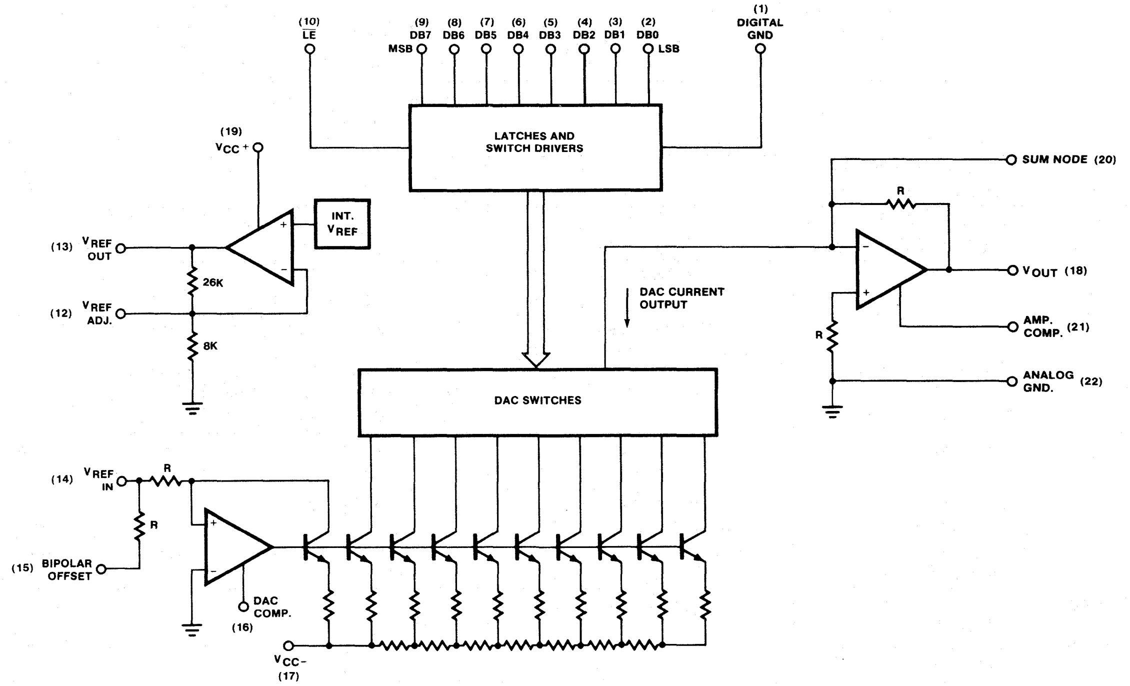
- **Precision 8-bit D/A converters**
- **A/D converters**
- **Programmable power supplies**
- **Test equipment**
- **Measuring instruments**
- **Analog-digital multiplication**

PIN CONFIGURATION



ORDER NUMBERS
NE/SE5018F,N

BLOCK DIAGRAM



All R values equal 5KΩ and are thermally matched.

Figure 1

8-BIT μP-COMPATIBLE D/A CONVERTER SE/NE5018

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	−18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF}IN$	Voltage at V_{REF} input	12	V
$V_{REF}ADJ$	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at V_{REF} OUT	Continuous	
I_{OUTSC}	Short-circuit current to ground or either supply at V_{OUT}	Continuous	
P_D	Power dissipation*		
	-N package	800	mW
	-F package	1000	mW
T_A	Operating temperature range		
	SE5018	−55 to +125	°C
	NE5018	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES
For N package, derate at 120°C/W above 35°C
For F package, derate at 75°C/W above 75°C

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5018. $-55°C \leq T_A \leq 125°C$, NE5018. $0°C \leq T_A \leq 70°C$ unless otherwise specified[1] Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	SE5018			NE5018			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Relative accuracy				±0.19			±0.19	%FS
$V_{CC}+$	Positive supply voltage		11.4	15		11.4	15		V
$V_{CC}-$	Negative supply voltage		−11.4	−15		−11.4	−15		V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1 = 0V	2.0			2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1 = 0V			0.8			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1 = 0V, $2V < V_{IN} < 18V$		0.1	10		0.1	10	μA
$I_{IN(0)}$	Logic "0" input current	Pin 1 = 0V, $-5V < V_{IN} < 0.8V$		−2.0	−10		−2.0	−10	μA
V_{FS}	Full scale output voltage	Unipolar operation $V_{REF\ IN} = 5.000V$, $T_A = 25°C$	9.50	9.961	10.50	9.50	9.961	10.50	V
V_{FS}	Full scale output voltage	Bipolar operation	4.5	+4.961	5.5	4.5	+4.961	5.5	V
		$V_{REF\ IN} = 5.000V$, $T_A = 25°C$	-5.04	−5.000	-4.960	5.04	−5.000	4.960	
V_{ZS}	Zero scale voltage		-30	5	+30	-30	5	+30	mV
I_{OS}	Output short circuit current	$T_A = 25°C$ $V_{OUT} = 0V$		15	40		15	40	mA
PSR+(out)	Output power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01		.001	.01	%FS/ %VS
PSR−(out)	Output power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq -16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01		.001	.01	%FS/ %VS
TC_{FS}	Full scale temperature coefficient	$V_{REF\ IN} = 5.000V$		20			20		ppm/°C
TC_{ZS}	Zero scale temperature coefficient			5			5		ppm/°C

DC ELECTRICAL CHARACTERISTICS (Cont'd) $V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5018. $-55°C \leq T_A \leq 125°C$, NE5018. $0°C \leq T_A \leq 70°C$ unless otherwise specified.[1] Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	SE/5018			NE5018			UNIT
			Min	Typ	Max	Min	Typ	Max	
I_{REF}	Reference output current	Note 8			3			3	mA
I_{REFSC}	Reference short circuit current	$T_A = 25°C$ $V_{REF\ OUT} = 0V$		15	30		15	30	mA
$PSR+_{(REF)}$	Reference power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, $I_{REF} = 1.0mA$		.003	.01		.003	.01	%VR/%VS
$PSR-_{(REF)}$	Reference power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq 16.5V$,		.003	.01		.003	.01	%VR/%VS
V_{REF}	Reference voltage	$I_{REF} = 1.0mA$ $T_A = 25°C$	4.9	5.0	5.25	4.9	5.0	5.25	V
TC_{REF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$		60			60		ppm/°C
Z_{IN}	DAC V_{REF} IN input impedance	$I_{REF} = 1.0mA$ $T_A = 25°C$	4.15	5.0	5.85	4.15	5.0	5.85	KΩ
$I_{CC}+$	Positive supply current	$V_{CC}+ = 15V$		7	14		7	14	mA
$I_{CC}-$	Negative supply current	$V_{CC}- = -15V$		−10	−15		−10	−15	mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$		255	435		255	435	mW

NOTE

1. Refer to Figure 2.

AC ELECTRICAL CHARACTERISTICS[2] $V_{CC} = \pm 15V$, $T_A = 25°C$

PARAMETER		TO	FROM	TEST CONDITIONS	SE/NE5018			UNIT
					Min	Typ	Max	
T_{SLH}	Settling time	±½ LSB	Input	All bits low to high[3]		1.8		μs
T_{SHL}	Settling time	±½ LSB	Input	All bits high to low[4]		2.3		μs
t_{plh}	Propagation delay	Output	Input	All bits switched low to high[3]		300		ns
t_{phl}	Propagation delay	Output	Input	All bits switched high to low[4]		150		ns
t_{plsb}	Propagation delay	Output	Input	1 LSB change[3,4]		150		ns
t_{plh}	Propagation delay	Output	$\overline{LE}$	low to high transition[5]		300		ns
t_{phl}	Propagation delay	Output	$\overline{LE}$	high to low transition[6]		150		ns
t_s	Set-up time	$\overline{LE}$	Input	2, 7	100			ns
t_h	Hold time	Input	$\overline{LE}$	2, 7	50			ns
t_{pw}	Latch enable pulse width			2, 7	150			ns

NOTES

2. Refer to Figure 3.
3. See Figure 6.
4. See Figure 7.
5. See Figure 8.
6. See Figure 9.
7. See Figure 10.
8. For reference currents > 3mA, use of an external buffer is required.

8-BIT μP-COMPATIBLE D/A CONVERTER SE/NE5018

DC PARAMETRIC TEST CONFIGURATION

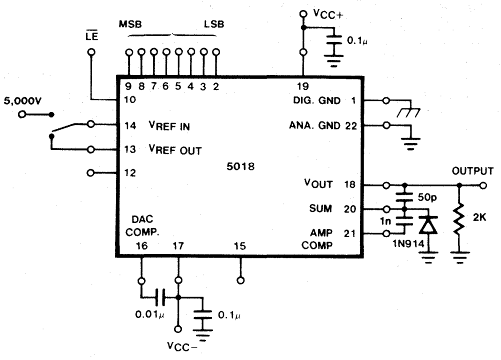


Figure 2

AC PARAMETRIC TEST CONFIGUTATION

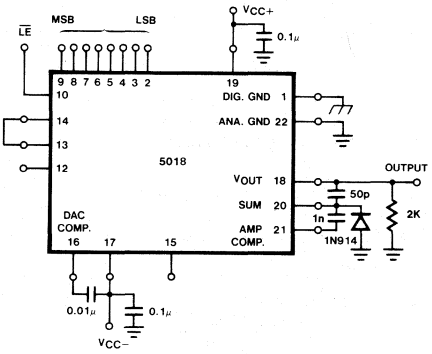


Figure 3

FULL/ZERO SCALE ADJUST—UNIPOLAR OUTPUT (0-10V)

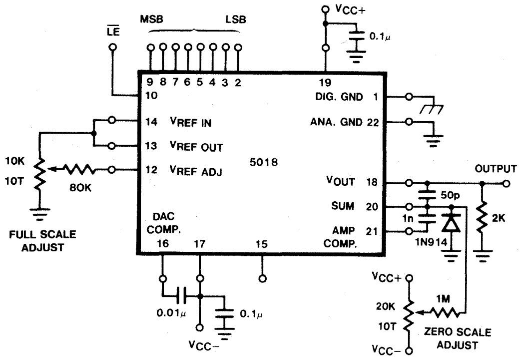


Figure 4

BIPOLAR OUTPUT OPERATION (−5 to +5V)

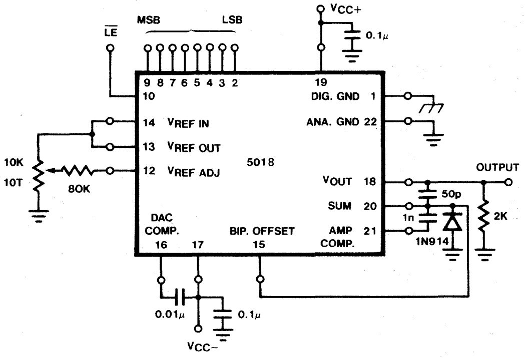


Figure 5

SETTLING TIME AND PROPAGATION DELAY, LOW TO HIGH DATA

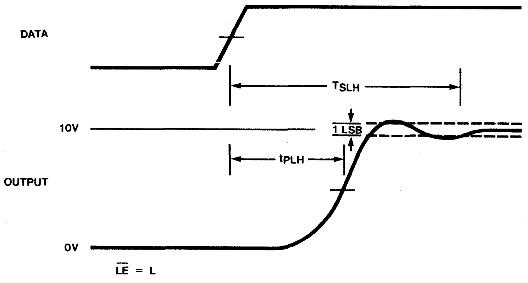


Figure 6

SETTLING TIME AND PROPAGATION DELAY, HIGH TO LOW DATA

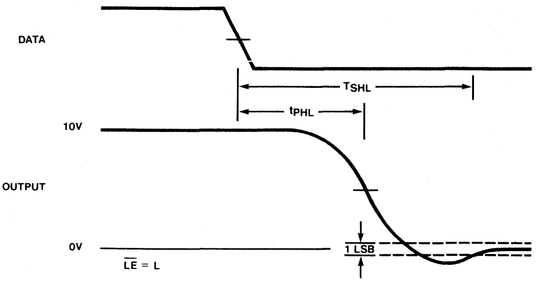


Figure 7

PROPAGATION DELAY, LATCH ENABLE TO OUTPUT

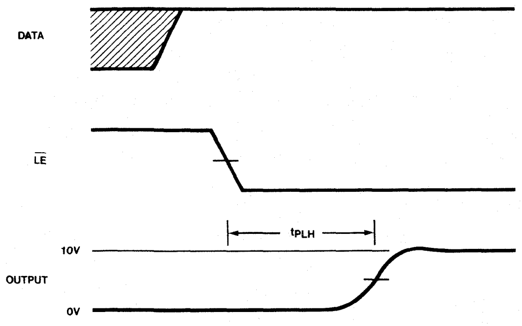


Figure 8

PROPAGATION DELAY, LATCH ENABLE TO OUTPUT

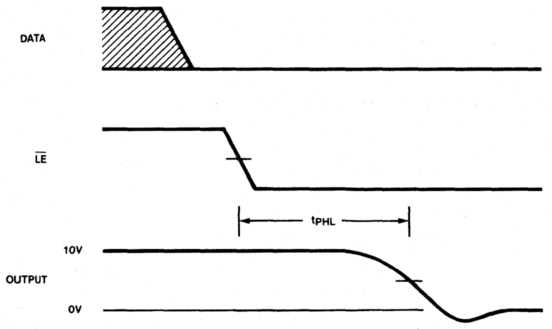


Figure 9

LATCH ENABLE PULSE WIDTH, SET-UP AND HOLD TIMES

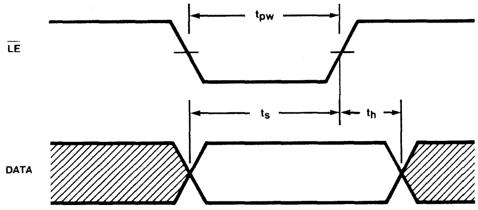


Figure 10

8-BIT μP-COMPATIBLE D/A CONVERTER SE/NE5019

DESCRIPTION

The NE5019 is a complete 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most micro-processors.

The chip also comprises a stable voltage reference (5V nominal) and a high slew rate buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

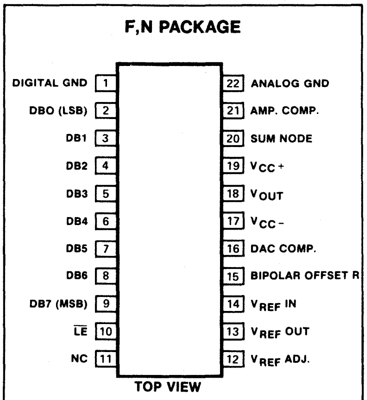
FEATURES

- **8-bit resolution**
- **Input latches**
- **Low-loading data inputs**
- **On-chip voltage reference**
- **Output buffer amplifier**
- **Accurate to ± 1/4 LSB (.1%)**
- **Monotonic to 8 bits**
- **Amplifier and reference both short-circuit protected**
- **Compatible with 8085, 6800 and many other μP's**

APPLICATIONS

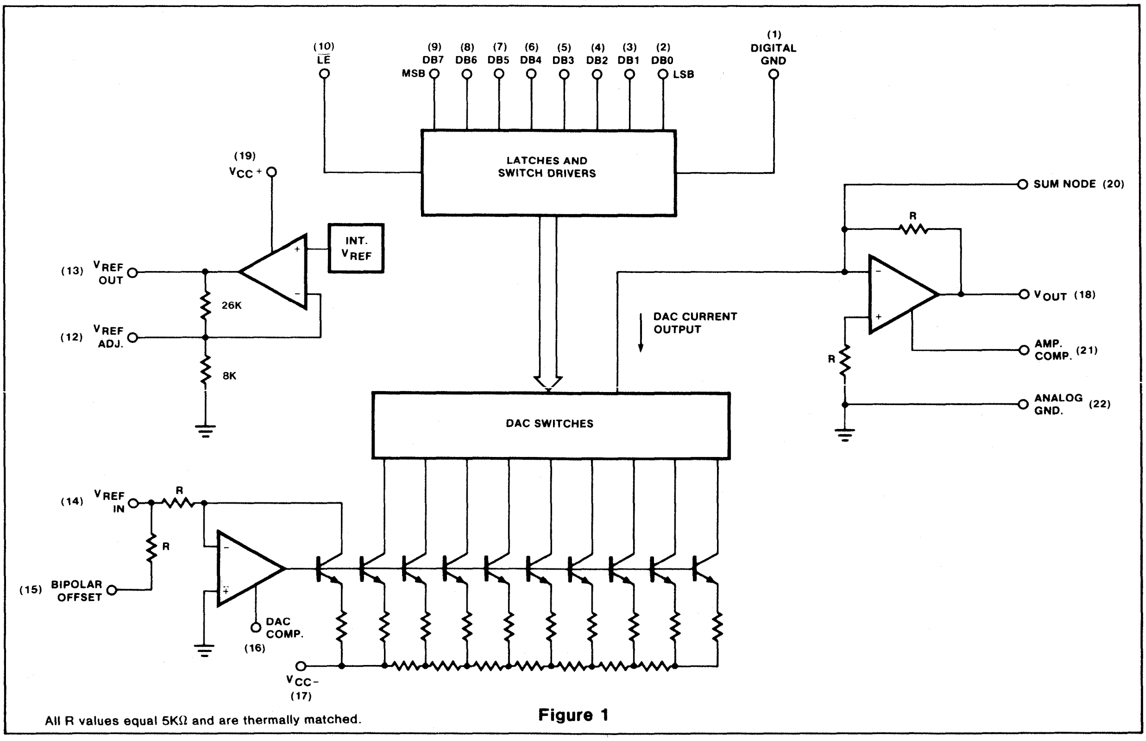
- **Precision 8-bit D/A converters**
- **A/D converters**
- **Programmable power supplies**
- **Test equipment**
- **Measuring instruments**
- **Analog-digital multiplication**

PIN CONFIGURATION



ORDER NUMBERS
NE5019F SE5019F
NE5019N

BLOCK DIAGRAM



All R values equal 5KΩ and are thermally matched.

Figure 1

8-BIT μP-COMPATIBLE D/A CONVERTER SE/NE5019

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	−18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF}IN$	Voltage at V_{REF} input	12	V
$V_{REF}ADJ$	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at V_{REF} OUT	Continuous	
I_{OUTSC}	Short-circuit current to ground or either supply at V_{OUT}	Continuous	
P_D	Power dissipation*		
	-N package	800	mW
	-F package	1000	mW
T_A	Operating temperature range		
	SE5019	−55 to +125	°C
	NE5019	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES
For N package, derate at 120°C/W above 35°C
For F package, derate at 75°C/W above 75°C

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5019. $-55°C \leq T_A \leq 125°C$, NE5019. $0°C \leq T_A \leq 70°C$ unless otherwise specified.[1] Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	SE5019			NE5019			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Relative accuracy				±0.1			±0.1	%FS
$V_{CC}+$	Positive supply voltage		11.4	15		11.4	15		V
$V_{CC}-$	Negative supply voltage		−11.4	−15		−11.4	−15		V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1 = 0V	2.0			2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1 = 0V			0.8			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1 = 0V, $2V < V_{IN} < 18V$		0.1	10		0.1	10	μA
$I_{IN(0)}$	Logic "0" input current	Pin 1 = 0V, $-5V < V_{IN} < 0.8V$		−2.0	−10		−2.0	−10	μA
V_{FS}	Full scale output voltage	Unipolar operation $V_{REF\ IN} = 5.000V$, $T_A = 25°C$	9.50	9.961	10.50	9.50	9.961	10.50	V
V_{FS}	Full scale output voltage	Bipolar operation	4.5	+4.961	5.5	4.5	+4.961	5.5	V
		$V_{REF\ IN} = 5.000V$, $T_A = 25°C$	-5.040	−5.000	-4.960	-5.040	−5.000	-4.960	
V_{ZS}	Zero scale voltage		-30	5	+30	-30	5	+30	mV
I_{OS}	Output short circuit current	$T_A = 25°C$ $V_{OUT} = 0V$		15	40		15	40	mA
PSR+(out)	Output power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01		.001	.01	%FS/%VS
PSR−(out)	Output power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq -16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01		.001	.01	%FS/%VS
TC_{FS}	Full scale temperature coefficient	$V_{REF\ IN} = 5.000V$		20			20		ppm/°C
TC_{ZS}	Zero scale temperature coefficient			5			5		ppm/°C

NOTE
1. Refer to Figure 2.

DC ELECTRICAL CHARACTERISTICS (Cont'd) $V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5019. $-55°C \leq T_A \leq 125°C$, NE5019. $0°C \leq T_A \leq 70°C$ unless otherwise specified.[1] Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	SE5019			NE5019			UNIT
			Min	Typ	Max	Min	Typ	Max	
I_{REF}	Reference output current	Note 8			3			3	mA
I_{REFSC}	Reference short circuit current	$T_A = 25°C$ $V_{REF\ OUT} = 0V$		15	30		15	30	mA
$PSR+_{REF}$	Reference power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, $I_{REF} = 1.0mA$		.003	.01		.003	.01	%VR/ %VS
$PSR-_{REF}$	Reference power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq 16.5V$,		.003	.01		.003	.01	%VR/ %VS
V_{REF}	Reference voltage	$I_{REF} = 1.0mA$ $T_A = 25°C$	4.9	5.0	5.25	4.9	5.0	5.25	V
TC_{REF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$		60			60		ppm/°C
Z_{IN}	DAC V_{REF}IN input impedance	$I_{REF} = 1.0mA$ $T_A = 25°C$	4.15	5.0	5.85	4.15	5.0	5.85	KΩ
$I_{CC}+$	Positive supply current	$V_{CC}+ = 15V$		7	14		7	14	mA
$I_{CC}-$	Negative supply current	$V_{CC}- = -15V$		−10	−15		−10	−15	mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$		255	435		255	435	mW

NOTE

1. Refer to Figure 2.

AC ELECTRICAL CHARACTERISTICS[2] $V_{CC} = \pm 15V$, $T_A = 25°C$

PARAMETER		TO	FROM	TEST CONDITIONS	SE/NE5019			UNIT
					Min	Typ	Max	
T_{SLH}	Settling time	± ½ LSB	Input	All bits low to high[3]		1.8		μs
T_{SHL}	Settling time	± ½ LSB	Input	All bits high to low[4]		2.3		μs
t_{plh}	Propagation delay	Output	Input	All bits switched low to high[3]		300		ns
t_{phl}	Propagation delay	Output	Input	All bits switched high to low[4]		150		ns
t_{plsb}	Propagation delay	Output	Input	1 LSB change[3,4]		150		ns
t_{plh}	Propagation delay	Output	$\overline{LE}$	low to high transition[5]		300		ns
t_{phl}	Propagation delay	Output	$\overline{LE}$	high to low transition[6]		150		ns
t_s	Set-up time	$\overline{LE}$	Input	2, 7	100			ns
t_h	Hold time	Input	$\overline{LE}$	2, 7	50			ns
t_{pw}	Latch enable pulse width			2, 7	150			ns

NOTES

2. Refer to Figure 3.
3. See Figure 6.
4. See Figure 7.
5. See Figure 8.
6. See Figure 9.
7. See Figure 10.
8. For reference currents > 3mA, use of an external buffer is required.

DC PARAMETRIC TEST CONFIGURATION

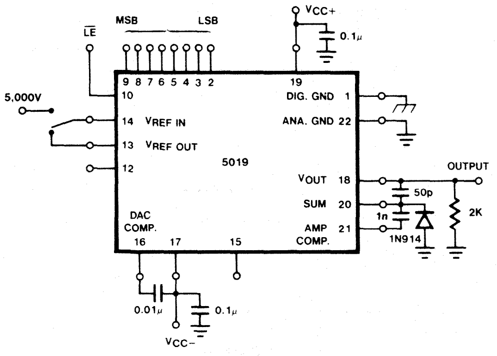


Figure 2

AC PARAMETRIC TEST CONFIGUTATION

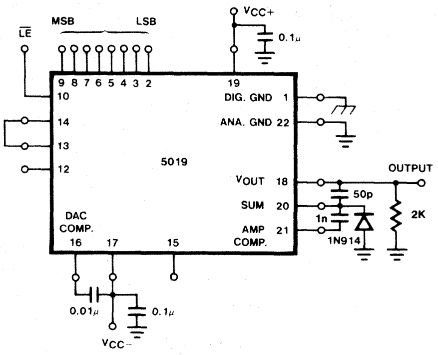


Figure 3

FULL/ZERO SCALE ADJUST—UNIPOLAR OUTPUT (0-10V)

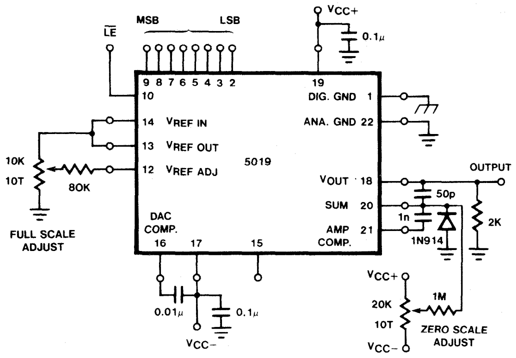


Figure 4

BIPOLAR OUTPUT OPERATION (−5 to +5V)

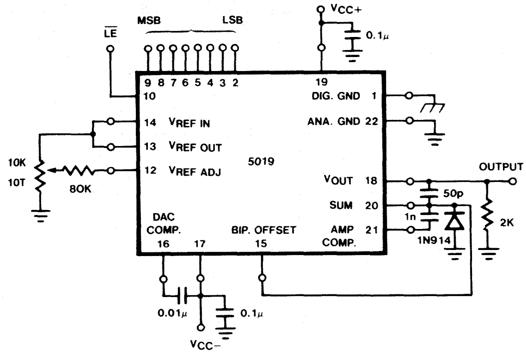


Figure 5

SETTLING TIME AND PROPAGATION DELAY, LOW TO HIGH DATA

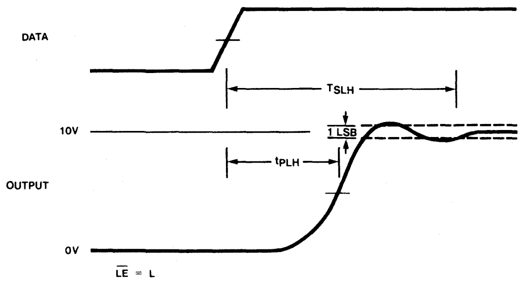


Figure 6

SETTLING TIME AND PROPAGATION DELAY, HIGH TO LOW DATA

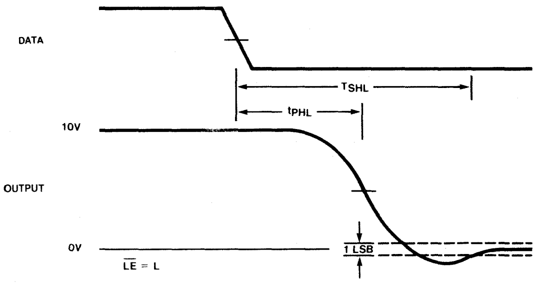


Figure 7

8-BIT μP-COMPATIBLE D/A CONVERTER SE/NE5019

PROPAGATION DELAY, LATCH ENABLE TO OUTPUT

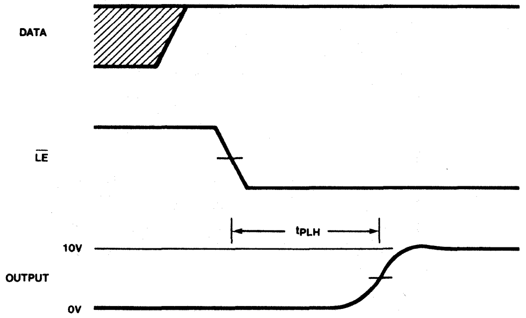


Figure 8

PROPAGATION DELAY, LATCH ENABLE TO OUTPUT

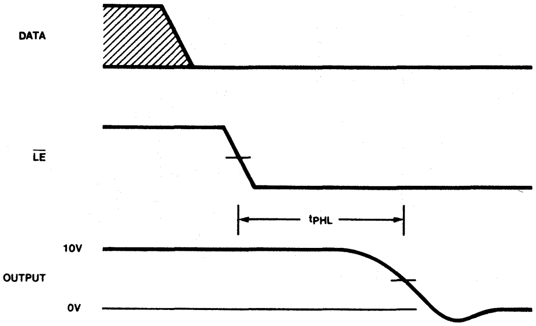


Figure 9

LATCH ENABLE PULSE WIDTH, SET-UP AND HOLD TIMES

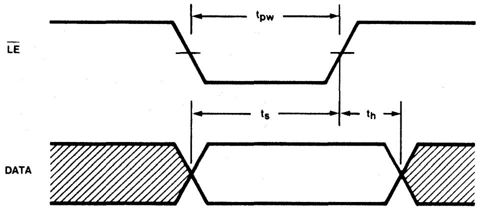


Figure 10

ANALOG DIVISION MARCH 1982

10-BIT µP-COMPATIBLE D/A CONVERTER NE5020

DESCRIPTION

The NE5020 is a microprocessor-compatible monolithic 10-bit digital to analog converter subsystem. This device offers 10-bit resolution and ±0.1% accuracy and monotonicity guaranteed over full operating temperature range.

Low loading latches, adjustable logic thresholds and addressing capability allow the NE5020 to directly interface with most microprocessor and logic controlled systems.

The NE5020 contains internal voltage reference, DAC switches and resistor ladder. Also, the input buffer and output summing amplifier are included. In addition, the matched application resistors for scaling either unipolar or bipolar output values are included on a single monolithic chip.

The result is a near minimum component count 10-bit resolution DAC system.

FEATURES

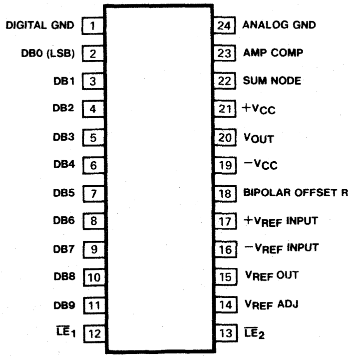
- **10-bit resolution**
- **Guaranteed monotonicity over operating range**
- **±0.1% relative accuracy**
- **Unipolar (0V to +10V) and Bipolar (±5V) output range**
- **Logic bus compatible**
- **5µsec settling time**

APPLICATIONS

- **Precision 10-bit D/A converters**
- **10-bit Analog to Digital converters**
- **Programmable power supplies**
- **Test equipment**
- **Measurement instruments**

PIN CONFIGURATION

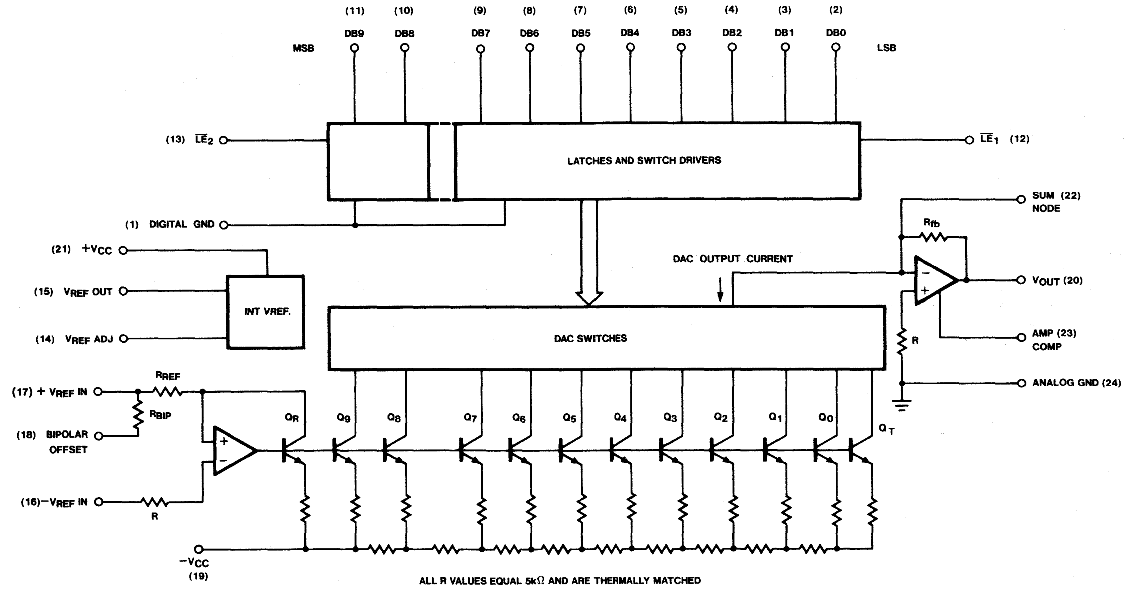
F, N PACKAGE



TOP VIEW

ORDER NUMBERS
NE5020F NE5020N

BLOCK DIAGRAM



ALL R VALUES EQUAL 5kΩ AND ARE THERMALLY MATCHED

Figure 1

10-BIT µP-COMPATIBLE D/A CONVERTER

NE5020

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	−18	V
V_{IN}	Logic input voltage	0 to 18	V
V_{REF} IN	Voltage at $+V_{REF}$ input	12	V
V_{REF} ADJ	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at V_{REF} OUT	Continuous	
I_{OUTSC}	Short-circuit current to ground or either supply at V_{OUT}	Continuous	
P_D	Power dissipation*		
	-N package	800	mW
	F package	1000	mW
T_A	Operating temperature range		
	NE5020	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES
For N package, derate at 120°C/W above 35°C
For F package, derate at 75°C/W above 75°C

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, $0°C \leq T_A \leq 70°C$ unless otherwise specified.[1]
Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	NE5020			UNIT
			Min	Typ	Max	
	Resolution				10	Bits
	Monotonicity				10	Bits
	Relative accuracy				±0.1	%FS
$V_{CC}+$	Positive supply voltage		11.4	15	16.5	V
$V_{CC}-$	Negative supply voltage		−11.4	−15	−16.5	V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1 = 0V	2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1 = 0V			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1 = 0V, $2V < V_{IN} < 18V$		0.1	10	µA
$I_{IN(0)}$	Logic "0" input current	Pin 1 = 0V, $-5V < V_{IN} < 0.8V$		−2.0	−10	µA
V_{FS}	Full scale output voltage	Unipolar operation $V_{REF\ IN} = 5.000V$, $T_A = 25°C$	9.5	9.9902	10.5	V
V_{FS}	Full scale output voltage	Bipolar operation	4.5	4.9902	5.5	V
		$V_{REF\ IN} = 5.000V$, $T_A = 25°C$	-5.040	−5.000	-4.960	
V_{ZS}	Zero scale voltage	Unipolar operation	-30	5	+30	mV
I_{OS}	Output short circuit current	$T_A = 25°C$ $V_{OUT} = 0V$		±15	±40	mA
$PSR+_{(out)}$	Output power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01	%FS/%VS
$PSR-_{(out)}$	Output power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq -16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01	%FS/%VS
TC_{FS}	Full scale temperature coefficient	$V_{REF\ IN} = 5.000V$		20		ppmFS/°C
TC_{ZS}	Zero scale temperature coefficient			5		ppmFS/°C

NOTE
1. Refer to Figure 2.

DC ELECTRICAL CHARACTERISTICS (Cont'd) $V_{CC}+ = +15V$, $V_{CC}- = -15V$, $0°C \leq T_A \leq 70°C$ unless otherwise specified.[1] Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	NE5020			UNIT
			Min	Typ	Max	
I_{REF}[2]	Reference output current				3	mA
$I_{REF\ SC}$	Reference short circuit current	$T_A = 25°C$ $V_{REF\ OUT} = 0V$		15	30	mA
$PSR+_{REF}$	Reference power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, $I_{REF} = 1.0mA$		.003	.01	%VR/ %VS
$PSR-_{REF}$	Reference power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq 16.5V$,		.003	.01	%VR/ %VS
V_{REF}	Reference voltage	$I_{REF} = 1.0mA$, $T_A = 25°C$	4.9	5.0	5.25	V
TC_{REF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$		60		ppm/°C
Z_{IN}	DAC V_{REF}IN input impedance	$I_{REF} = 1.0mA$		5.0		kΩ
$I_{CC}+$	Positive supply current	$V_{CC}+ = 15V$		7	14	mA
$I_{CC}-$	Negative supply current	$V_{CC}- = -15V$		−10	−15	mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$		255	435	mW

NOTE

1. Refer to Figure 2.
2. For I_{REF} OUT greater than 3mA, an external buffer is required.

AC ELECTRICAL CHARACTERISTICS[3] $V_{CC} = \pm 15V$, $T_A = 25°C$

PARAMETER		TO	FROM	TEST CONDITIONS	NE5020			UNIT
					Min	Typ	Max	
T_{SLH}	Settling time	± ½ LSB	Input	All bits low to high[4]		5		µs
T_{SHL}	Settling time	± ½ LSB	Input	All bits high to low[5]		5		µs
t_{plh}	Propagation delay	Output	Input	All bits switched low to high[4]		300		ns
t_{phl}	Propagation delay	Output	Input	All bits switched high to low[5]		150		ns
t_{plsb}	Propagation delay	Output	Input	1 LSB change[4,5]		150		ns
t_{plh}	Propagation delay	Output	$\overline{LE}$	low to high transition[6]		300		ns
t_{phl}	Propagation delay	Output	$\overline{LE}$	high to low transition[7]		150		ns
t_s	Set-up time	$\overline{LE}$	Input	3, 8	100			ns
t_h	Hold time	Input	$\overline{LE}$	3, 8	50			ns
t_{pw}	Latch enable pulse width			3, 8	150			ns

NOTES

3. Refer to Figure 3.
4. See Figure 6.
5. See Figure 7.
6. See Figure 8.
7. See Figure 9.
8. See Figure 10.

10-BIT µP-COMPATIBLE D/A CONVERTER NE5020

DC PARAMETRIC TEST CONFIGURATION

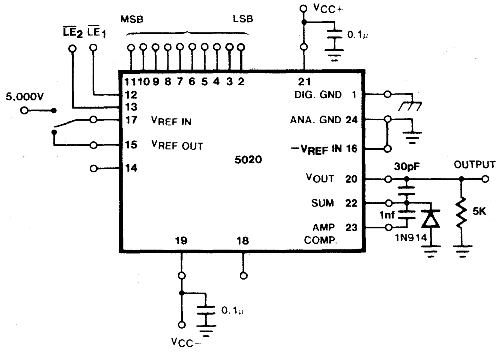


Figure 2

AC PARAMETRIC TEST CONFIGURATION

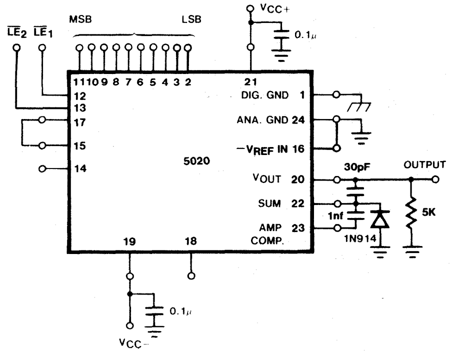


Figure 3

FULL/ZERO SCALE ADJUST—UNIPOLAR OUTPUT (0–10V)

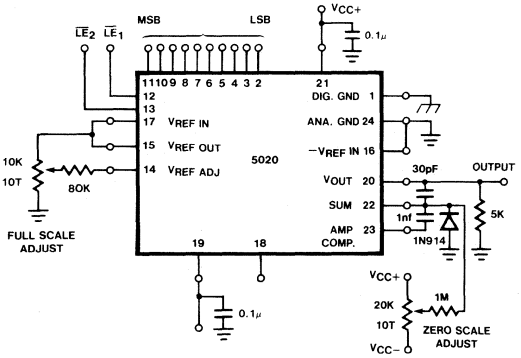


Figure 4

BIPOLAR OUTPUT OPERATION (−5 to +5V)

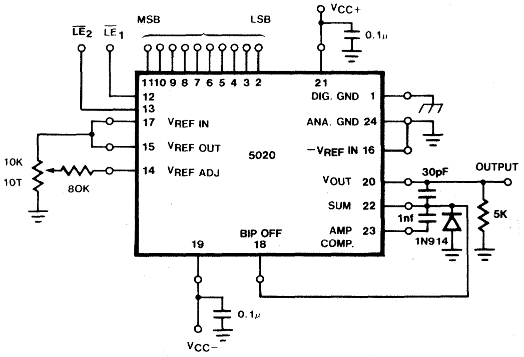


Figure 5

SETTLING TIME AND PROPAGATION DELAY, LOW TO HIGH DATA

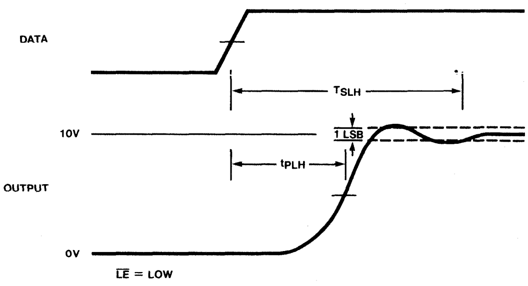


Figure 6

SETTLING TIME AND PROPAGATION DELAY, HIGH TO LOW DATA

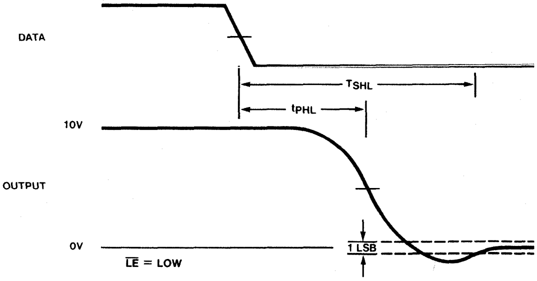


Figure 7

10-BIT µP-COMPATIBLE D/A CONVERTER NE5020

PROPAGATION DELAY, LATCH ENABLE TO OUTPUT

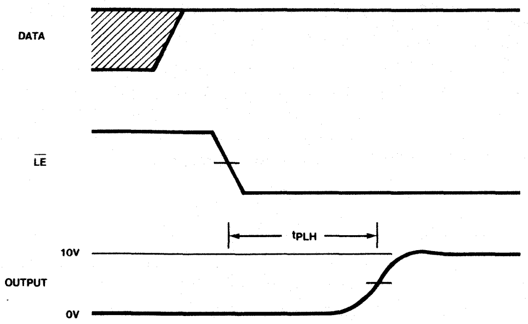


Figure 8

PROPAGATION DELAY, LATCH ENABLE TO OUTPUT

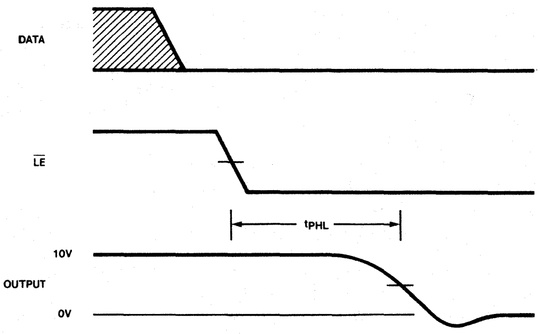


Figure 9

LATCH ENABLE PULSE WIDTH, SET-UP AND HOLD TIMES

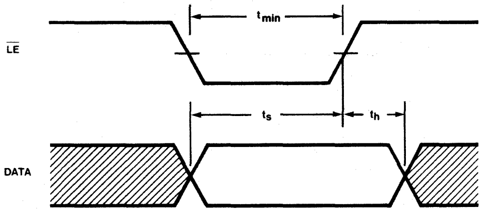


Figure 10

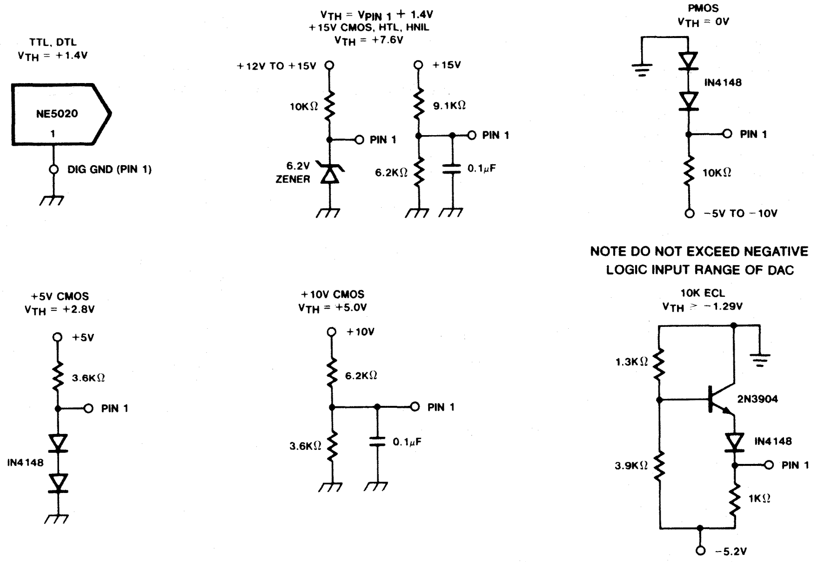


Figure 11

10-BIT μP-COMPATIBLE D/A CONVERTER NE5020

CIRCUIT DESCRIPTION

The NE5020 provides ten data latches, an internal voltage reference, application resistors, and a scaled output voltage, in addition to the basic DAC components (see block diagram, figure 1).

Latch Circuit

Digital interface with the NE5020 is readily accomplished through the use of two latch enable ports ($\overline{LE}_1$ and $\overline{LE}_2$) and ten data input latches. $\overline{LE}_2$ controls the two most significant bits of data (DB_9 and DB_8) while $\overline{LE}_1$ controls the eight lesser significant bits (DB_7 through DB_ϕ). Both the latch enable ports ($\overline{LE}$) and the data inputs are static and threshold sensitive. When the latch enable ports ($\overline{LE}$) are high (Logic '1') the data inputs become very high impedances and essentially disappear from the data bus. Addressing the $\overline{LE}$ with a low (Logic '0') the latches become active and adapt the logic states present on the data bus. During this state, the output of the DAC will change to the value proportional to the data bus value. When the latch enable returns to a high state, the selected set of data inputs (i.e., depending on which $\overline{LE}$ goes high) 'memorize' the data bus logic states and the output changes to the unique output value corresponding to the binary word in the latch.

The data inputs are inactive and high impedance (typically requiring −2μA for low (.8V max) or 0.1μA for high (2.0V min)) when the $\overline{LE}$ is high. Any changes on the data bus with $\overline{LE}$ high will have no effect on the DAC output.

The digital logic inputs ($\overline{LE}$ and DB) for the NE5020 utilize a differential input logic system with a threshold level of +1.4 volts with respect to the voltage level on the digital ground pin (Pin 1). Figure 11 details several bias schemes used to provide the proper threshold voltage levels for various logic families.

To be compatible with a bus orientated system the DAC should respond in as short a period as possible to insure full utilization of the microprocessor, controller and I/O control lines. Figure 10 shows the typical timing requirements of the latch and data lines. This figure indicates that data on the data bus should be stable for at least 50nsec after $\overline{LE}$ is changed to a high state.

The independent $\overline{LE}$ ($\overline{LE}_1$ and $\overline{LE}_2$) lines allow for direct interface from an 8 bit data bus (see figure 12). Data for the two MSB's is supplied and stored when $\overline{LE}_2$ is activated low and returned high according to the NE5020 timing requirements. Then $\overline{LE}_1$ is activated low and the remaining eight LSB's of data are transferred into the DAC. With $\overline{LE}_1$ returning high the loading of ten bit data word from an eight bit data bus is complete.

Occasionally the analog output must change to its data value within one data address operation. This is no problem using the NE5020 on a 16 bit bus or any other data bus with 10 or greater data bits.

This can be accomplished from an 8 bit data bus by utilizing an external latch circuit to preload the two MSB data values. Figure 13 shows the circuit configuration.

After preloading (via $\overline{LE}$ pre-load) the external latch with the two MSB values, $\overline{LE}_2$ is activated low and the eight LSB's and the

NE5020 μP INTERFACE 8-BIT DATA BUS EXAMPLE

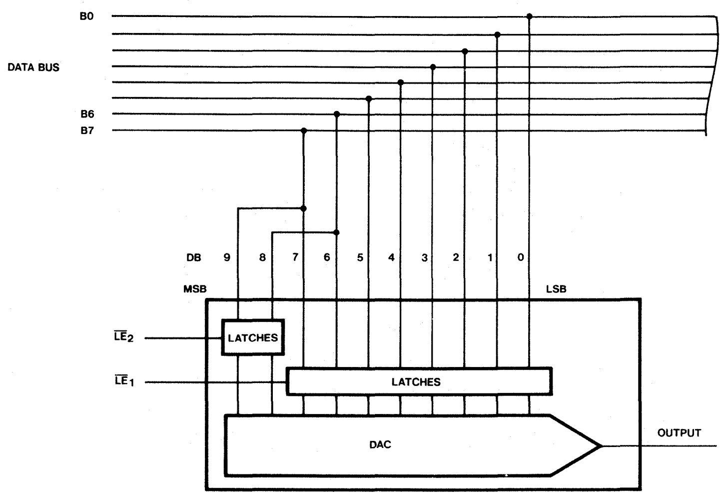


Figure 12

PRELOADING THE 2 MSB'S TO PROVIDE A SINGLE STEP OUTPUT

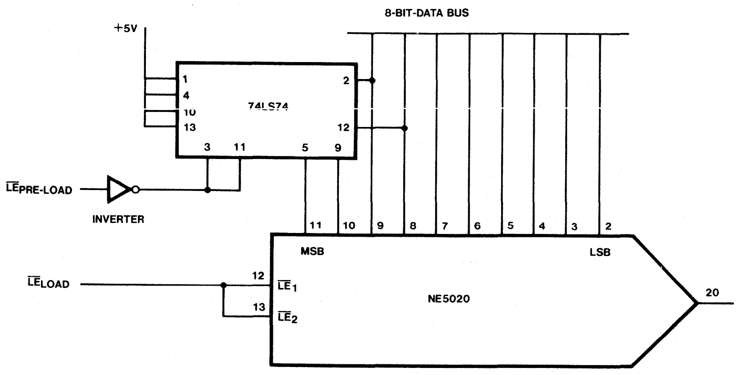


Figure 13

two MSB's are concurrently loaded into the DAC in one address operation. This permits the DAC output to make its appropriate change at one time.

Reference Interface

The NE5020 contains an internal bandgap voltage reference which is designed to have a very low temperature coefficient and excellent long term stability characteristics.

The internal bandgap reference (1.23V) is buffered and amplified to provide the 5 volt reference output. Providing a V_{REF}ADJ (pin 14) allows trimming of the reference output. Utilization of the adjust circuit shown in figure 16 performs not only V_{REF} adjustment but also full scale output adjust. Notice that the V_{REF}ADJ pin is essentially the sum node of an op amp and is sensitive to excessive node capacitance. Any capacitance on the node can be minimized by placing the external resistors as close as possible to the V_{REF}ADJ pin and observing good layout practices.

The V_{REF} out node can drive loads greater than the DAC V_{REF} input requirements and can be used as an excellent system voltage reference. However, to minimize load effects on the DAC system accuracy, it is recommended that a buffer amplifier is used.

Input Amplifier

The DAC reference amplifier is a high gain internally compensated op amp used to convert the input reference voltage to a precision bias current for the DAC ladder network.

Figure 1 details the input reference amplifier and current ladder. The voltage to current converter of the DAC amp will generate a 1mA reference current through Q_R with a 5 volt V_{REF}. This current sets the input bias to the ladder network. Data bit 9 (DB_9)(Q_9), when turned on, will mirror this current and will contribute 1mA to the output. DB_8 (Q_8) will contribute ½ of that value or 0.5mA and so on. These current values act as current sinks and will add at the sum node to produce a DAC ladder to sum node function of:

$$I_{OUT} = \frac{2V_{REF}}{R_{REF}} \left(\frac{DB9}{2} + \frac{DB8}{4} + \frac{DB7}{8} + \frac{DB6}{16} + \frac{DB5}{32} + \frac{DB4}{64} + \frac{DB3}{128} + \frac{DB2}{256} + \frac{DB1}{512} + \frac{DB0}{1024} \right)$$

Because of the fixed internal compensation of the reference amp, the slew rate is limited to typically 0.7V/μsec and source impedances at the $V_{REF\ INPUT}$ greater than 5kΩ should be avoided to maintain stability.

The $-V_{REF\ INPUT}$ pin is uncommitted to allow utilization of negative polarity reference voltages. In this mode $+V_{REF\ INPUT}$ is grounded and the negative reference is tied directly to the $-V_{REF\ INPUT}$. The $-V_{REF\ INPUT}$ contains a 5kΩ resistor that matches a like resistor in the $+V_{REF\ INPUT}$ to reduce voltage offset caused by op amp input bias currents.

Output Amplifier and Interface

The NE5020 provides an on chip output op amp to eliminate the need for additional external active circuits. Its two stage design with feed forward compensation allows it to slew at 15V/μsec and settle to within ± ½LSB in 5μsec. These times are typical when driving the rated loads of $R_L \geq 5k$ and $C_L \leq 50pF$ with recommended values of C_{FF} = 1nF and C_{FB} = 30pF. Typical input offset voltages of 5mV and 50k open loop gain insure an accurate current to voltage conversion is performed when using the on chip R_{FB} resistor. R_{FB} is matched to R_{REF} and R_{BIP} to maintain accurate voltage gain over operating conditions. The diode shown from ground to sum node prevents the DAC current switches from saturating the op amp during large signal transitions which would otherwise increase the settling time.

The output op amp also incorporates output short circuit protection for both positive and negative excursions. During this fault condition I_{OUT} will limit at ± 15mA typical. Recovery from this condition to rated accuracy will be determined by duration of short circuit and die temperature stabilization.

Bipolar Output Voltage

The NE5020 includes a thermally matched resistor, R_{BIP}, to offset the output voltage by 5 volts to obtain −5V to +5V output voltage range operation. This is accomplished by shorting pins 18 and 22 (see figure 14). This connection produces a current equal to ($V_{REF\ IN} - V_{sum\ node}$) ÷ R_{BIP}, (1mA nominal), which is injected into the sum node. Since full scale current out is approximately 2mA (1.9980mA), (2mA − 1mA)5k = 5V will appear at the output. For zero DAC output currents, 1mA is still injected into sum mode and V_{OUT} = −(5k)(1mA) = −5V. Zero scale adjust and full scale adjust are performed as described below, noting that full scale voltage is now approximately +5 volts, zero scale adjust may be used to trim V_{OUT} = 0.00 with the MSB high or V_{OUT} = −5.0V with all bits off.

Zero Scale Adjustment

The method of trimming the small offset error that may exist when all data bits are low is shown in figure 15. The trim is the result of injecting a current from resistor R_2 that counteracts the error current. Adjusting potentiometer R_1 until V_{OUT} equals 0.000 volts in the unipolar mode or −5.000 volts in the bipolar mode (see bipolar section) accomplishes this trim.

Full Scale Adjustment

A recommended full scale adjustment circuit when using the internal voltage reference is shown in figure 16. Potentiometer R_3 is adjusted until V_{OUT} equals 9.99023V. In many applications where the absolute accu-

BIPOLAR OUTPUT

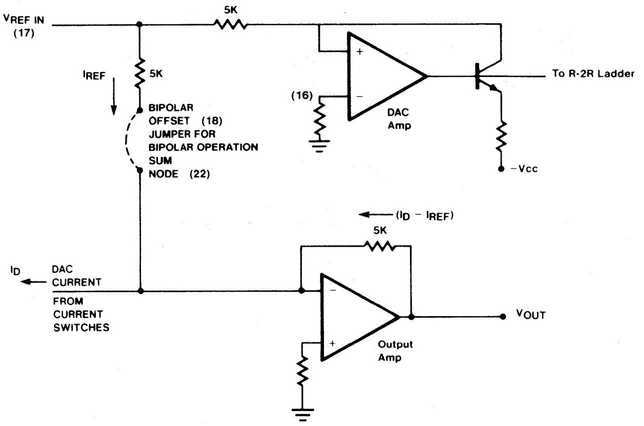


Figure 14

racy of full scale is of low importance when compared to the other system accuracy factors, then this adjustment circuit is optional.

As resistors R_{REF}, R_{fb} and R_{BIP} shown in figure 1 are integrated in close proximity, they match and track in value closely over wide ambient temperature variations. Typical matching is less than ±0.3% which implies that typical full scale (or gain) error is less than ±0.3% of ideal full scale value.

ZERO SCALE ADJUSTMENT

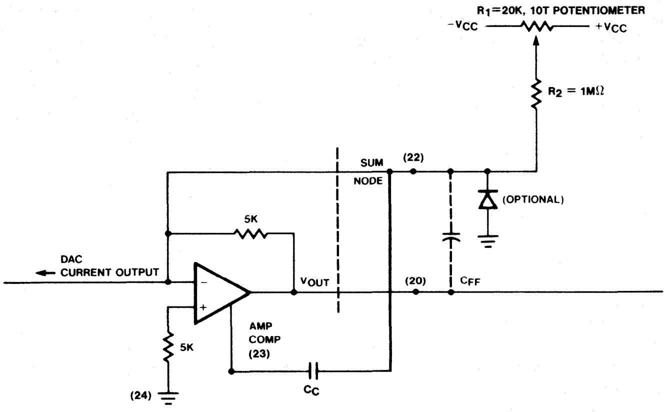


Figure 15

REFERENCE ADJUST CIRCUIT

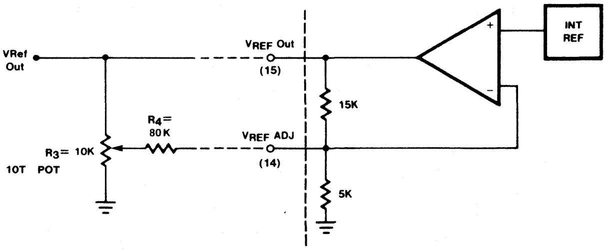


Figure 16

8-BIT GENERAL PURPOSE A/D CONVERTER NE5034

DESCRIPTION

The NE5034 is a high-speed microprocessor-compatible 8-bit Analog-to-Digital converter. It uses the successive approximation conversion technique, and includes the comparator, reference DAC, SAR, an internal clock and three-state buffers all on the same chip.

The converter can accommodate a wide analog input voltage range, bipolar or unipolar, selectable through external input resistors. An external capacitor controls the internal clock frequency, providing conversion times down to 17μs. Faster conversion times are possible using an external clock.

Microprocessor interfacing requirements are simple, allowing analog-to-digital conversion with a minimum of external components.

FEATURES

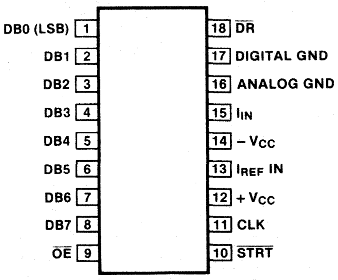
- **8-bit resolution and accuracy**
- **Accepts unipolar or bipolar inputs**
- **Three-state output buffers for easy microprocessor interface**
- **Choice of internal or external clocking**
- **Short conversion time, 17μs typical using internal clock**

APPLICATIONS

- **All microprocessor-based monitoring and control systems requiring analog signal inputs.**
- **Typical applications include: Automated process control, machine tools, robots, test and measurement instruments, environmental controls**
- **Other applications include: Ratiometric A/D conversion, very high resolution A/D conversion systems requiring high speed 8-bit building blocks**

PIN CONFIGURATION

F,N PACKAGE



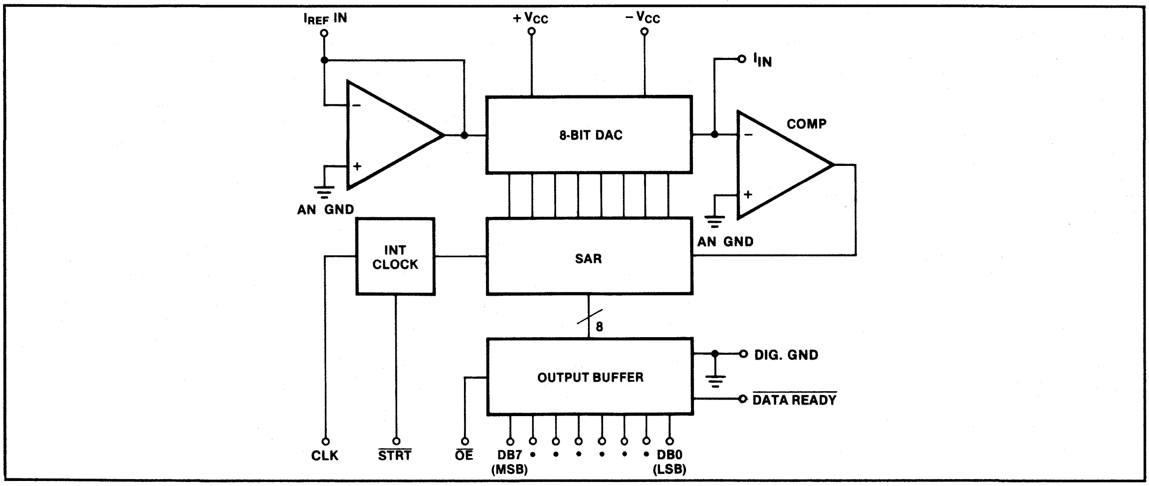
TOP VIEW

ORDER NUMBERS
NE5034F, NE5034N

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
$V_{CC}+$	Positive supply voltage	0 to +6	V
$V_{CC}-$	Negative supply voltage	0 to −15	V
I_{REF}	Reference current	1.5	mA
I_{IN}	Analog input current	5.0	mA
V_O	Data output voltage	6.0	V
Analog GND to Digital GND		1.0	V
V_L	Logic input voltage	−1 to $V_{CC}+$	V
P_D	Power dissipation		
	N package	800	mW
	F package	1000	mW
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

BLOCK DIAGRAM



8-BIT GENERAL PURPOSE A/D CONVERTER NE5034

DC ELECTRICAL CHARACTERISTICS $+V_{CC} = 5.0V$, $-V_{CC} = -12V$, $0°C \leq T_A \leq 70°C$ unless otherwise specified

SYMBOL AND PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution		8	8	8	Bits
	Relative accuracy error[1, 2]				± 1/2	LSB
$V_{CC}+$	Positive supply range		4.75	5.0	5.25	V
$V_{CC}-$	Negative supply range		−11.4	− 12	−12.6	V
E_{FS}	Full scale gain error	$I_{REF} = 1.0mA$, $T_A = 25°C$		± 2	± 5	LSB
E_{ZS}	Zero scale offset error	$I_{REF} = 1.0mA$, $T_A = 25°C$		± 0.5	± 1	LSB
Psr	Power supply rejection[3]	$I_{REF} = 1.0$ mA, V_{CC} + 4.75 to + 5.25V, V_{CC} − 11.4 to − 12.6V			± 1/2	LSB
V_{IH}	Logic 1 input voltage ($\overline{\text{STRT}}$ and $\overline{\text{OE}}$)		2.0			V
V_{IH}	Logic 1 input voltage ext. clock		2.4			V
V_{IL}	Logic 0 input voltage ($\overline{\text{STRT}}$ and $\overline{\text{OE}}$)				0.8	V
V_{IL}	Logic 0 input voltage ext clock				0.7	V
I_{IH}	Logic 1 input current ($\overline{\text{STRT}}$ and $\overline{\text{OE}}$)	$V_{IN} = 2.4V$			20	μA
I_{IH}	Logic 1 input current ext clock	$V_{IN} = 2.4V$		100		μA
I_{IL}	Logic 0 input current ($\overline{\text{STRT}}$ and $\overline{\text{OE}}$)	$V_{IN} = 0.4V$		− 20	− 100	μA
I_{IL}	Logic 0 input current ext. clock	$V_{IN} = 0.7V$		− 100		μA
V_{OL}	Logic 0 output voltage	$I_{OL} = 1.6mA$, $\overline{\text{OE}} = 0.8V$			0.4	V
V_{OH}	Logic 1 output voltage	$I_{OH} = 400\mu A$, $\overline{\text{OE}} = 0.8V$	2.4			V
I_{OZ}	Three-state leakage	$\overline{\text{OE}} = 2.0V$, $V_{OL} = 0V$ or 5V		± 10		μA
I_{CC+}	Positive supply current	$V_{CC}+ 5V$, $V_{CC}- 12V$		18	36	mA
I_{CC}	Negative supply current	$V_{CC}+ 5V$, $V_{CC}- 12V$		− 11	− 22	mA

NOTES

1. Relative accuracy is defined as the deviation of the code transition points from the ideal code transition points on a straight line drawn from zero scale to full scale of the device.
2. Specifications given in LSBs refer to the weight of the least significant bit at the 8-bit level which is 0.39% of the full scale voltage.
3. MAX change in full scale.

AC ELECTRICAL CHARACTERISTICS $V+ = +5V$, $V- = -12V$, $T_A = 25°C$

SYMBOL & PARAMETER	TO	FROM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Internal clock frequency			$C_L = 60pF$ (See Figure 1)		500		KHz
External clock frequency						700	KHz
Tw $\overline{\text{STRT}}$ pulse width			Clock freq. = 500KHz	400			ns
External clock pulse width positive/negative				600			ns
Set up time[1]			See Figure 3	300			ns
tp (out data) propagation delay	data out	$\overline{\text{OE}}$	See Figure 2		50	200	ns
tp (out $\overline{\text{DR}}$) propagation delay	data ready out	8th clock	See Figure 3		700		ns
tp (3-state) propagation delay 3-state	high impedance o/p	$\overline{\text{OE}}$	See Figure 2		60	200	ns
tp (DB0) propagation delay	DB0	$\overline{\text{DR}}$	See Figure 3			500	ns
tp (SDR) $\overline{\text{STRT}}$ low to $\overline{\text{DR}}$ high	data ready high	$\overline{\text{STRT}}$ low	See Figure 3		700		ns

NOTE

1. See description of "Set up time".

8-BIT GENERAL PURPOSE A/D CONVERTER NE5034

TYPICAL PERFORMANCE CHARACTERISTICS

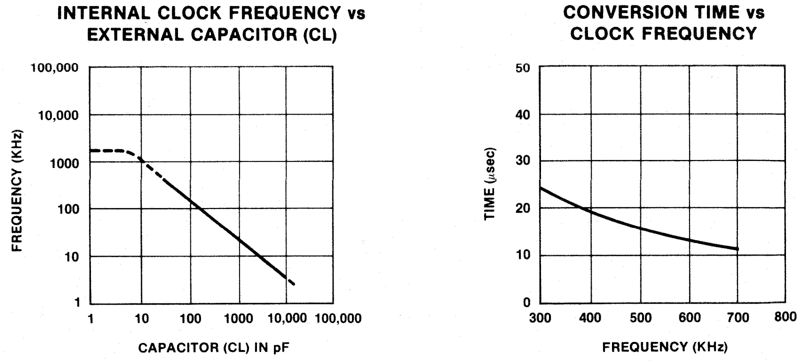
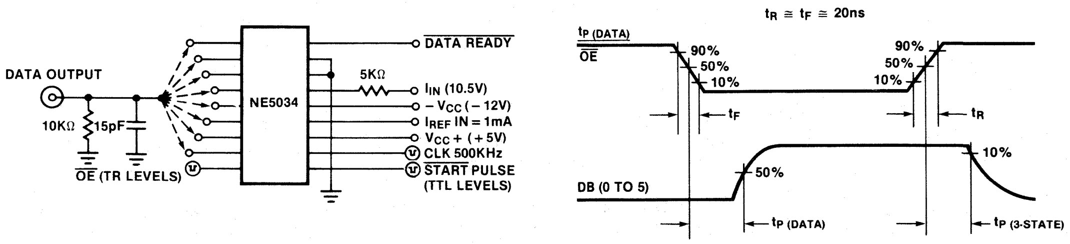


FIGURE 1

TEST LOAD CIRCUITS

DATA OUTPUT HIGH



DATA OUTPUT LOW

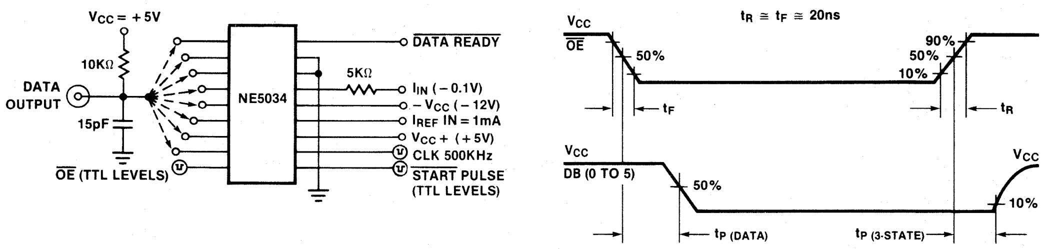


FIGURE 2

8-BIT GENERAL PURPOSE A/D CONVERTER NE5034

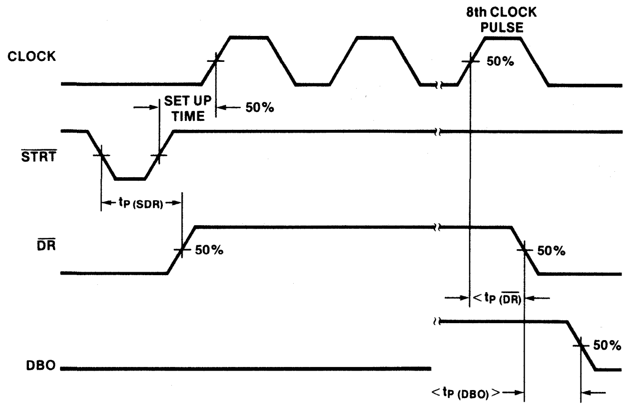


FIGURE 3

FUNCTIONAL PIN DEFINITIONS

DATA READY (DR)

This is an output pin used to indicate that a conversion is in progress. DR goes to a logic "1" when STRT is at a logic "0". At the completion of a conversion DR returns to a logic "0". There is a delay (MAX 0.5μs) from the time DR goes to "0" to the time DB0 data is valid.

DB0-DB7

Eight three-state data outputs each with a drive capability of one TTL load. DB0 is the LSB and DB7 is the MSB.

OE

Output enable input. When OE is at a logic "1" the data outputs assume a high impedance state. With OE at a logic "0", data is placed on the outputs. Data appearing on the outputs is only valid if both OE and DR are at logic "0" (see note on DR timing).

STRT

This pin is used to reset the converter and start a new conversion. A logic "0" applied to this pin for a minimum of 400ns will reset the converter to a condition with DB7 at a logic "1" and all other Data outputs at logic "0". It will also cause DR to go to a logic "1" (see timing diagrams for delay times). Conversion will start with the 1st clock pulse after STRT returns to a logic "1" (see notes on set up time required). A STRT pulse while a conversion is taking place will cause the conversion to be aborted and the converter will reset. (See notes on short-cycle operation.)

CLK IN

An external capacitor between this pin and ground generates the internal clock pulses. (See diagram for clock frequency vs capacitor value). In order to synchronize the internal clock, to the start pulse a diode (small signal type e.g., 1N914) should be connected between STRT and CLK IN (see Figures 4 and 5). Without this diode the start pulse could occur at a time which could cause one of the conditions described in the Note on "set up" time. Applying an external TTL-or MOS-compatible clock to this pin slaves the NE5034 to external clock frequency. In this case, the diode is not required but the "set up" time requirements should be noted.

BASIC CIRCUIT DESCRIPTION

The NE5034 is an 8-bit A/D converter which incorporates the successive-approximation conversion method. Upon receipt of the STRT pulse, successive bits, beginning with the MSB (DB7), are applied to the input of the internal 8-bit current output DAC by the I^2L successive-approximation register (SAR) (see Block Diagram).

The comparator determines whether the output current of the DAC is greater or less than the input current converted from the unknown analog input voltage through an external input resistor. If the DAC output current is greater, the data latch for the trial bit is reset to a '0'; if it is less, the trial data bit stays at '1'. After all the bits from DB7 to DB0 have been tried, the SAR contains a valid 8-bit binary output code which accurately represents the unknown analog input to within ± 1/2 LSB (± 0.2%). This binary output will now remain in the SAR until another STRT pulse is applied.

During the successive-approximation sequence, the DATA READY signal remains at '1'. Upon completion of the conversion, the signal goes to a '0', indicating that data is valid and ready. If the OE input is left at a '0' during the conversion, the DATA OUTPUT shows the conversion sequence (see short cycle section). When the OE line is made a logic '1', the output buffers will go to a high impedance state and will remain so until the OE is returned to a '0' state.

TIMING DESCRIPTION

The timing diagram shown in Figure 7 shows the successive trial and decisions for each data bit.

With STRT at a logic "0" the converter is reset to a condition with DB7 at a logic "1", DR at a logic "1" and DB0-DB6 at logic "0".

Conversion starts after STRT returns to a logic "1". Starting with DB7 each bit is tried in turn, with the decision point being at the time of the positive going edge of the clock. Starting with the first positive edge after STRT returns to logic "1" (see note on "set up" time). The 8th positive going edge makes the decision on DB0 (LSB) and also causes DR to return to a logic "0" to indicate the conversion is complete. (See note on DR timing.)

SHORT-CYCLE OPERATION

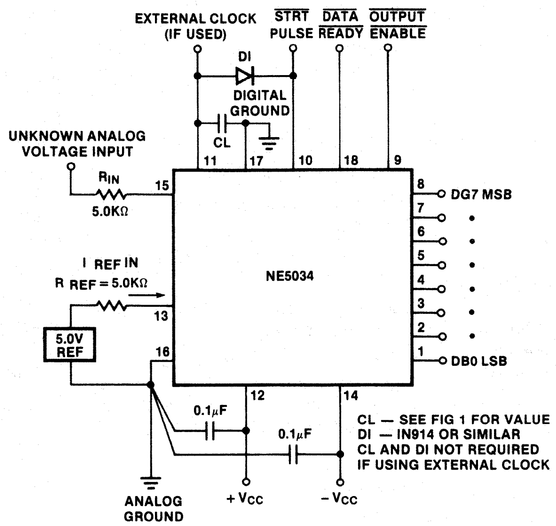
In applications where less than 8 bits of resolution are required the NE5034 can be operated to achieve shorter conversion times. No hard wire changes are required to perform "short-cycling".

Conversion to X number of bits is completed at the end of X + 0.5 clock cycles (after a start pulse) DR will still be at a logic "1" state.

OE can be used to 3-state the outputs even during short-cycle operation.

8-BIT GENERAL PURPOSE A/D CONVERTER NE5034

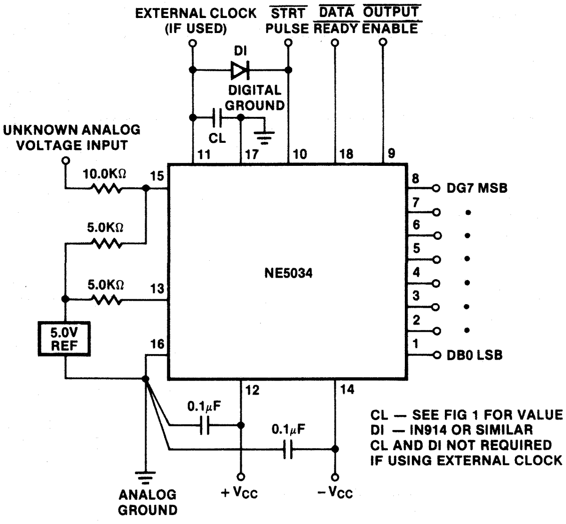
BASIC SET-UP DIAGRAM UNIPOLAR INPUT VALUES (0→10V)



CL — SEE FIG 1 FOR VALUE
DI — IN914 OR SIMILAR
CL AND DI NOT REQUIRED
IF USING EXTERNAL CLOCK

FIGURE 4.

BASIC SET-UP DIAGRAM BIPOLAR INPUT VALUES (± 10V RANGE)



CL — SEE FIG 1 FOR VALUE
DI — IN914 OR SIMILAR
CL AND DI NOT REQUIRED
IF USING EXTERNAL CLOCK

FIGURE 5.

8-BIT GENERAL PURPOSE A/D CONVERTER NE5034

SET UP TIME

When using an external clock, the positive going edge of the start pulse must be synchronized to the clock pulse. There is a "set up" time of 300ns required between the time of the start pulse returning to a logic "1" and the next positive going edge of the clock.

If the positive edge of the start pulse occurs less than 300ns prior to the positive clock edge, one of the following conditions will occur:

a) The converter recognizes the clock pulse and converts as normal.
b) The conversion starts one clock pulse later.
c) The conversion never starts, this will be indicated by the fact that $\overline{DR}$ does not return to logic "0". In this case a new start pulse will be required.

DATA READY ($\overline{DR}$) TIMING

After $\overline{DR}$ returns to a logic "0" indicating a conversion is complete there is a time delay of 500ns before the data at DB0 output (the Least Significant Bit) is valid.

ZERO OFFSET (NEGATIVE FULL SCALE) CALIBRATION PROCEDURES

1. Apply continuous start pulses to the $\overline{STRT}$ input.
2. Apply 1/2 LSB in the case of unipolar operation, or 1/2 LSB above − FS in the case of bipolar operation to the analog input.
3. Observe all data outputs after each conversion is completed.
4. Adjust the potentiometer connected to I_{IN} (see Figure 6) until the LSB flickers between '0' and '1', and all other data outputs remain '0' following each conversion.

FULL SCALE (POSITIVE FULL SCALE) CALIBRATION:

1. Apply continuous start pulses to the $\overline{STRT}$ input.
2. Apply full scale minus 1 1/2 LSB to the analog input.
3. Observe all data outputs after each conversion is completed.
4. Adjust the voltage applied to $V_{REF\ IN}$ (Figure 4) until the LSB varies between '0' and '1', and all other data outputs stay '1' after each conversion.

NOTE:

1. Where an input of 1/2 LSB is called for, the voltage is equal to $\frac{FS}{256}$.
2. The sequence of calibration should be:
   a. Zero offset
   b. Full scale adjust
   c. Zero offset
   d. Full scale adjust

OPERATING PRECAUTIONS:

Analog and digital grounds should have separate returns. Noise and jitter on digital ground will degrade accuracy unless the input is referenced to a 'clean' analog ground.

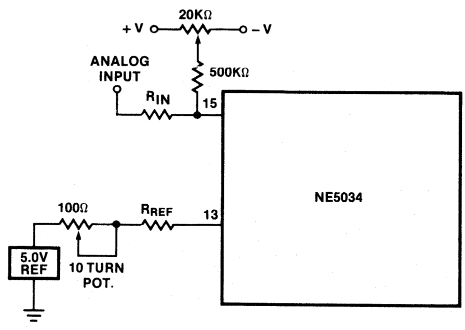


FIGURE 6. SUGGESTED ZERO/FULL SCALE ADJUST CIRCUIT

UNIPOLAR BINARY OPERATION:

A standard connection for a 0 to 10V unipolar binary operation, with $V_{REF\ IN}$ equal to +5 volts, is shown in Figure 4. The NE5034 can quantize full scale ranges of 1V to 10V. It should be noted, however, that for smaller full scale ranges, the accuracy and speed will degrade.

The input voltage versus output code relationship for unipolar operation is shown in Table 1. The full scale range is 2 times $I_{REF\ IN}$.

Table 1. Unipolar—Binary

ANALOG INPUT	DIGITAL OUTPUT CODE
NOTES 1, 2, 3	MSB LSB
FS—1 LSB	1 1 1 1 1 1 1 1
FS—2 LSB	1 1 1 1 1 1 1 0
3/4 FS	1 1 0 0 0 0 0 0
1/2 FS + 1 LSB	1 0 0 0 0 0 0 1
1/2 FS	1 0 0 0 0 0 0 0
1/2 FS − 1 LSB	0 1 1 1 1 1 1 1
1/4 FS	0 1 0 0 0 0 0 0
1 LSB	0 0 0 0 0 0 0 1
0	0 0 0 0 0 0 0 0

Table 2. Bipolar—Offset Binary

ANALOG INPUT	DIGITAL OUTPUT CODE
NOTES 1, 3, 4	MSB LSB
+(FS − 1 LSB)	1 1 1 1 1 1 1 1
+(FS − 2 LSB)	1 1 1 1 1 1 1 0
+(1/2 FS)	1 1 0 0 0 0 0 0
+(1 LSB)	1 0 0 0 0 0 0 1
0	1 0 0 0 0 0 0 0
−(1 LSB)	0 1 1 1 1 1 1 1
−(1/2 FS)	0 1 0 0 0 0 0 0
−(FS − 1 LSB)	0 0 0 0 0 0 0 1
−FS	0 0 0 0 0 0 0 0

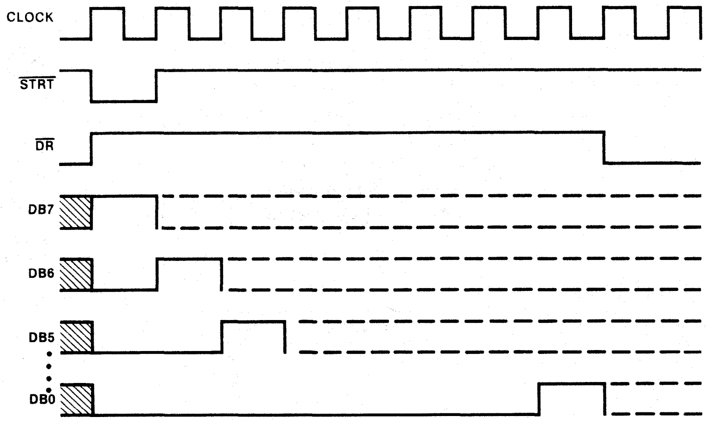
BIPOLAR (OFFSET BINARY) OPERATION:

A standard connection for a −5 to +5V or −10 to +10V bipolar operation is shown in Figure 5.

NOTES:

1. Analog inputs shown are nominal center values of code.
2. "FS" is full scale; i.e., $2I_{REF\ IN}$ (Unipolar mode).
3. 1 LSB equals (2^{-8}) (FS).
4. "FS" is full scale; i.e., $I_{REF\ IN}$ (Bipolar mode).

8-BIT GENERAL PURPOSE A/D CONVERTER NE5034



NOTE

1. $\overline{OE}$ = Logic "0"
2. See "Short-Cycle" section

FIGURE 7. NE5034 TIMING DIAGRAM

6-BIT A/D CONVERTER (SERIAL OUTPUT) NE5036

Preliminary

DESCRIPTION

The NE5036 is an easy to use, low cost, successive approximation Analog to Digital converter, fabricated in Bipolar/I^{2}L technology, and packaged in a convenient 8-pin mini dip package.

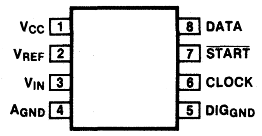
With an external reference voltage, the NE5036 will accept input voltages between 0V and V_{REF}. Holding the $\overline{\text{START}}$ pin low for at least 8 clock pulses in duration will provide the 6-bit result of the conversion in a serial format.

FEATURES

- **Three-state output buffer for easy μProcessor interfacing**
- **Fast successive approximation converter, 23μsec**
- **T^{2}L compatible inputs and outputs**
- **Easy interface to CMOS μProcessors**
- **Guaranteed no missing codes over full operating range**
- **Single supply operation, + 5V**
- **High impedance analog inputs**
- **Positive true binary serial output**

PIN CONFIGURATION

FE, N PACKAGE



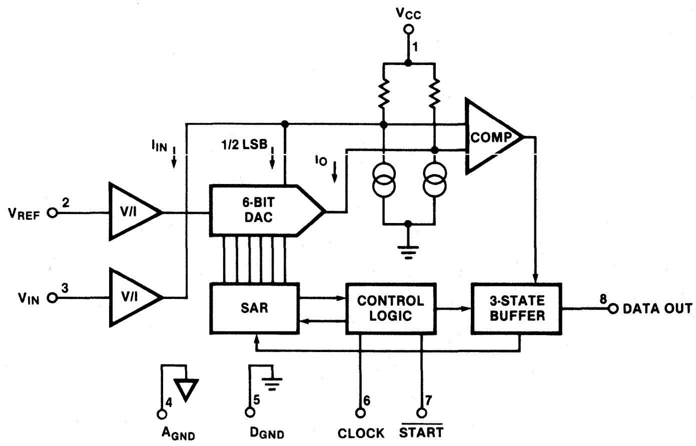
TOP VIEW

ORDER NUMBERS
NE5036FE, NE5036N

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power supply voltage	7	V
V_{REF}	Reference voltage	7	V
$V_{IN\,(Analog)}$	Analog input voltage	7	V
$V_{IN\,(Digital)}$	Digital input voltage ($\overline{\text{START}}$ & CLOCK)	7	V
D_{OUT}	Data output pin		
	Three-state mode	7	V
	Enabled mode	20	mA
Δ_{GND}	Analog GND to digital GND	± 1	V
T_A	Operating temperature range	0 to 70	°C
T_{Stg}	Storage temperature range	– 65 to 150	°C
t_{Sold}	Lead soldering temperature	300	°C
P_D	Power dissipation		
	FE package	220	mW
	N package	220	mW

BLOCK DIAGRAM



6-BIT A/D CONVERTER (SERIAL OUTPUT) NE5036

Preliminary

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 5.0V$; $V_{REF} = 2.0V$; Clock = 350kHz; $0°C \le T_A \le 70°C$ unless otherwise specified. Typical values are specified at 25°C.

SYMBOL AND PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution		6	6	6	Bits
Relative accuracy[1,2]			1/4	1/2	LSB
V_{CC} Positive supply voltage		+4.75	+5.0	+5.50	V
ϵ_{FS} Full scale gain error[2,3,4]	$V_{REF} = 2.0V$, $T_A = 25°C$		±1	±2	LSB
ϵ_{ZS} Zero scale offset error[2]	$V_{REF} = 2.0V$, $T_A = 25°C$		±1/2	−1/2, +2	LSB
P_{SR} Power supply rejection Max change in full scale[2]	$V_{REF} = 2.0V$ $4.75V \le V_{CC} \le 5.5V$		±1/2	±1	LSB
I_{IN} Analog input bias current	$0 \le V_{IN} \le 2.5V$		1	10	μA
I_{REF} Reference bias current	$0 \le V_{REF} \le 2.5V$		1	10	μA
R_{IN} Analog input resistance		3	30		MΩ
V_{IH} Logic '1' input voltage		2.0			V
V_{IL} Logic '0' input voltage				0.8	V
I_{IH} Logic '1' input current				10	μA
I_{IL} Logic '0' input current				10	μA
I_{OH} Logic '1' output current	$2.4V \le V_{OH}$	300			μA
I_{OL} Logic '0' output current	$V_{OL} \le 0.4V$	1.6			mA
I_{OZ} Three-state leakage current				±40	μA
I_{CC} Positive supply current			14	24	mA

AC ELECTRICAL CHARACTERISTICS

$V_{CC} = 5.0V$; $V_{REF} = 2.0V$; Clock = 350kHz; $0°C \le T_A \le 70°C$ unless otherwise specified. Typical values are specified at 25°C. (Refer to test figures.)

SYMBOL AND PARAMETER	TO	FROM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{MAX} Max clock frequency				350			kHz
T_{CONV} Conversion time						8	Clock cycles
t_W Clock pulse width				1.3			μs
t_S Setup time, $\overline{START}$ to clock[6]	Clock	$\overline{START}$		500			ns
$t_{P\,(OUT)}$ Propagation delay[5]	Data out	Clock	$T_A = 25°C$, $t_r = t_f < 20ns$			600	ns
$t_{P\,(3\text{-}STATE)}$ Propagation delay[5]	Data (3-State)	$\overline{START}$	$T_A = 25°C$, $t_r = t_f < 20ns$			600	ns

NOTES

1. Relative accuracy is defined as the deviation of the code transition points from the ideal code transition points on the straight line drawn from zero scale to full scale of the device.
2. Specifications given in LSB's refer to the weight of the least significant bit at the bit level which is 1.56% of the full scale voltage.
3. Full scale gain error is the deviation of the code transition point (111110 to 111111) from its ideal value (accounting for offset error at 000000).
4. The analog input voltage (V_{IN}) range is from 0V to V_{REF} nominally, with the output remaining at 111111 even though the input may increase from V_{REF} to V_{CC}. (For optimum performance V_{REF} can be any value from 1.5V to 2.5V.)
5. The time between the specified reference points on the clock and the output waveforms with the output changing (low to high or high to low).
6. The high to low transition of the $\overline{START}$ pulse should occur at least 500ns prior to the negative edge of the clock pulse to insure its recognition. The $\overline{START}$ pulse should stay high for at least 500ns between conversions to guarantee proper recognition.

6-BIT A/D CONVERTER (SERIAL OUTPUT) NE5036

Preliminary

CIRCUIT DESCRIPTION

NE5036 is a complete 6-bit, serial output, A/D converter which incorporates the successive approximation method. The chip includes the internal control logic, the successive approximation register (SAR), 6-bit DAC, comparator and the output buffer. An externally generated clock source (max freq = 350 kHz) must be provided to pin 6. An external reference voltage supplied to pin 2 sets the full scale range of the A/D converter as shown in the Block Diagram.

Upon the $\overline{\text{START}}$ pin going low, successive approximation conversion commences after the first low going edge of the clock pulse. Successive bits, beginning with the MSB (D5) are applied to the input of the internal 6-bit current output DAC by the I^2L successive approximation register.

The comparator determines whether the output current of the DAC is greater or less than the input current, converted from the unknown analog input voltage through the V/I converter. If the DAC output is greater, that bit of the DAC is set to 0 and simultaneously the output buffer goes to 0. If it is less that bit stays at 1 and the output buffer goes to 1. After the second high to low transition of the clock pulse, the MSB (D5) data is valid. On successive clock pulses, successive bits are tried and the output buffer represents that bit. $\overline{\text{START}}$ has to stay low for at least 8 clock pulses for the conversion to be completed and to access the 6-bit result of the conversion. A conversion in process can be interrupted by issuing another $\overline{\text{START}}$ pulse.

When $\overline{\text{START}}$ is in a high state, the output buffer is in a high impedance state.

The timing diagram for the device is shown in Figure 1.

TRANSFER CHARACTERISTICS

The NE5036 is designed to have a nominal 1/2 LSB offset, so that the code transition points are located 1/2 LSB on either side of the exact analog input for a given code. Thus the first transition (000000 to 000001) will occur at an input of 1/2 LSB (15.63mV with a V_{REF} of 2.0V), plus any offset. Subsequent transition (to full scale — 111111) will occur at 62.5 LSB (1.953V at V_{REF} of 2.0V).

The ideal transfer characteristic of NE5036 is shown in Figure 2.

LAYOUT PRECAUTIONS

Analog ground (pin 4) and Digital ground (pin 5) are not connected internally and should be connected together as close to the device as possible for optimum performance. The leads to the analog inputs should be kept as short as possible to minimize input noise pickup. Input bypass capacitors from the analog inputs to ground will eliminate noise pickup. Power supplies should be decoupled with at least $1\mu F$, located close to the device to minimize noise spikes on V_{CC}.

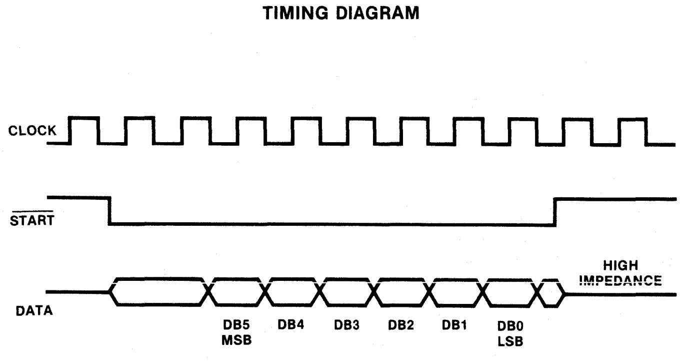


Figure 1

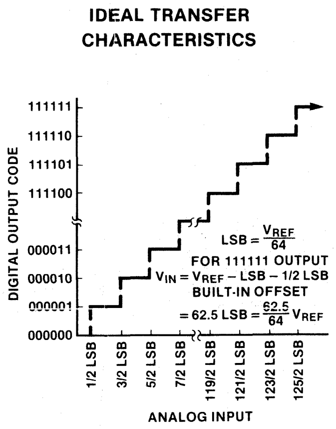


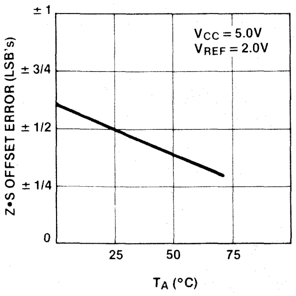
Figure 2

6-BIT A/D CONVERTER (SERIAL OUTPUT) NE5036

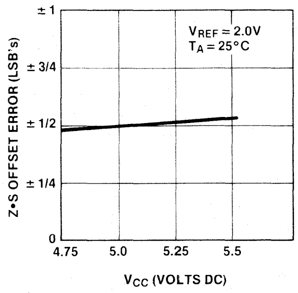
Preliminary

TYPICAL PERFORMANCE CHARACTERISTICS

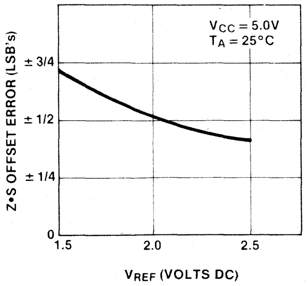
ZERO SCALE OFFSET ERROR vs TEMPERATURE



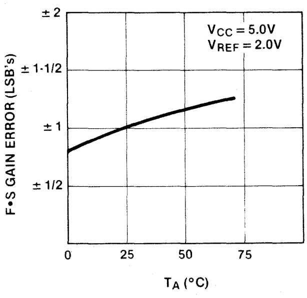
ZERO SCALE OFFSET ERROR vs V_{CC}



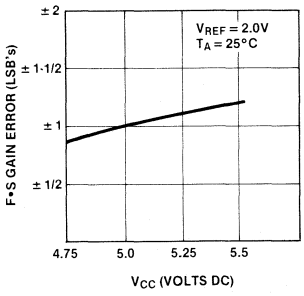
ZERO SCALE OFFSET ERROR vs V_{REF}



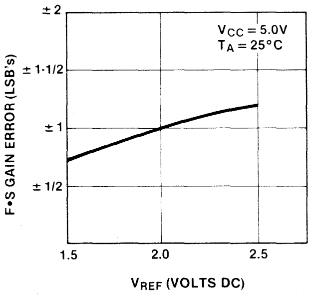
FULL SCALE GAIN ERROR vs TEMPERATURE



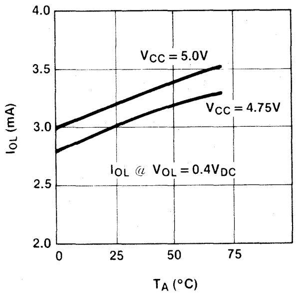
FULL SCALE GAIN ERROR vs V_{CC}



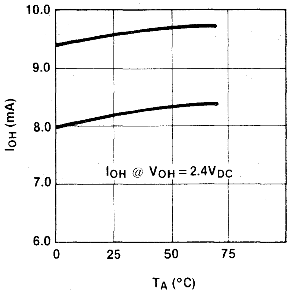
FULL SCALE GAIN ERROR vs R_{REF}



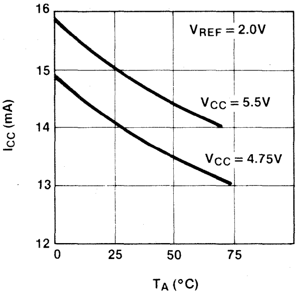
I_{OL} vs TEMPERATURE (DATA OUTPUT)



I_{OH} vs TEMPERATURE (DATA OUTPUT)



I_{CC} vs TEMPERATURE

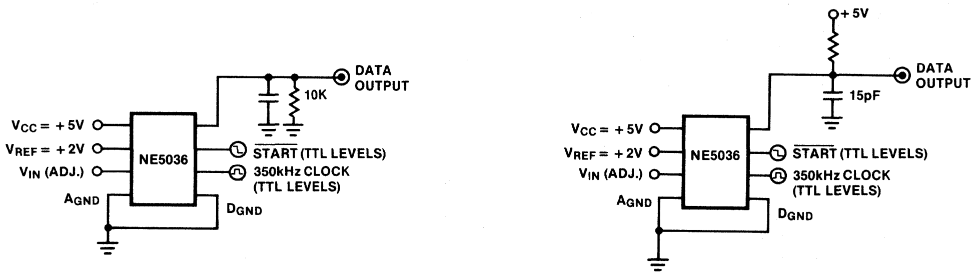


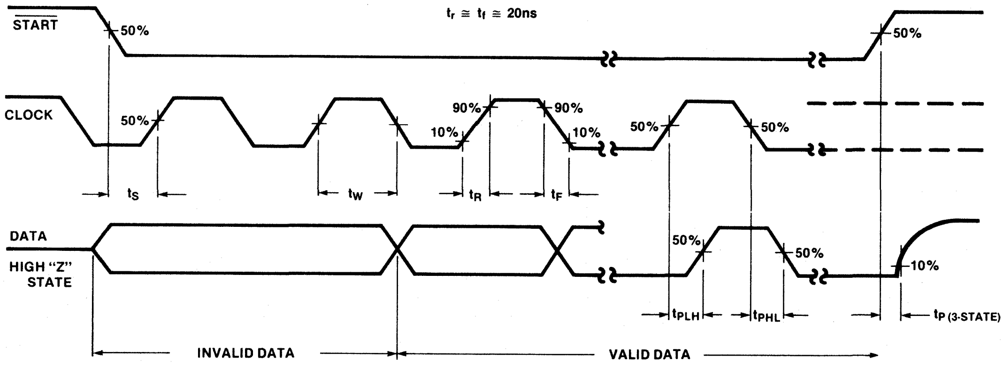
AC TEST CIRCUITS AND WAVEFORMS

PROPAGATION DELAY TIME $t_{p\,(DATA)}$

DATA OUTPUT (LOW TO HIGH)

DATA OUTPUT (HIGH TO LOW)





6-BIT A/D CONVERTER (PARALLEL OUTPUTS) NE5037

Preliminary

DESCRIPTION

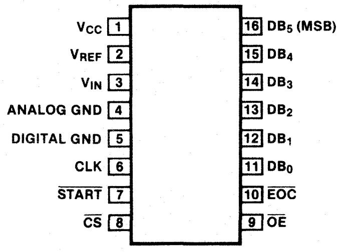
The NE5037 is a low cost, complete successive approximation analog to digital (A/D) converter, fabricated in Bipolar/I^2L technology. With an external reference voltage, the NE5037 will accept input voltages between 0V and V_{REF}. An external $\overline{START}$ pulse of at least 300ns in duration will provide the 6-bit result of the conversion in parallel format. Full conversion with no missing codes occurs in 9μs.

FEATURES

- **T^2L compatible inputs and outputs**
- **Three state output buffer**
- **Easy interface to CMOS μProcessors**
- **Fast conversion—9μs**
- **Guaranteed no missing codes over full temp range**
- **Single supply operation, +5V**
- **Positive true binary outputs**
- **High impedance analog inputs**

PIN CONFIGURATION

F, N PACKAGE



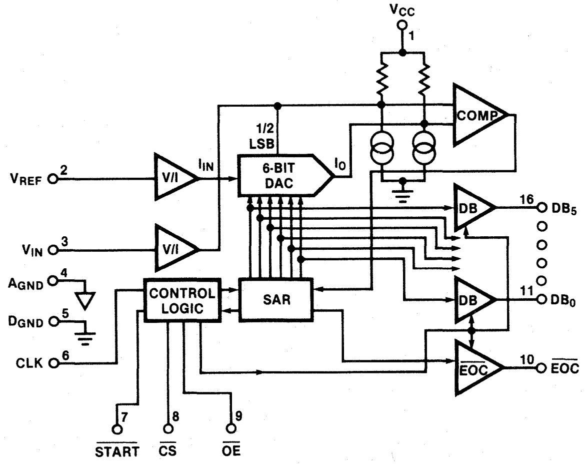
TOP VIEW

ORDER NUMBERS
NE5037F, NE5037N

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power supply voltage	7	V
V_{REF}	Reference voltage	7	V
$V_{IN\ (Analog)}$	Analog input voltage	7	V
$V_{IN\ (Digital)}$	Digital input voltage ($\overline{CS}$, $\overline{OE}$, $\overline{START}$, CLK)	7	V
D_{OUT}	Data outputs (DB0 to DB5)		
	Three-state mode	7	V
	Enabled mode (each output)	5	mA
$\overline{EOC}$	End of conversion	V_{CC}	
Δ_{GND}	Analog GND to digital GND	±1	V
T_A	Operating temperature range	0 to 70	°C
T_{STG}	Storage temperature range	−65 to 150	°C
t_{SOLD}	Lead soldering temperature (10 seconds)	300	°C
P_D	Power dissipation		
	F package	220	mW
	N package	220	mW

BLOCK DIAGRAM



6-BIT A/D CONVERTER (PARALLEL OUTPUTS) NE5037

Preliminary

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V; V_{REF} = 2.0V; Clock = 1MHz; 0°C ≤ T_A ≤ 70°C unless otherwise specified. Typical values are specified at 25°C.

SYMBOL AND PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution		6	6	6	Bits
	Relative accuracy[1,2]			1/4	1/2	LSB
V_{CC}	Positive supply voltage		+4.75	+5.0	+5.50	V
ϵ_{FS}	Full scale gain error[2,3,4]	$V_{REF}=2.0V$, $T_A=25°C$		±1	±2	LSB
ϵ_{ZS}	Zero scale offset error[2]	$V_{REF}=2.0V$, $T_A=25°C$		±1/2	−1/2, +2	LSB
P_{SR}	Power supply rejection Max change in full scale[2]	$V_{REF}=2.0V$ $4.75V \leq V_{CC} \leq 5.5V$		±1/2	±1	LSB
I_{IN}	Analog input bias current	$0 \leq V_{IN} \leq 2.5V$		1	10	μA
I_{REF}	Reference bias current	$0 \leq V_{REF} \leq 2.5V$		1	10	μA
R_{IN}	Analog input resistance		3	30		MΩ
V_{IH}	Logic '1' input voltage		2.0			V
V_{IL}	Logic '0' input voltage				0.8	V
I_{IH}	Logic '1' input current				10	μA
I_{IL}	Logic '0' input current				10	μA
I_{OH}	Logic '1' output current[5]	$2.4V \leq V_{OH}$	300			μA
I_{OL}	Logic '0' output current[5]	$V_{OL} \leq 0.4V$	1.6			mA
I_{OZ}	Three-state leakage current				±40	μA
I_{CC}	Positive supply current			18	24	mA

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V; V_{REF} = 2.0V; Clock = 1MHz; 0°C ≤ T_A ≤ 70°C unless otherwise specified. Typical values are specified at 25°C. (Refer to AC test figures.)

SYMBOL AND PARAMETER		TO	FROM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{MAX}	Maximum clock frequency				1			MHz
t_W	Start pulse width						300	ns
	Minimum positive/negative clock pulse width						300	ns
T_{CONV}	Conversion time						9	Clock cycles
$t_{P\ (OUT\ DATA)}$	Propagation delay[6]	Data out	$\overline{OE}$	$T_A=25°C$, $t_r=t_f \leq 20ns$			500	ns
$t_{P\ (OUT\ EOC)}$	Propagation delay[7]	$\overline{EOC}$	Clock	$T_A=25°C$, $t_r=t_f \leq 20ns$			800	ns
$t_{P\ (3\text{-}STATE)}$	Propagation delay, 3-state	3-State Data	$\overline{OE}$	$T_A=25°C$, $t_r=t_f \leq 20ns$			500	ns

NOTES

1. Relative accuracy is defined as the deviation of the code transition points from the ideal code transition points on a straight line drawn from zero scale to full scale of the device.
2. Specifications given in LSB's refer to the weight of the least significant bit at the 6 bit level which is 1.56% of the full scale voltage.
3. Full scale gain error is the deviation of the full scale code transition point (111110 to 111111) from its ideal value.
4. The analog input voltage (V_{IN}) range is 0V to V_{REF} nominally, with the output remaining at 111111 even though the input may increase from V_{REF} to V_{CC}. (For optimum performance, V_{REF} can be any value from 1.5V to 2.5V.)
5. The data outputs have active pull-ups. The $\overline{EOC}$ line is open collector with a nominal 5kΩ internal pull-up resistor
6. Propagation delay of data outputs is defined as the delay in the data outputs reading their final value after the low going edge of $\overline{OE}$.
7. Propagation delay of $\overline{EOC}$ is defined as the delay in $\overline{EOC}$ going low, following the low going edge of the 9th clock pulse after the start pulse.

CIRCUIT DESCRIPTION

NE5037 is a complete 6-bit, parallel output, microprocessor compatible, A/D converter which incorporates the successive approximation method. The chip includes the internal control logic, the successive approximation register (SAR), 6-bit DAC, comparator and output buffers. An externally generated clock source (max frequency = 1MHz) must be provided to pin 6.

An external reference voltage supplied to pin 2 sets the full scale range of the A/D converter.

The $\overline{CS}$ pin must be at a low level prior to the start of the conversion process. Upon receipt of a $\overline{START}$ pulse the internal control logic resets the SAR. On the first low going edge of the clock pulse, successive approximation conversion commences. Successive bits beginning with the MSB (D5) are supplied to the input of the internal 6-bit current output DAC by the I²L successive approximation register.

The comparator determines whether the output current of the DAC is greater or less than the input current, converted from the unknown analog input voltage through the V/I converter. If the DAC output is greater, that bit of the DAC is set to '0' and simultaneously the corresponding output buffer goes to '0'. If it is less, that bit stays at '1' and the output buffer also stays at '1'. On successive clock pulses, successive bits of the DAC are tried and the corresponding output buffer represents the bits of the DAC. On the eighth low going edge of the clock pulse (after the receipt of the start pulse). The $\overline{\text{EOC}}$ pin goes low, thereby indicating that the conversion is complete. The output data is now valid. In order to access the result of the conversion, the $\overline{\text{OE}}$ pin must be set to a low level. $\overline{\text{EOC}}$ is reset to a high state when $\overline{\text{OE}}$ is low. When $\overline{\text{OE}}$ is in a '1' state, the output buffers are in a high impedance state.

Refer to Figure 1 for the timing diagram.

TRANSFER CHARACTERISTICS

The ideal transfer characteristic of the NE5037 is shown in Figure 2.

The NE5037 is designed to have a nominal ½ LSB offset so that the code transition points are located ½ LSB on either side of the exact analog inputs for a given code.

Thus the first transition (000000 to 000001) will occur at an input of ½ LSB (15.63mV with a V_{REF} of 2.0V). Subsequent transitions will occur at nominal increments of 1 LSB. The last transition (to full scale—111111) will occur at 62.5 LSB (1.953V at V_{REF} of 2.0V).

LAYOUT PRECAUTIONS

Analog ground (pin 4) and Digital ground (pin 5) are not connected internally and should be connected together as close to the device as possible, for optimum performance. The circuit will operate with as much as ±200mV between the two grounds but some degradation will occur. The leads to the analog inputs should be kept as short as possible to minimize noise pickup. Input bypass capacitors from the analog inputs to ground will eliminate noise pickup. Power supplies should be decoupled with at least 1μF located close to the device to minimize noise spikes.

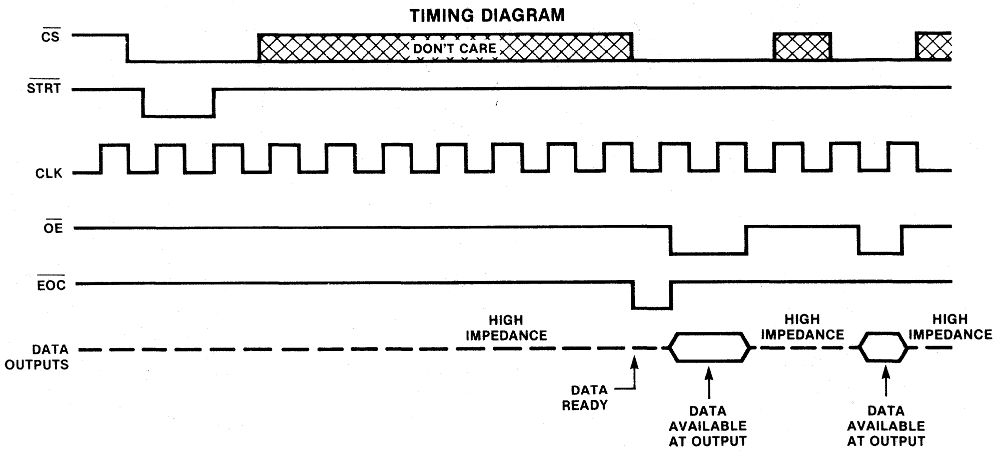


Figure 1

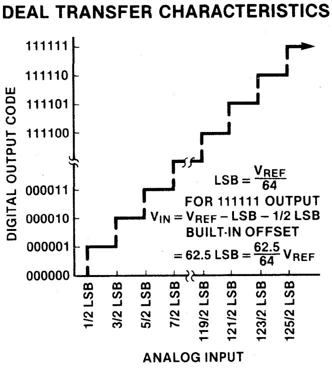
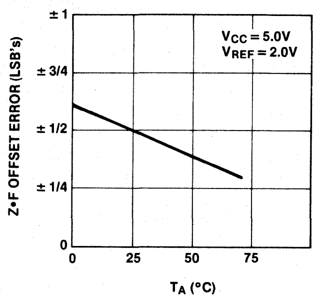
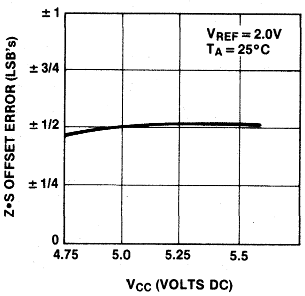


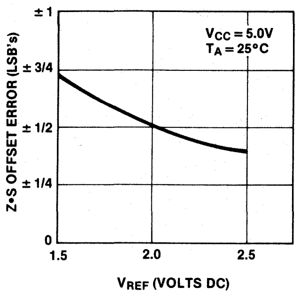
Figure 2

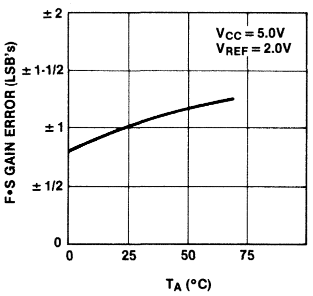
Preliminary

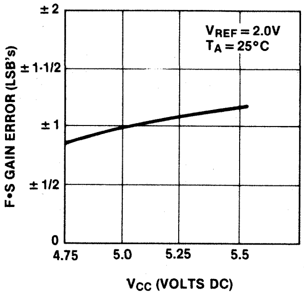
TYPICAL PERFORMANCE CHARACTERISTICS

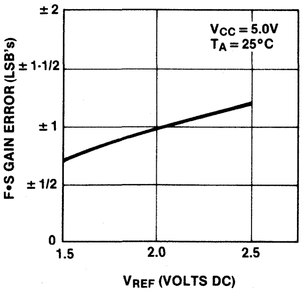

ZERO SCALE OFFSET ERROR vs TEMP

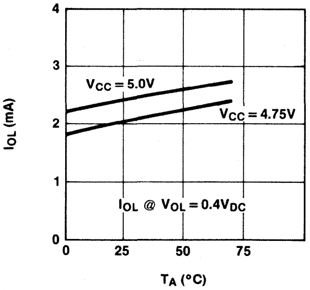

ZERO SCALE OFFSET ERROR vs V_{CC}

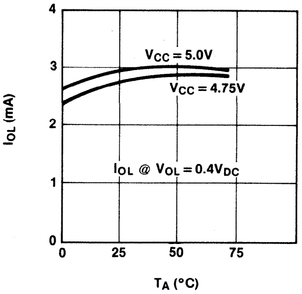

ZERO SCALE OFFSET ERROR vs V_{REF}

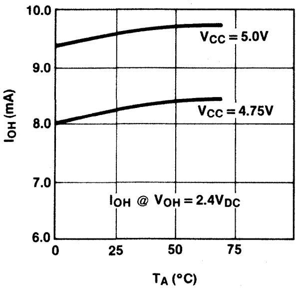

FULL SCALE GAIN ERROR vs TEMP

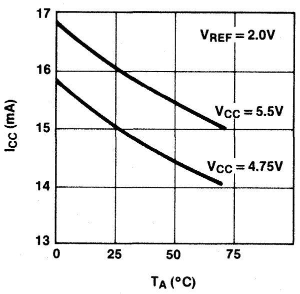

FULL SCALE GAIN ERROR vs V_{CC}

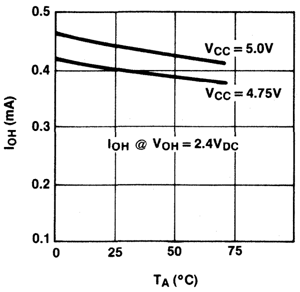

FULL SCALE GAIN ERROR vs V_{REF}


I_{OL} vs TEMP (DATA OUTPUTS)


I_{OL} vs TEMP ($\overline{EOC}$)


I_{OH} vs TEMP (DATA OUTPUTS)


I_{CC} vs TEMP

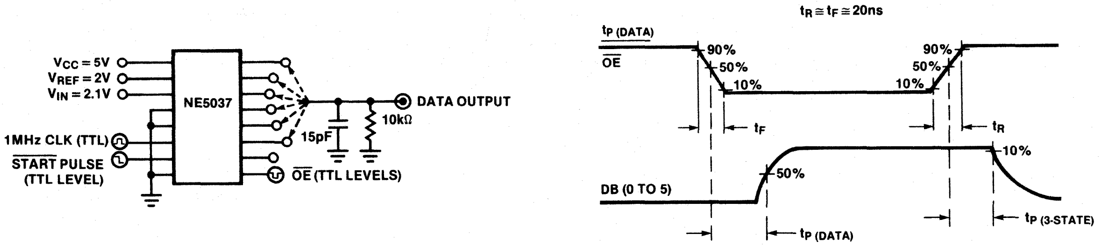

I_{OH} vs TEMP ($\overline{EOC}$)

6-BIT A/D CONVERTER (PARALLEL OUTPUTS) NE5037

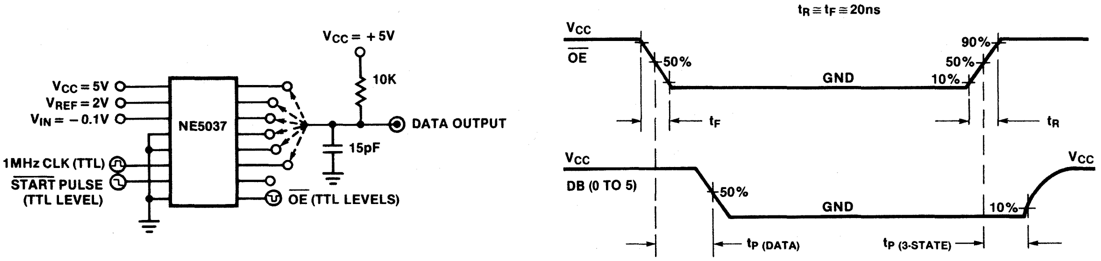
Preliminary

AC TEST CIRCUITS AND WAVEFORMS

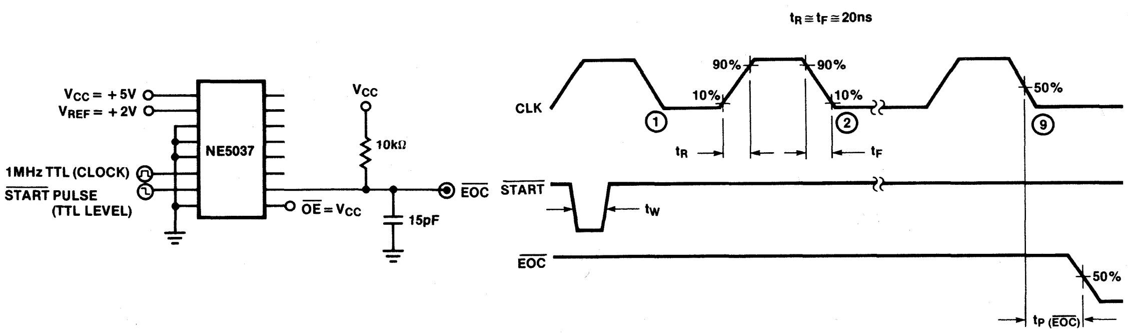
PROPAGATION DELAY TIME $t_{P\,(DATA)}$ AND $t_{P\,(3\text{-}STATE)}$



DATA OUTPUT HIGH



PROPAGATION DELAY TIME EOC $t_{P\,(EOC)}$



ANALOG DIVISION MARCH 1982

8-BIT μP-COMPATIBLE D/A CONVERTER—CURRENT OUTPUT NE/SE5118

DESCRIPTION

The NE5118 is a high-speed 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most microprocessors.

The chip also comprises a stable voltage reference (5V nominal). The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output has high voltage compliance increasing versatility.

FEATURES

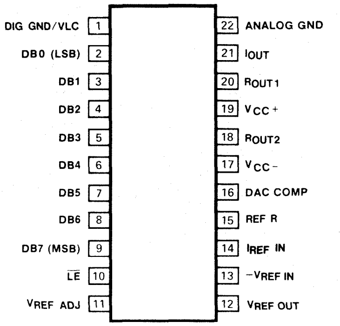
- **8-bit resolution**
- **Input latches**
- **Low-loading data inputs**
- **On-chip voltage reference**
- **Fast settling output current—200ns**
- **Accurate to ± 1/2 LSB (.19%)**
- **Monotonic to 8 bits**
- **Reference short-circuit protected**
- **Compatible with 8086, 6800 and many other μP's**

APPLICATIONS

- **Precision 8-bit D/A converters**
- **A/D converters**
- **Programmable power supplies**
- **Test equipment**
- **Measuring instruments**
- **Analog-digital multiplication**
- **CRT display drivers**
- **High-speed modems**

PIN CONFIGURATION

F,N PACKAGE



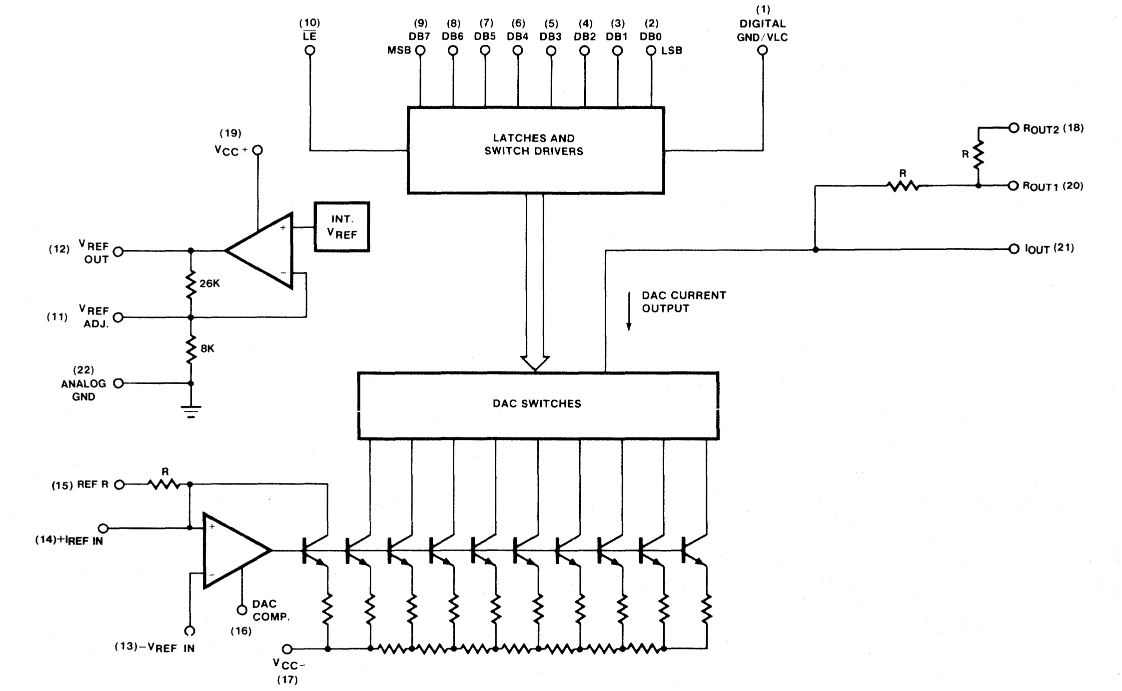
TOP VIEW

ORDER NUMBERS

NE5118F SE5118F

NE5118N

BLOCK DIAGRAM



All R values equal 5kΩ and are thermally matched.

Figure 1

8-BIT μP-COMPATIBLE D/A CONVERTER—CURRENT OUTPUT

NE/SE5118

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	−18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF}IN$	Voltage at R_{REF} input	12	V
$V_{REF}ADJ$	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at V_{REF} OUT	Continuous	
I_{REFIN}	Reference input current (Pin 14)	3	mA
P_D	Power dissipation*		
	-N package	800	mW
	-F package	1000	mW
T_A	Operating temperature range		
	SE5118	−55 to +125	°C
	NE5118	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES

For N package, derate at 120°C/W above 35°C

For F package, derate at 75° C/W above 75°C

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5118. $-55°C \leq T_A \leq 125°C$, NE5118. $0°C \leq T_A \leq 70°C$ unless otherwise specified. Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	SE5118			NE5118			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Relative accuracy				±0.19			±0.19	%FS
$V_{CC}+$	Positive supply voltage		11.4	15		11.4	15		V
$V_{CC}-$	Negative supply voltage		−11.4	−15		−11.4	−15		V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1 = 0V	2.0			2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1 = 0V			0.8			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1 = 0V, $2V<V_{IN}<18V$		0.1	10		0.1	10	μA
$I_{IN(0)}$	Logic "0" input current	Pin 1 = 0V, $-5V<V_{IN}<0.8V$		−2.0	−10		−2.0	−10	μA
I_{FS}	Full scale output current	Unipolar operation $V_{REF\ IN} = 5.000V$, $T_A = 25°C$	1.90	1.992	2.10	1.90	1.992	2.10	mA
I_{ZS}	Zero scale current		-6	1	+6	-6	1	+6	μA
V_{REF}	Reference voltage	I_{REF} = 1mA T_A = 25°C	4.9	5.0	5.25	4.9	5.0	5.25	V
$PSR+(out)$	Output power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, external $V_{REF\ IN}$ = 5.000V		.001	.01		.001	.01	%FS/ %VS
$PSR-(out)$	Output power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq -16.5V$. external $V_{REF\ IN}$ = 5.000V		.001	.01		.001	.01	%FS/ %VS
TC_{FS}	Full scale temperature coefficient	V_{REFIN} = 5.000V[1]		20			20		ppm/°C
TC_{ZS}	Zero scale temperature coefficient	I_{REFIN} = 1.00mA[2]		5			5		ppm/°C

NOTES

1. This is for voltage out only. See Unipolar Voltage Output schematic.
2. This is for current output mode.

DC ELECTRICAL CHARACTERISTICS

(Cont'd) $V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5118. $-55°C \leq T_A \leq 125°C$, NE5118. $0°C \leq T_A \leq 70°C$ unless otherwise specified. Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	SE5118			NE5118			UNIT
			Min	Typ	Max	Min	Typ	Max	
I_{REF}	Reference output current	Note 1			3			3	mA
I_{REFSC}	Reference short circuit current	$T_A = 25°C$ $V_{REF\ OUT} = 0V$		15	30		15	30	mA
$PSR+_{(REF)}$	Reference power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, $I_{REF} = 1.0mA$		.003	.01		.003	.01	%VR/%VS
$PSR-_{(REF)}$	Reference power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq 16.5V$, $I_{REF} = 1.0mA$		.003	.01		.003	.01	%VR/%VS
TC_{REF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$		60			60		ppm/°C
Z_{IN}	DAC $R_{REF}IN$ input impedance			5.0			5.0		kΩ
$I_{CC}+$	Positive supply current	$V_{CC}+ = 15V$		7	14		7	14	mA
$I_{CC}-$	Negative supply current	$V_{CC}- = -15V$		−10	−15		−10	−15	mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$		255	435		255	435	mW

AC ELECTRICAL CHARACTERISTICS

$V_{CC} = \pm 15V$, $T_A = 25°C$

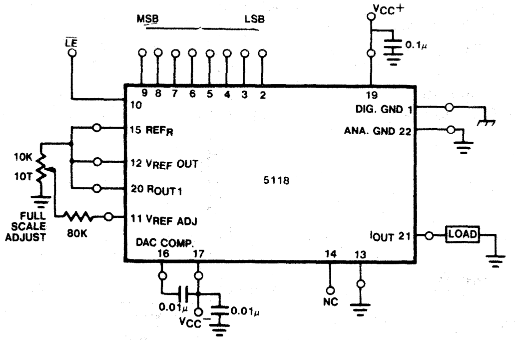
PARAMETER		TO	FROM	TEST CONDITIONS	SE/NE5118			UNIT
					Min	Typ	Max	
T_{SLH}	Settling time	± ½ LSB	Input	All bits Low-to-high		200		ns
T_{SHL}	Settling time	± ½ LSB	Input	All bits High-to-low		200		ns
t_{PLH}	Propagation delay	Output	Input	All bits switched Low-to-high		60		ns
t_{PHL}	Propagation delay	Output	Input	All bits switched High-to-low		60		ns
t_{PLSB}	Propagation delay	Output	Input	1 LSB change		60		ns
t_{PLH}	Propagation delay	Output	$\overline{LE}$	Low-to-high transition		60		ns
t_{PHL}	Propagation delay	Output	$\overline{LE}$	High-to-low transition		60		ns
t_s	Set-up time	$\overline{LE}$	Input		100			ns
t_h	Hold time	Input	$\overline{LE}$		50			ns
t_{pw}	Latch enable pulse width				150			ns

NOTES

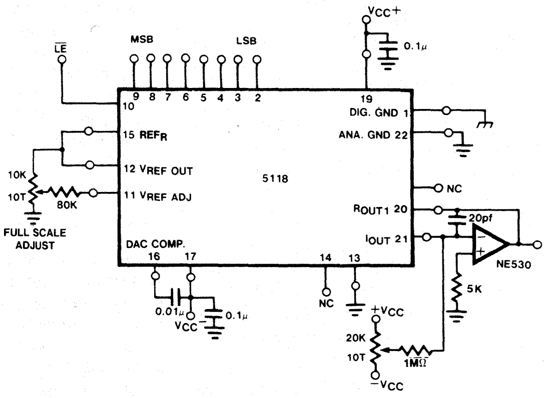
1. For reference currents > 3mA, use of an external buffer is required.

8-BIT µP-COMPATIBLE D/A CONVERTER—CURRENT OUTPUT NE/SE5118

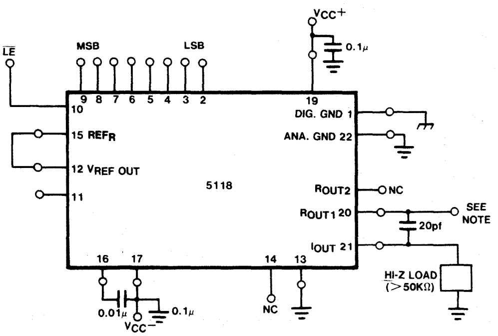
BIPOLAR OUTPUT OPERATION (−1mA TO +1mA)



UNIPOLAR VOLTAGE OUTPUT (0 →+10V)



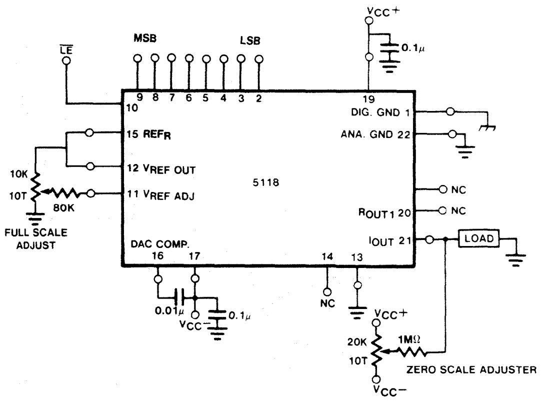
FAST VOLTAGE OUTPUT



NOTE

DATA INPUT CODE	VOLTAGE OUTPUT (PIN 21)	
0 0 0 0 0 0 0 0	+10V	0V
1 1 1 1 1 1 1 1	0V	−10V
	Pin 20 tied to +10V	Pin 20 tied to 0V

BASIC UNIPOLAR CURRENT OUTPUT (0 →−2mA)



8-BIT μP-COMPATIBLE D/A CONVERTER—CURRENT OUTPUT NE/SE5119

DESCRIPTION

The NE5119 is a high-speed 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most microprocessors.

The chip also comprises a stable voltage reference (5V nominal). The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output has high voltage compliance increasing versatility.

FEATURES

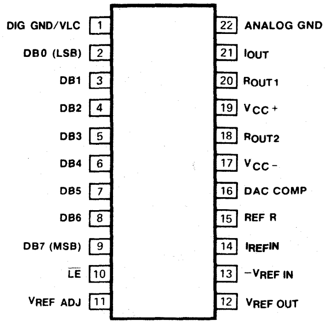
- **8-bit resolution**
- **Input latches**
- **Low-loading data inputs**
- **On-chip voltage reference**
- **Fast settling output current—200ns**
- **Accurate to ± 1/4 LSB (.1%)**
- **Monotonic to 8 bits**
- **Reference short-circuit protected**
- **Compatible with 8086, 6800 and many other μP's**

APPLICATIONS

- **Precision 8-bit D/A converters**
- **A/D converters**
- **Programmable power supplies**
- **Test equipment**
- **Measuring instruments**
- **Analog-digital multiplication**
- **CRT display drivers**
- **High-speed modems**

PIN CONFIGURATION

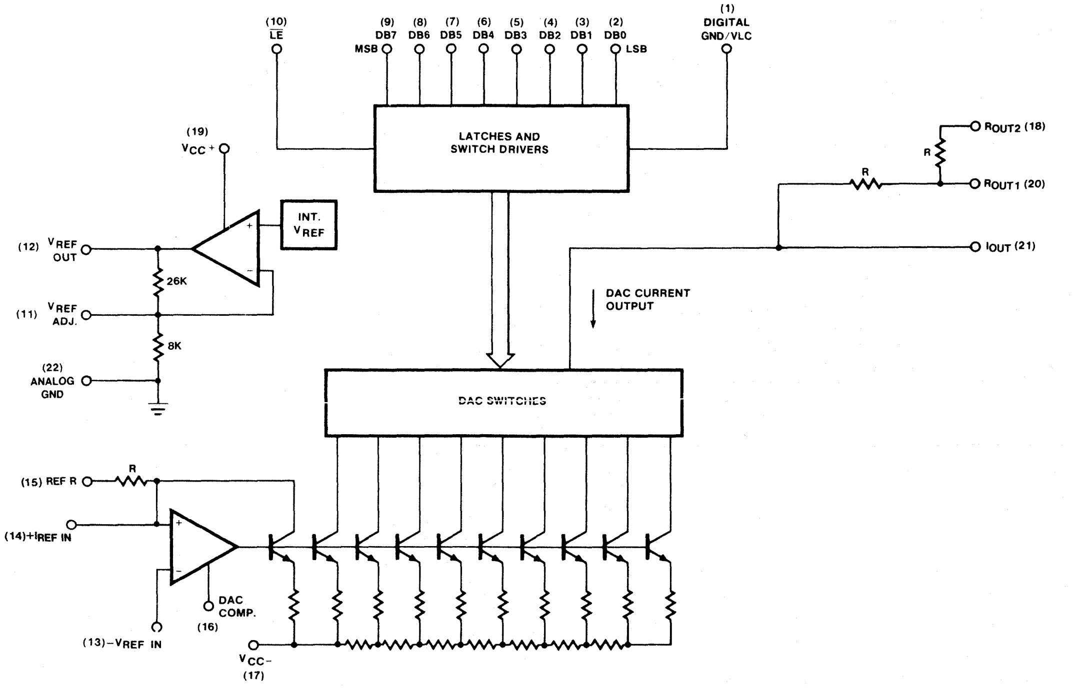
F,N PACKAGE



TOP VIEW

ORDER NUMBERS
NE5119F SE5119F
NE5119N

BLOCK DIAGRAM



All R values equal 5kΩ and are thermally matched.

Figure 1

8-BIT µP-COMPATIBLE D/A CONVERTER—CURRENT OUTPUT NE/SE5119

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	−18	V
V_{IN}	Logic input voltage	0 to 18	V
V_{REF}^{IN}	Voltage at R_{REF} input	12	V
V_{REF}^{ADJ}	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at V_{REF} OUT	Continuous	
$I_{REF_{IN}}$	**Reference input current (Pin 14)**	3	mA
P_D	**Power dissipation***		
	-N package	800	mW
	-F package	1000	mW
T_A	Operating temperature range		
	SE5119	−55 to +125	°C
	NE5119	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES

For N package, derate at 120°C/W above 35°C

For F package, derate at 75° C/W above 75°C

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5119. $-55°C \leq T_A \leq 125°C$, NE5119. $0°C \leq T_A \leq 70°C$ unless otherwise specified. Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	SE5119			NE5119			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Relative accuracy				±0.1			±0.1	%FS
$V_{CC}+$	Positive supply voltage		11.4	15		11.4	15		V
$V_{CC}-$	Negative supply voltage		−11.4	−15		−11.4	−15		V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1 = 0V	2.0			2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1 = 0V			0.8			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1 = 0V, $2V<V_{IN}<18V$		0.1	10		0.1	10	µA
$I_{IN(0)}$	Logic "0" input current	Pin 1 = 0V, $-5V<V_{IN}<0.8V$		−2.0	−10		−2.0	−10	µA
I_{FS}	Full scale output current	Unipolar operation $V_{REF\ IN} = 5.000V$, $T_A = 25°C$	1.90	1.992	2.10	1.90	1.992	2.10	mA
I_{ZS}	Zero scale current			1			1		µA
V_{REF}	Reference voltage	$I_{REF} = 1mA$ $T_A = 25°C$	4.9	5.0	5.25	4.9	5.0	5.25	V
PSR+(out)	Output power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01		.001	.01	%FS/%VS
PSR−(out)	Output power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq -16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01		.001	.01	%FS/%VS
TC_{FS}	Full scale temperature coefficient	$V_{REF_{IN}} = 5.000V$[1]		20			20		ppm/°C
TC_{ZS}	Zero scale temperature coefficient	$I_{REF_{IN}} = 1.00mA$[2]		5			5		ppm/°C

NOTES

1. This is for voltage out only. See Unipolar Voltage Output schematic
2. This is for current output mode

DC ELECTRICAL CHARACTERISTICS

(Cont'd) $V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5119. $-55°C \leq T_A \leq 125°C$,
NE5119. $0°C \leq T_A \leq 70°C$ unless otherwise specified.
Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	SE5119			NE5119			UNIT
			Min	Typ	Max	Min	Typ	Max	
I_{REF}	Reference output current	Note 1			3			3	mA
I_{REFSC}	Reference short circuit current	$T_A = 25°C$ $V_{REF\ OUT} = 0V$		15	30		15	30	mA
$PSR+_{(REF)}$	Reference power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, $I_{REF} = 1.0mA$		.003	.01		.003	.01	%VR/%VS
$PSR-_{(REF)}$	Reference power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq 16.5V$, $I_{REF} = 1.0mA$		.003	.01		.003	.01	%VR/%VS
TC_{REF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$		60			60		ppm/°C
Z_{IN}	DAC $R_{REF}IN$ input impedance			5.0			5.0		kΩ
$I_{CC}+$	Positive supply current	$V_{CC}+ = 15V$		7	14		7	14	mA
$I_{CC}-$	Negative supply current	$V_{CC}- = -15V$		−10	−15		−10	−15	mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$		255	435		255	435	mW

AC ELECTRICAL CHARACTERISTICS

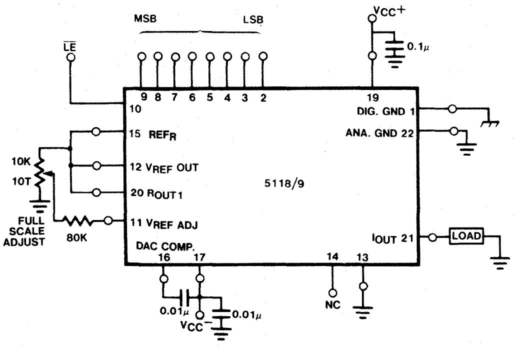
$V_{CC} = \pm 15V$, $T_A = 25°C$

PARAMETER		TO	FROM	TEST CONDITIONS	SE/NE5119			UNIT
					Min	Typ	Max	
T_{SLH}	Settling time	± ½ LSB	Input	All bits Low-to-high		200		ns
T_{SHL}	Settling time	± ½ LSB	Input	All bits High-to-low		200		ns
t_{PLH}	Propagation delay	Output	Input	All bits switched Low-to-high		60		ns
t_{PHL}	Propagation delay	Output	Input	All bits switched High-to-low		60		ns
t_{PLSB}	Propagation delay	Output	Input	1 LSB change		60		ns
t_{PLH}	Propagation delay	Output	$\overline{LE}$	Low-to-high transition		60		ns
t_{PHL}	Propagation delay	Output	$\overline{LE}$	High-to-low transition		60		ns
t_s	Set-up time	$\overline{LE}$	Input		100			ns
t_h	Hold time	Input	$\overline{LE}$		50			ns
t_{pw}	Latch enable pulse width				150			ns

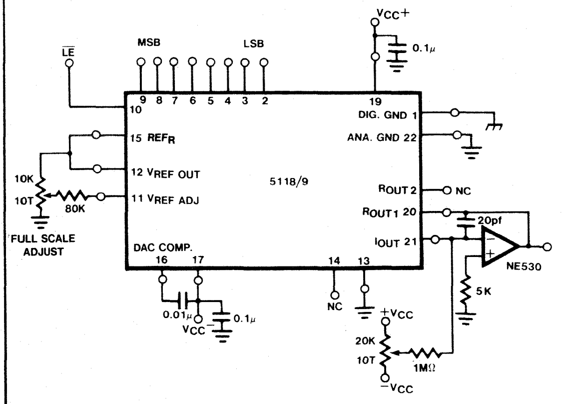
NOTES

1. For reference currents > 3mA, use of an external buffer is required.

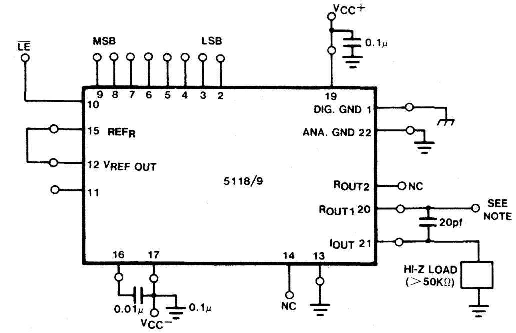
BIPOLAR OUTPUT OPERATION (−1mA TO +1mA)



UNIPOLAR VOLTAGE OUTPUT (0 → +10V)



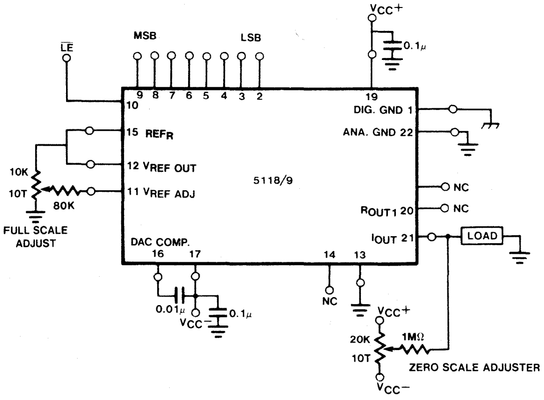
FAST VOLTAGE OUTPUT



NOTE

DATA INPUT CODE	VOLTAGE OUTPUT (PIN 21)	
0 0 0 0 0 0 0 0	+10V	0V
1 1 1 1 1 1 1 1	0V	−10V
	Pin 20 tied to +10V	Pin 20 tied to 0V

BASIC UNIPOLAR CURRENT OUTPUT (0 → −2mA)



Section 12
Sample and Hold Circuits

INDEX

Section 12 — Sample and Hold Circuits

SAMPLE AND HOLD CIRCUITS—SYMBOLS AND DEFINITIONS

Acquisition Time

The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

Aperture Delay Time

The time elapsed from the hold command to the opening of the switch.

Aperture Jitter

Also called "aperture uncertainty time", it's the time variation or uncertainty with which the switch opens, or the time variation in aperture delay.

Aperture Time

The delay required between "hold" command and an input analog transition, so that the transition does not affect the hold output.

Effective Aperture Delay

The time difference between the hold command and the time at which the input signal is at the held voltage.

Figure Of Merit

The ratio of the available charging current during sample mode to the leakage current during hold mode.

Hold-Mode Droop

The output voltage change per unit of time while in hold. Commonly specified in V/s, μV/μs or other convenient units.

Hold-Mode Feed Through

The percentage of an input sinusoidal signal that is measured at the output of a sample-hold when it's in hold mode.

Hold Settling Time

The time required for the output to settle within 1mV of final value after the "hold" logic command.

Sample-To-Hold Offset Error

The difference in output voltage between the time the switch starts to open, and the time when the output has settled completely. It is caused by charge being transferred to the hold capacitor switch as it opens.

Slew Rate

The fastest rate at which the sample & hold output can change (specified in V/μs).

Hold Step

The voltage step at the output of the sample and hold when switching from sample mode to hold mode with a steady (dc) analog input voltage. Logic swing is 5V.

Dynamic Sampling Error

The error introduced into the held output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

Gain Error

The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

Threshold

Level shall be defined as that level which causes the switch control to change state.

MONOLITHIC SAMPLE AND HOLD CIRCUIT LF398

DESCRIPTION

The Signetics LF398 is a monolithic sample and hold circuit which utilizes high-voltage Ion-Inplant JFET technology to obtain ultra-high dc accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, dc gain accuracy is 0.004% typical and acquisition time is as low as 6μs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin and does not degrade input offset drift. The wide bandwidth allows the LF398 to be included inside the feedback loop of 1MHz op amps without having stability problems. Input impedance of $10^{10}\Omega$ allows high source impedances to be used without degrading accuracy.

P-channel junction FET's are combined with bipolar devices in the output amplifier to give droop rates as low as 5mV/min with a 1μF hold capacitor. The JFET's have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feed-through from input to output in the hold mode even for input signals equal to the supply voltages.

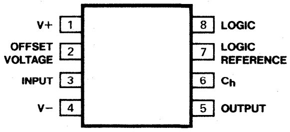
Logic inputs on the LF398 are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS. Differential threshold is 1.4V. The LF398 will operate from ±5V to ±18V supplies. It is available in an 8-lead TO-5 package or an 8-pin plastic DIP.

FEATURES

- **Operates from ±5V to ±18V supplies**
- **Less than 10μs acquisition time**
- **TTL, PMOS, CMOS compatible logic input**
- **0.5mV typical hold step at $C_h = 0.01\mu F$**
- **Low input offset**
- **0.002% gain accuracy**
- **Low output noise in hold mode**
- **Input characteristics do not change**
  - **during hold mode**
- **High supply rejection ratio in sample or hold**
- **Wide bandwidth**
- **The LF398 is ideally suited for a wide variety of sample and hold applications including data acquisition, analog to digital conversion, synchronous demodulation, and automatic test setup.**

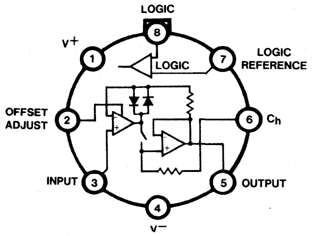
PIN CONFIGURATION

N PACKAGE



TOP VIEW
ORDER NUMBERS
LF398N

H PACKAGE

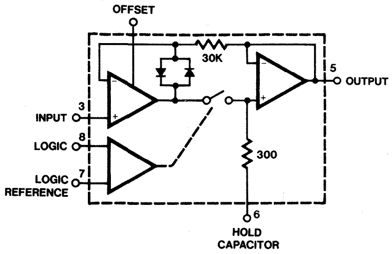


TOP VIEW
ORDER NUMBERS
LF398H

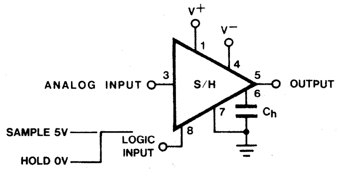
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	±18	V
Power dissipation (package limitation)[1]	500	mW
Operating ambient temperature range		
LF398	0 to +70	°C
Storage temperature range	−65 to +150	°C
Input voltage	Equal to supply voltage	
Logic to logic reference differential voltage[2]	+7, −30	V
Output short circuit duration	Indefinite	
Hold capacitor short circuit duration	10	sec
Lead temperature (soldering, 10sec)	300	°C

FUNCTIONAL DIAGRAM



TYPICAL APPLICATIONS



MONOLITHIC SAMPLE AND HOLD CIRCUIT LF398

DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, $V_S = \pm 15V$, $T_j = 25°C$, $-11.5V \leq V_{IN} \leq +11.5V$, $C_h = 0.01\mu F$, and $R_L = 10k\Omega$. Logic reference voltage = OV and logic voltage = 2.5V.

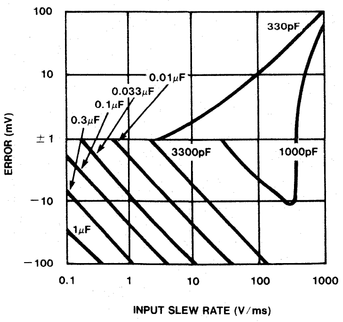
PARAMETER	TEST CONDITIONS	LF398			UNIT
		Min	Typ	Max	
Input offset voltage[6]	$T_j = 25°C$ Full temperature range		2	7 10	mV mV
Input bias current[6]	$T_j = 25°C$ Full temperature range		10	50 100	nA nA
Input impedance	$T_j = 25°C$		10^{10}		Ω
Gain error	$T_j = 25°C$, $R_L = 10K$ Full temperature range		0.004	0.01 0.02	% %
Feedthrough attenuation ratio at 1kHz	$T_j = 25°C$, $C_h = 0.01\mu F$	80	90		dB
Output impedance	$T_j = 25°C$, "HOLD" mode Full temperature range		0.5	4 6	Ω Ω
"HOLD" step[4] Supply current[6]	$T_j = 25°C$, $C_h = 0.01\mu F$, $V_{OUT} = 0$ $T_j \geq 25°C$		1.0 4.5	2.5 6.5	mV mA
Logic and logic reference input current	$T_j = 25°C$		2	10	μA
Leakage current into hold capacitor[6]	$T_j = 25°C$[5] Hold mode		30	200	pA
Acquisition time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000pF$ $C_h = 0.01\mu F$		4 20		μs μs
Hold capacitor charging current	$V_{IN}-V_{OUT} = 2V$		5		mA
Supply voltage rejection ratio	$V_{OUT} = 0$	80	110		dB
Differential logic threshold	$T_j = 25°C$	0.8	1.4	2.4	V

NOTES

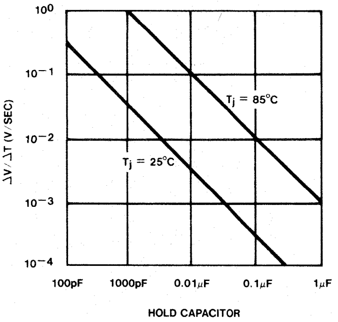
1. The maximum junction temperature of the LF398 is 150°C. When operating at elevated ambient temperature, the TO-5 and plastic DIP packages must be derated based on a thermal resistance (θjA) of 150°C/W.
2. Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.
3. Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, $V_S = \pm 15V$, $T_j = 25°C$, $-11.5V \leq V_{IN} \leq +11.5V$, $C_h = 0.01\mu F$, and $R_L = 10k$. Logic reference voltage = OV and logic voltage = 2.5V.
4. Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01μF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.
5. Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.
6. The parameters guaranteed over a supply voltage of ±5 to ±18V.

TYPICAL AC PERFORMANCE CHARACTERISTICS (cont'd)

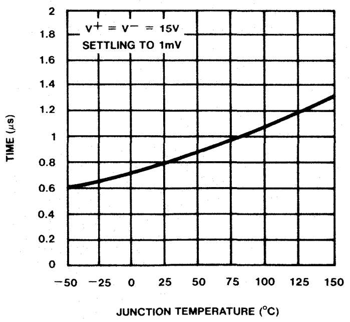
DYNAMIC SAMPLING ERROR



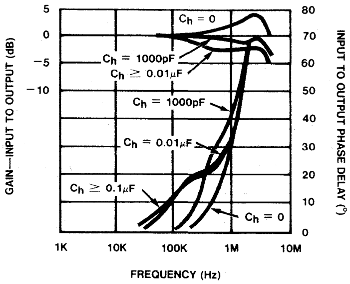
OUTPUT DROOP RATE



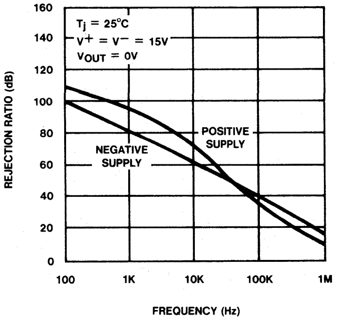
"HOLD" SETTLING TIME



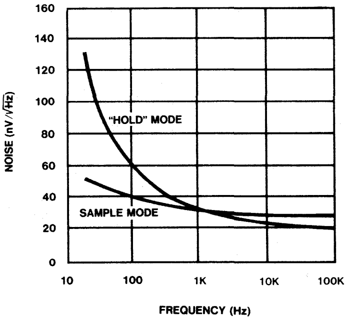
PHASE AND GAIN
(INPUT TO OUTPUT, SMALL SIGNAL)



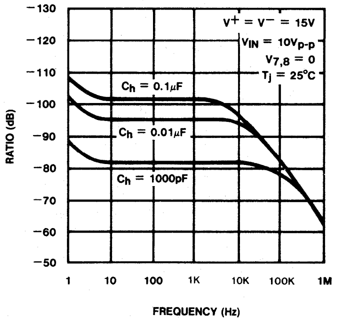
POWER SUPPLY REJECTION



OUTPUT NOISE



FEEDTHROUGH REJECTION RATIO
(HOLD MODE)

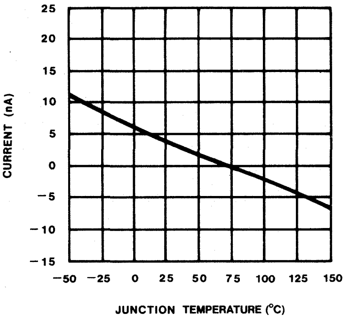


MONOLITHIC SAMPLE AND HOLD CIRCUIT

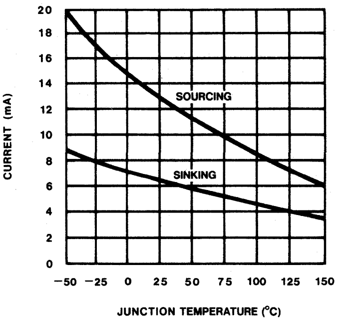
LF398

TYPICAL DC PERFORMANCE CHARACTERISTICS

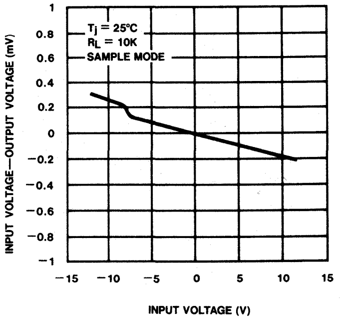
INPUT BIAS CURRENT



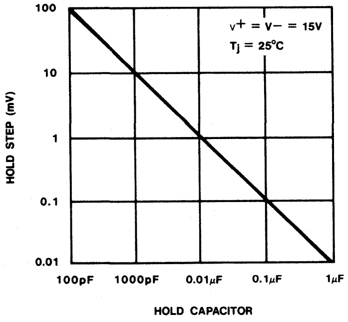
OUTPUT SHORT CIRCUIT CURRENT



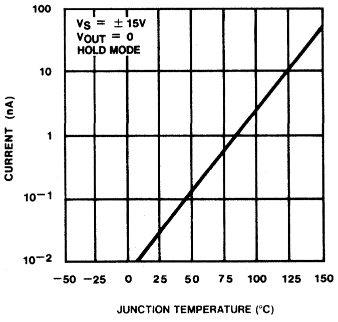
GAIN ERROR



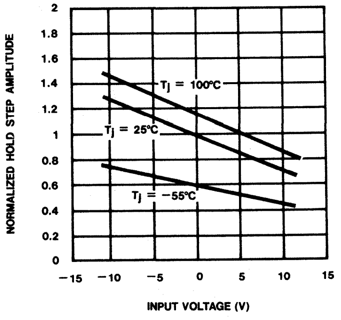
HOLD STEP



LEAKAGE CURRENT INTO HOLD CAPACITOR

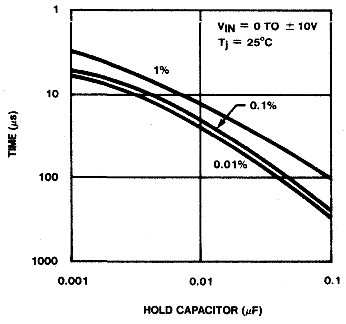


HOLD STEP INPUT VOLTAGE

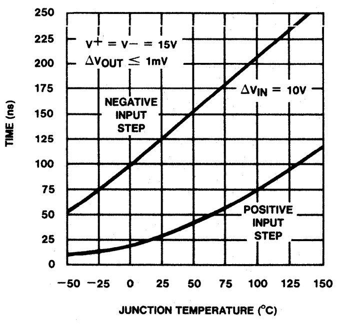


TYPICAL AC PERFORMANCE CHARACTERISTICS

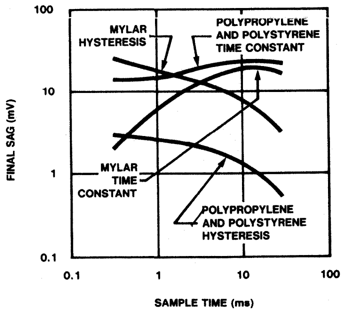
ACQUISITION TIME



APERTURE TIME



CAPACITOR HYSTERESIS



SAMPLE AND HOLD AMPLIFIER NE/SE5537

DESCRIPTION

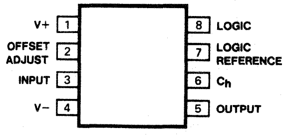
The NE5537 monolithic Sample and Hold amplifier combines the best features of ion implanted JFET's with bipolar devices to obtain high accuracy, fast acquisition time, and low droop rate. This device is pin compatible with the LF198, and features superior performance in droop rate and output drive capability. The circuit shown in Figure 1 contains two operational amplifiers which function as a unity gain amplifier in the Sample mode. The first amplifier has bipolar input transistors which gives the system a low offset voltage. The second amplifier has JFET input transistors to achieve low leakage current from the hold capacitor. A unique circuit design for leakage current cancellation using current mirrors gives the NE5537 a low droop rate at higher temperature. The output stage has the capability to drive a 2KΩ load. The logic input is compatible with TTL, PMOS or CMOS logic. The differential logic threshold is 1.4V with the Sample mode occurring when the logic input is high. It is available in 8-lead TO-5 and 8-pin plastic DIP packages.

FEATURES

- Operates from ±5V to ±18V supplies
- Hold leakage current 6pA @ T_j25°C
- Less than 10μs acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5mV typical hold step at $C_h = 0.01\mu F$
- Low input offset: 1MV (typical)
- 0.002% gain accuracy with $R_L = 2k\Omega$
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth

PIN CONFIGURATION

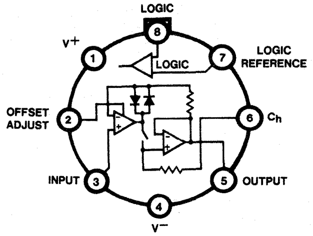
N PACKAGE



TOP VIEW

ORDER NUMBERS
NE/SE5537N

H PACKAGE
Metal Can Package



TOP VIEW

ORDER NUMBERS
NE/SE5537-H

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	±18	V
Power dissipation (package limitation)[1]	500	mW
Operating ambient temperature range		
SE5537	−55 to +125	°C
NE5537	0 to +70	°C
Storage temperature range	−65 to +150	°C
Input voltage	Equal to supply voltage	
Logic to logic reference differential voltage[2]	+7, −30	V
Output short circuit duration	Indefinite	
Hold capacitor short circuit duration	10	sec
Lead temperature (soldering, 10sec)	300	°C

NOTES

1. The maximum junction temperature of the SE5537 is 150°C and for the NE5537 is100°C. When operating at elevated ambient temperature, the TO-5 and plastic DIP packages must be derated based on a thermal resistance (θja) of 150°C/W.
2. Although the differential voltage may not exceed the limits given, the common mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

BLOCK DIAGRAM

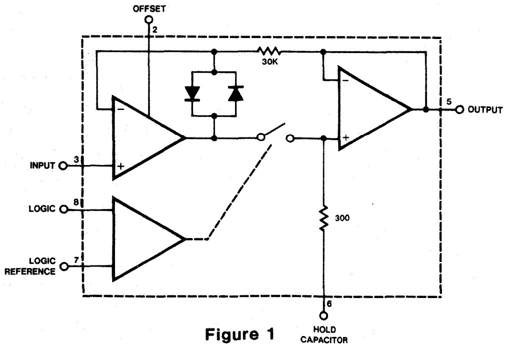


Figure 1

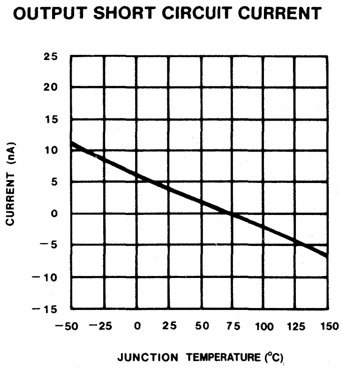
ELECTRICAL CHARACTERISTICS[3]

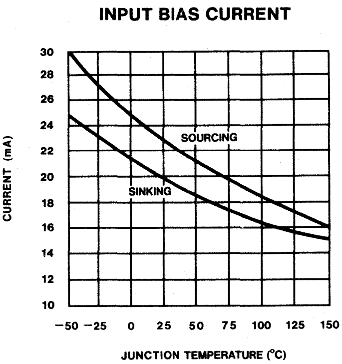
PARAMETER	TEST CONDITIONS	SE5537			NE5537			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage[6]	T_j = 25°C Full temperature range		1	3 5		2	7 10	mV mV
Input bias current[6]	T_j = 25°C Full temperature range		5	25 75		10	50 100	nA nA
Input impedance	T_j = 25°C		10^{10}			10^{10}		Ω
Gain error	T_j = 25°C, $-10V \leq V_{IN} \leq 10V$, R_L = 2K $-11.5V \leq V_{IN} \leq 11.5V$, R_L = 10K Full temperature range		0.002	0.007 0.02		0.004	0.01 0.02	% %
Feedthrough attenuation ratio at 1kHz	T_j = 25°C, C_h = 0.01µF	86	96		80	90		dB
Output impedance	T_j = 25°C, "HOLD" mode full temperature range		0.5	2 4		0.5	4 6	Ω
"HOLD" Step[4]	T_j = 25°C, C_h = 0.01µF, V_{OUT} = 0		0.5	2.0		1.0	2.5	mV
Supply current[6]	T_j=25°C		4.5	6.5		4.5	7.5	mA
Logic and logic reference input current	T_j = 25°C		2	10		2	10	µA
Leakage current into hold capacitor[6]	T_j = 25°C hold mode[5]		6	50		6	100	pA
Acquisition time to 0.1%	V_{OUT} = 10V, C_h = 1000pF C_h = 0.01µf		4 20			4 20		µs µs
Hold capacitor charging current	$V_{IN} - V_{OUT}$ = 2V		5			5		mA
Supply voltage rejection ratio	V_{OUT} = 0	80	110		80	110		dB
Differential logic threshold	T_j = 25°C	0.8	1.4	2.4	0.8	1.4	2.4	V

NOTES

3. Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, $V_S = \pm 15V$, T_j = 25°C, $-11.5V \leq V_{IN} \leq 11.5V$, C_h = 0.01µF, and R_L = 2kΩ. Logic reference voltage = 0V and logic voltage = 2.5V.
4. Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01F hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.
5. Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.
6. These parameters guaranteed over a supply voltage range of ±5 to ±18V.

TYPICAL PERFORMANCE CHARACTERISTICS

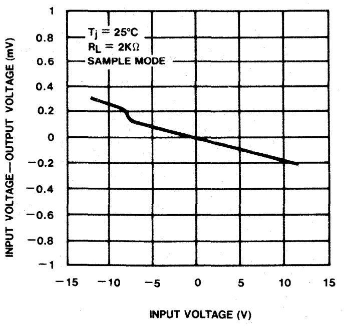

OUTPUT SHORT CIRCUIT CURRENT


INPUT BIAS CURRENT

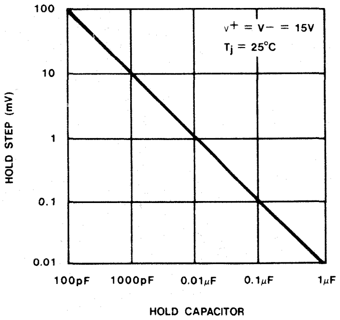
SAMPLE AND HOLD AMPLIFIER NE/SE5537

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

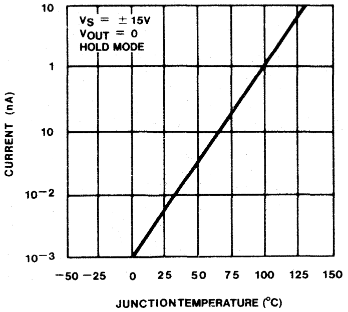
GAIN ERROR



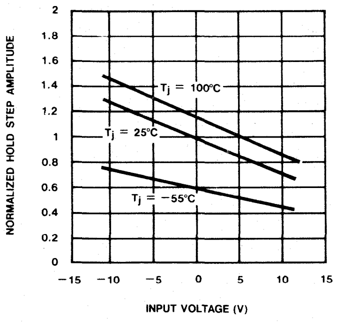
HOLD STEP



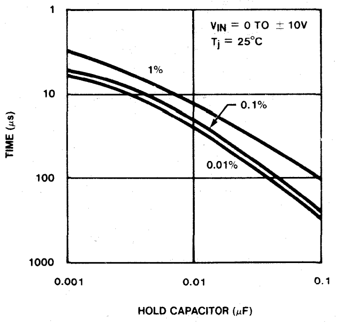
LEAKAGE CURRENT INTO HOLD CAPACITOR



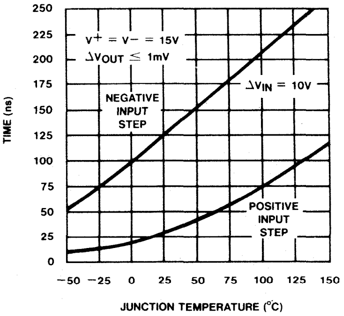
HOLD STEP vs INPUT VOLTAGE



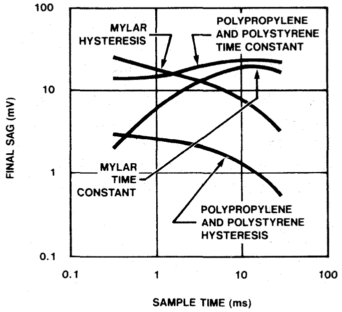
ACQUISITION TIME



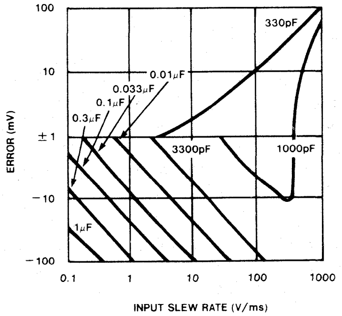
APERTURE TIME



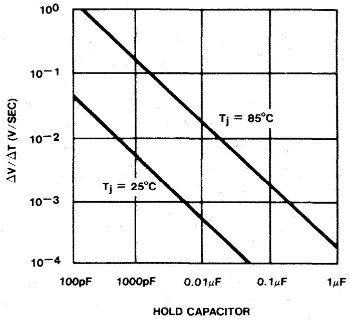
CAPACITOR HYSTERESIS



DYNAMIC SAMPLING ERROR



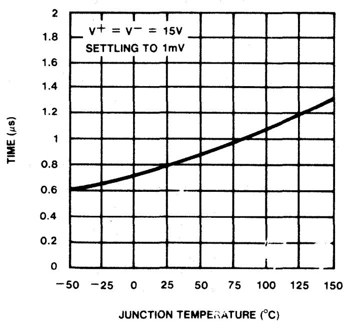
OUTPUT DROOP RATE



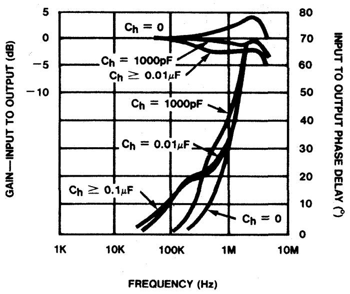
SAMPLE AND HOLD AMPLIFIER NE/SE5537

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

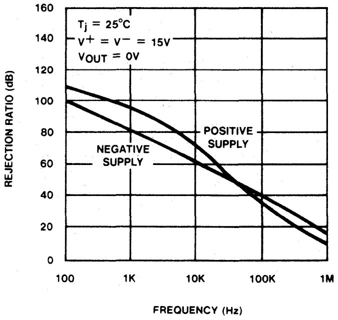
"HOLD" SETTLING TIME



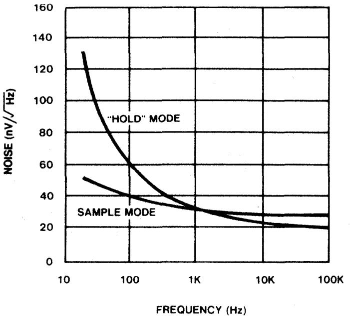
PHASE AND GAIN (INPUT TO OUTPUT, SMALL SIGNAL)



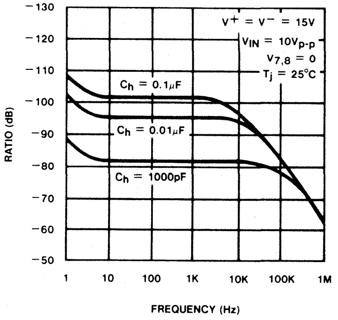
POWER SUPPLY REJECTION



OUTPUT NOISE



FEEDTHROUGH REJECTION RATIO (HOLD MODE)



SAMPLE AND HOLD

INTRODUCTION

For many years designers have used the sample and hold (or track and hold) to operate on analog information in a time frame which is expedient.

By sampling a segment of the information and holding it until the proper timing for converting to some form of control signal or readout allows the designer certain freedom in performing predetermined manipulative functions. Therefore, the sample and hold can be defined as a "selective analog memory cell".

The memory is volatile and will also decay with time.

When using the sample and hold method for evaluating signal information, the designer is given the added feature of eliminating outside noise elements. With the analog to digital converter products available today the "dc memory" of the sample and hold can be easily converted to digital format and further incorporated into microprocessor based systems.

Parametric evaluation of the sample and hold will be discussed in the following paragraphs.

DEFINITION OF TERMS

ACQUISITION TIME: The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

APERTURE DELAY TIME: The time elapsed from the hold command to the opening of the switch.

APERTURE JITTER: Also called "aperture uncertainty time", it's the time variation or uncertainty with which the switch opens, or the time variation in aperture delay.

APERTURE TIME: The delay required between "hold" command and an input analog transition, so that the transition does not affect the held output.

BANDWIDTH: The frequency at which the gain is down 3dB from its dc value. It's measured in sample (track) mode with a small-signal sine wave that doesn't exceed the slew rate limit.

EFFECTIVE APERTURE DELAY: The time difference between the hold command and the time at which the input signal is at the held voltage.

FIGURE OF MERIT: The ratio of the available charging current during sample mode to the leakage current during hold mode.

HOLD-MODE DROOP: The output voltage change per unit of time while in hold. Commonly specified in V/s, μV/μs or other convenient units.

HOLD-MODE FEEDTHROUGH: The percentage of an input sinusoidal signal that is measured at the output of a sample-hold when it's in hold mode.

HOLD SETTLING TIME: The time required for the output to settle within 1mV of final value after the "hold" logic command.

SAMPLE-TO-HOLD OFFSET ERROR: The difference in output voltage between the time the switch starts to open, and the time when the output has settled completely. It is caused by charge being transferred to the hold capacitor switch as it opens.

SLEW RATE: The fastest rate at which the sample & hold output can change (specified in V/μs).

HOLD STEP: The voltage step at the output of the sample and hold when switching from sample mode to hold mode with a steady (dc) analog input voltage. Logic swing is 5V.

DYNAMIC SAMPLING ERROR: The error introduced into the held output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

GAIN ERROR: The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

THRESHOLD: Level shall be defined as that level which causes the switch control to change state.

BASIC BLOCK DIAGRAM

The basic circuit concept of the sample and hold circuit incorporates the use of two (2) operational amplifiers and a switch control mechanism (which determines sample, hold or track conditions). Reference figure 1.

The block diagram of the NE5537 is a closed loop non-inverting unity gain sample and hold system. The input buffer amplifier supplies the current necessary to charge the hold capacitor, while the output buffer amplifier closes the loop such that the output voltage is identical to the input voltage (with consideration for input offset voltage, offset current, and temperature variations which are common to *all* sample and hold circuits, be they monolithic, hybrid or modular).

When the sampling switch is open (in the hold mode) the clamping diodes close the loop around the input amplifier to keep it from being overdriven into saturation.

The switch control is driven by external logic levels via a timing sequence remote from the sample and hold device. Reference figure 2. The switch control has a floating reference (pin 7), referred to as the logic reference which makes the sample and hold device compatible to several types of external logic signals (TTL, PMOS, & CMOS). The switching device operates at a threshold level of 1.4V.

The switch mechanism is on (sampling an information stream) when the logic level is high (pin 8 is 1.4 volts higher than pin 7) and presents a load of 5 microamperes to the input logic signal. The analog sampled signal is amplified, stored (in the external holding capacitor), and buffered. At the end of the sampling period the internal switch mechanism turns off (switch opens) and the "stored analog memory" information on the external capacitor (pin 6) is loaded down by an operational amplifier connected in the unity gain non-inverting configuration. This amplifier, whose input impedance is effectively:

$$R = R_{IN}(A_{OL})/(1 + 1/A)$$

where R = Effective input impedance
R_{IN} = Open loop input impedance
A_{OL} = Open loop gain
A = AC loop gain

Therefore, the higher the open loop gain of the second operational amplifier, the larger the effective loading on the capacitor. The larger the load, the lower the "leakage" current and the better the droop characteristics.

In actuality the amplifiers are designed with special leakage current cancellation circuits along with FET input devices. The leakage current cancellation circuits give better high temperature operation (remember that the FET amplifiers double in required bias current for every 10 degree increase in junction temperature).

Sampling time for the NE5537 is less than 10μsec, (measured to 0.1% of input signal). Leakage current is 6pA at a rate output load of 2kΩ.

BASIC APPLICATIONS

Multiplying DAC

As depicted in the block diagram of figure 3, the sample and hold circuit is used to supply a "variable" reference to the digital to analog converter. As the input reference varies, the output will change in accordance with equation 1, shown in figure 3.

Varying the input signal reference level can aid the system in performing both compression and expansion operations. The multiplying DAC's used are the Signetics SE/NE 5008; however, if the rate of change of the reference variation is kept slow enough a microprocessor compatible DAC can be incorporated, such as the NE5018 or the NE5020.

DATA ACQUISITION SYSTEMS

As mentioned earlier, the designer may wish to operate on several different segments of an "analog" signal; however he is limited by the fact that only one analog to digital converter channel is available to him. Figure 4 shows the means by which a multiplexing system may be accomplished.

APPLICATION HINTS

Hold Capacitor

A significant source of error in an accurate sample and hold circuit is dielectric absorption in the hold capacitor. A mylar cap, for instance, may "sag back" up to 0.2% after a quick change in voltage. A long "soak" time is required before the circuit can be put back into the hold mode with this type of capacitor. Dielectrics with very low hysteresis are polystyrene, polypropylene, and Teflon. Other types such as mica and polycarbonate are not nearly as good. Ceramic is unusable with >1% hysteresis. The advantage of polypropylene over polystyrene is that it extends the maximum ambient temperature from 85°C to 100°C. The hysteresis relaxation time constant in polystyrene, for instance, is 10-50ms. If A-to-D conversion can be made within 1ms, hysteresis error will be reduced by a factor of ten.

DC Zeroing

DC Zeroing is accomplished by connecting the offset adjust pin to the wiper of a 1kΩ potentiometer which has one end tied to V^+ and the other end tied through a resistor to ground. The resistor should be selected to give ≃0.6mA through the 1KΩ potentiometer.

Sampling Dynamic Signals

Sampling errors due to moving (changing) input signals are of significant concern to designers employing sample and hold circuits. There exist finite phase delays through the sample and hold circuit causing an input-output phase differential for moving signals. In addition, the series protection resistor (300Ω to pin 6 of the NE5537) will add an RC time constant, over and above the slew rate limitation of the input buffer/current drive amplifier. This means that at the moment the "hold" command arrives, the hold capacitor voltage may be somewhat different than the actual analog input. The effect of these delays is opposite to the effect created by delays in the logic which switches the circuit from sample to hold. For example, consider an analog input of 20 Vp-p at 10kHz. Maximum dV/dt is 0.6V/μs. With no analog phase delay and 100ns logic delay, one could expect up to (0.1μs) (0.6V/μs) = 60mV error if the "hold" signal arrived near maximum dV/dt of the input. A positive going input would give a ±60mV error. Now assume a 1MHz (3dB) bandwidth for the overall analog loop. This generates a phase delay of 160ns. If the hold capacitor sees this exact delay, then error due to analog delay will be (0.16μs) (0.6V/μs) = −96mV (analog) for a total of −36mV. To add to the confusion, analog delay is proportional to hold capacitor value while digital delay remains constant. A family of curves (dynamic sampling error) is included to help estimate errors.

A curve labeled *Aperture Time* has been included for sampling conditions where the input is steady during the sampling period, but may experience a sudden change nearly coincident with the "hold" command. This curve is based on a 1mV error fed into the output.

A second curve, *Hold Settling Time* indicates the time required for the output to settle to 1mV after the "hold" command.

Digital Feedthrough

Fast rise time logic signals can cause hold errors by feeding externally into the analog input at the same time the amplifier is put into the hold mode. To minimize this problem, board layout should keep logic lines as far as possible from the analog input. Grounded guarding traces may also be used around the input line, especially if it is driven from a high impedance source. Reducing high amplitude logic signals to 2.5V will also help.

Logic signals also couple to the hold capacitor. This hold capacitor should be guarded by a P.C. card trace connected to the sample-and-hold output. This will also minimize board leakage.

SPECIAL NOTES

1. Not all definitions herein defined are measured parametrically for the NE5537, but are legitimate terms used in sample and hold systems.
2. Reference should be made to Design Engineering, volumes 23 (Nov. 8, 1978), 25 (Dec. 6, 1978) and 26 (Dec. 20, 1978) for articles written by Eugene Zuch of Datel Systems, Inc. for a further discussion of sample and hold circuits.
3. Reference also made to National Semiconductor Corporation's Special Functions Data Book (1976).

TYPICAL APPLICATIONS

TYPICAL CONNECTION

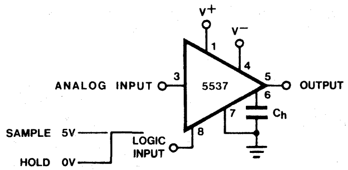
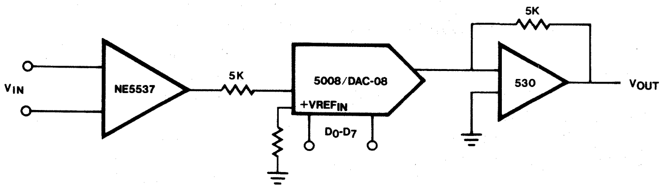


Figure 2

MULTIPLYING DAC APPLICATION



$$V_{OUT} = V_{IN} \times \frac{1}{256}\left\{2^0 D_0 + 2^1 D_1 + \quad 2^7 D_7\right\}$$ EQUATION 1

Figure 3

ANALOG DATA MULTIPLEXING

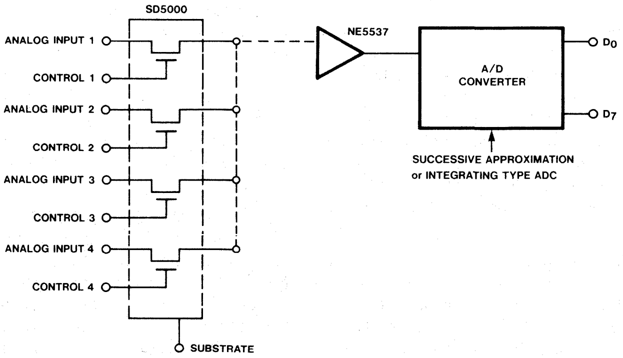


Figure 4

Section 13
Transistor Arrays

INDEX

Section 13 — Transistor Arrays

SEVEN TRANSISTOR ARRAY

CA3081/CA3082

DESCRIPTION

The CA3081 and CA3082 are monolithic integrated circuits, each consisting of seven separate npn transistors on a common substrate. The transistors are capable of driving loads of up to 100mA. At the same time, the transistor geometry used gives maximum current gain at quite low currents, making the devices also suitable for small-signal applications. In the CA3081, the transistors are connected in a common emitter configuration, while in the CA3082, the collectors are common. The transistor arrays are particularly suitable for driving light-emitting diodes and seven-segment displays, as well as for general purpose applications. The CA3081 and CA3082 are available in both 16-lead dual-in-line plastic and cerdip packages.

FEATURES

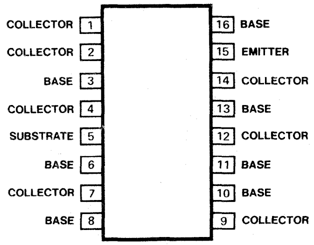
- **Seven transistors permit a wide range of applications in either a common emitter (CA3081) or common-collector (CA3082) configuration.**
- **High I_C: 100mA maximum**
- **Low $V_{CE\ sat}$ (at 50mA): 0.4V typical**

APPLICATIONS

- **Drivers for:**
  Incandescent display devices
  LED
  Relay control
  Thyristor firing

PIN CONFIGURATIONS

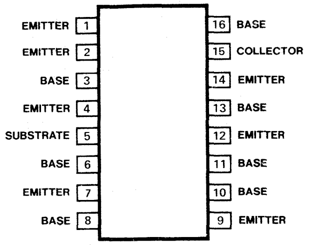
F,N PACKAGE



TOP VIEW

ORDER NUMBERS
CA3081F, CA3081N

F,N PACKAGE



TOP VIEW

ORDER NUMBERS
CA3082F, CA3082N

PIN DESIGNATION (CA3081)

PIN NO.	SYMBOL	NAME AND FUNCTION
1	C1	Collector, Transistor 1
2	C2	Collector, Transistor 2
3	B2	Base, Transistor 2
4	C5	Collector, Transistor 5
5	SUB	Substrate
6	B5	Base, Transistor 5
7	C7	Collector, Transistor 7
8	B7	Base, Transistor 7
9	C6	Collector, Transistor 6
10	B6	Base, Transistor 6
11	B4	Base, Transistor 4
12	C4	Collector, Transistor 4
13	B3	Base, Transistor 3
14	C3	Collector, Transistor 3
15	E	Common emitter
16	B1	Base, Transistor 1

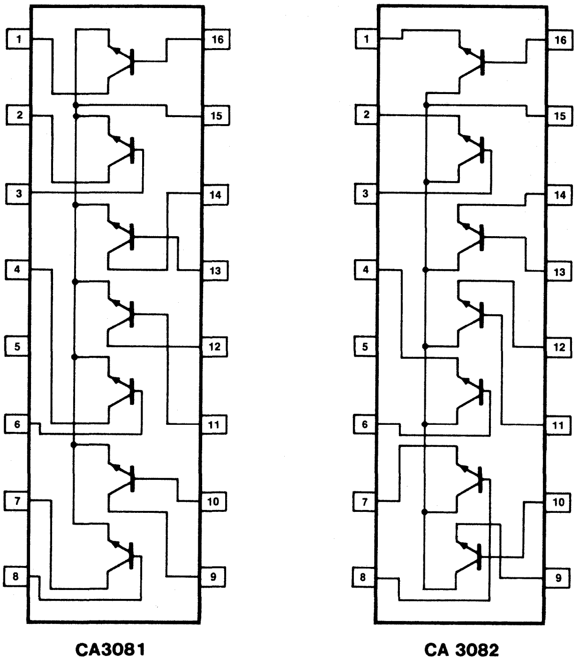
PIN DESIGNATION (CA3082)

PIN	SYMBOL	NAME AND FUNCTION
1	E1	Emitter, Transistor 1
2	E2	Emitter, Transistor 2
3	B2	Base, Transistor 2
4	E5	Emitter, Transistor 5
5	SUB	Substrate
6	B5	Base, Transistor 5
7	E6	Emitter, Transistor 6
8	B6	Base, Transistor 6
9	E7	Emitter, Transistor 7
10	B7	Base, Transistor 7
11	B4	Base, Transistor 4
12	E4	Emitter, Transistor 4
13	B3	Base. Transistor 3
14	E3	Emitter, Transistor 3
15	C	Common collector
16	B1	Base, Transistor 1

SEVEN TRANSISTOR ARRAY

CA3081/CA3082

BLOCK DIAGRAM



CA3081 CA 3082

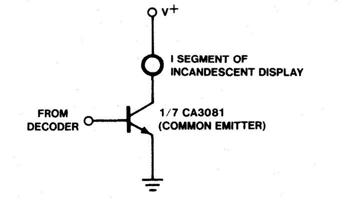
ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$

	PARAMETER	RATING	UNIT
P	Power dissipation:		
	Any one transistor	500	mW
P_{TOT}	Total package	750	mW
	Above 55°C	Derate Linearly 6.67	mW/°C
	Ambient temperature range:		
T_A	Operating	−55 to +125	°C
T_{stg}	Storage	−65 to +150	°C
	Lead temperature (10 seconds)	265	°C
V_{CEO}	Collector to emitter voltage[1]	16	V
V_{CBO}	Collector to base voltage[1]	20	V
V_{CIO}	Collector to substrate voltage[1,2]	20	V
V_{EBO}	Emitter to base voltage[1]	5	V
I_C	Collector current[1]	100	mA
I_B	Base current[1]	20	mA

NOTES

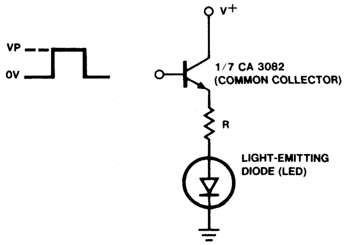
1. Ratings apply for each transistor in the device.
2. The collector of each transistor of the CA3081 and CA3082 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

TYPICAL READ-OUT DRIVER APPLICATIONS



NOTE
Schematic diagram showing one transistor of the CA3081 driving one segment of an incandescent display.

Figure 6



NOTES
Schematic diagram showing one transistor of the CA3082 driving a light-emitting diode (LED).

*The resistance for R is determined by the relationship

$$R = \frac{V_P - V_{BE} - V_F(LED)}{I(LED)}$$

$R = 0$ for $V_P = V_{BE} + V_F(LED)$

Where: V_P = Input pulse voltage
V_F = Forward voltage drop across the diode

Figure 7

SEVEN TRANSISTOR ARRAY CA3081/CA3082

STATIC ELECTRICAL CHARACTERISTICS FOR EACH TRANSISTOR $T_A = 25°C$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CBO} (BR)	Collector to base breakdown voltage	$I_C = 500\mu A, I_E = 0$	20	60		V
V_{CIO} (BR)	Collector to substrate breakdown voltage	$I_C = 500\mu A, I_E = 0, I_B = 0$	20	60		V
V_{CEO} (BR)	Collector to emitter breakdown voltage	$I_C = 1mA, I_B = 0$	16	24		V
V_{EBO} (BR)	Emitter to base breakdown voltage	$I_C = 500\mu A$	5	6.9		V
h_{FE}	DC forward current Transfer Ratio	$V_{CE} = 0.5V, I_C = 30mA$	30	68		
		$V_{CE} = 0.8V, I_C = 50mA$	40	70		
V_{BE} sat	Base to emitter saturation voltage	$I_C = 30mA, I_B = 1mA$		0.87	1.0	V
V_{CE} sat	Collector to emitter saturation voltage					
	CA3081/CA3082	$I_C = 30mA, I_B = 1mA$		0.27	0.5	V
	CA3081	$I_C = 50mA, I_B = 5mA$		0.4	0.7	V
	CA3082	$I_C = 50mA, I_B = 5mA$		0.4	0.8	V
I_{CEO}	Collector cutoff current	$V_{CE} = 10V, I_B = 0$			10	μA
I_{CBO}	Collector cutoff current	$V_{CB} = 10V, I_E = 0$			1	μA

TYPICAL PERFORMANCE CHARACTERISTICS

h_{FE} vs I_C

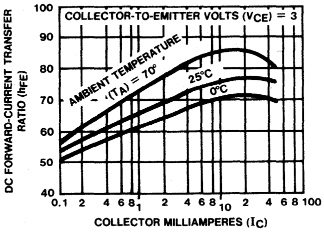


Figure 2

V_{BEsat} vs I_C

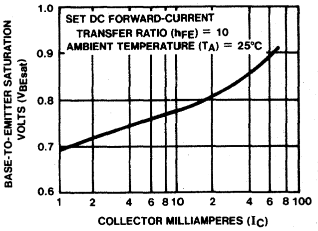


Figure 3

V_{CEsat} vs I_C at T_A = 25°C

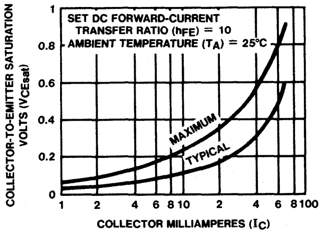


Figure 4

V_{CEsat} vs I_C at T_A = 70°C

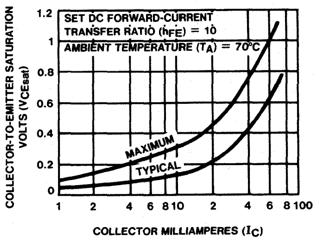


Figure 5

HIGH VOLTAGE TRANSISTOR ARRAY

CA3183

DESCRIPTION

The CA3183 is a general purpose high-voltage silicon n-p-n transistor array on a common monolithic substrate. This integrated circuit features a tighter control of breakdown voltage, providing for applications requiring higher voltages. The array consists of five high-current transistors with independent connections for each transistor. Additionally, two of the transistors (Q_1 and Q_2) are matched at low-current for applications where offset parameters are of special importance. A special substrate terminal has also been included for greater flexibility in circuit design. The CA3183 is available in both 16-lead dual-in-line plastic and cerdip packages and operates over the ambient temperature range of −40°C to +85°C.

FEATURES

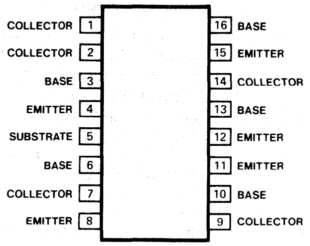
- Matched general purpose transistors
- V_{BE} matched ±5mV maximum
- High I_C : 75mA maximum

APPLICATIONS

- General use in signal processing systems in dc through VHF range
- Custom designed differential amplifiers
- Temperature compensated amplifiers
- Lamp and relay drivers
- Thyristor firing

PIN CONFIGURATION

F, N PACKAGE



TOP VIEW

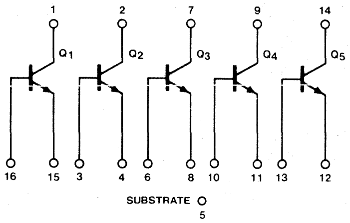
ORDER NUMBERS

CA3183F CA3183N

PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	C1	Collector, transistor 1
2	C2	Collector, transistor 2
3	B2	Base, transistor 2
4	E2	Emitter, transistor 2
5	SUB	Substrate
6	B3	Base, transistor 3
7	C3	Collector, transistor 3
8	E3	Emitter, transistor 3
9	C4	Collector, transistor 4
10	B4	Base, transistor 4
11	E4	Emitter, transistor 4
12	E5	Emitter, transistor 5
13	B5	Base, transistor 5
14	C5	Collector, transistor 5
15	E1	Emitter, transistor 1
16	B1	Base, transistor 1

BLOCK DIAGRAM



HIGH VOLTAGE TRANSISTOR ARRAY CA31

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CEO}	Collector-emitter voltage[1]	40	V
V_{CBO}	Collector-base voltage[1]	50	V
V_{CIO}	Collector-substrate voltage[1,2]	50	V
V_{EBO}	Emitter-base voltage[1]	5	V
I_C	Collector current[1]	75	mA
I_B	Base current[1]	20	mA
P	Power dissipation:		
	any one transistor	500	mW
P_{TOT}	total package up to 55°C	750	mW
T_A	Operating ambient temperature	−40 to +85	°C
T_{stg}	Storage temperature	−65 to +150	°C

NOTES

1. For each transistor.
2. The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal should be maintained at either dc or signal (ac) ground. A suitable bypass capacitor can be used to establish a signal ground.

STATIC ELECTRICAL CHARACTERISTICS FOR EACH TRANSISTOR T_A = 25°C unless otherwise specified.

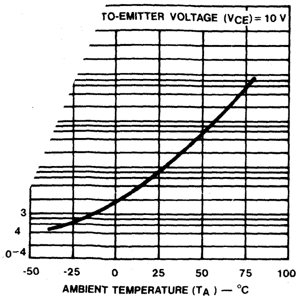
PARAMETER		TEST CONDITIONS	CA3183			UNIT
			Min	Typ	Max	
V_{CEO} (BR)	Collector-emitter breakdown voltage	$I_C = 1mA, I_B = 0$	40			V
V_{CBO} (BR)	Collector-base breakdown voltage	$I_C = 100\mu A, I_E = 0$	50			V
V_{CIO} (BR)	Collector-substrate breakdown voltage	$I_{CI} = 100\mu A, I_B = 0, I_E = 0$	50			V
V_{EBO} (BR)	Emitter-base breakdown voltage	$I_E = 500\mu A, I_C = 0$	5			V
I_{CEO}	Collector cutoff current	$V_{CE} = 10V, I_B = 0$			10	μA
I_{CBO}	Collector cutoff current	$V_{CB} = 10V, I_E = 0$			1	μA
h_{FE}	DC forward current transfer ratio	$V_{CE} = 3V, I_C = 10mA$ $V_{CE} = 5V, I_C = 50mA$	40 40			
V_{BE}	Base-emitter voltage	$V_{CE} = 3V, I_C = 10mA$	0.65	0.75	0.85	V
V_{CE} (SAT)	Collector-emitter saturation voltage	$I_C = 50mA, I_B = 5mA$		1.7	3.0	V

STATIC ELECTRICAL CHARACTERISTICS FOR TRANSISTORS Q1 AND Q2 (AS A DIFFERENTIAL AMPLIFIER) T_A = 25°C unless otherwise specified.

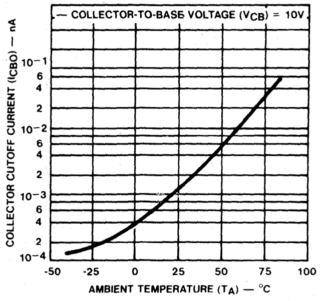
PARAMETER		TEST CONDITIONS	CA3183			UNIT
			Min	Typ	Max	
V_{IO}	Absolute input offset voltage	$V_{CE} = 3V, I_C = 1mA$		0.47	5	mV
I_{IO}	Absolute input offset current	$V_{CE} = 3V, I_C = 1mA$		0.78	2.5	μA

MANCE CHARACTERISTICS

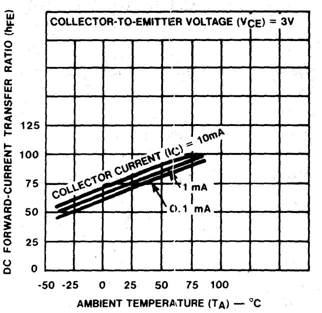
ANY TRANSISTOR



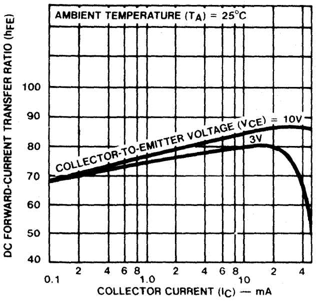
I_{CBO} v T_A FOR ANY TRANSISTOR



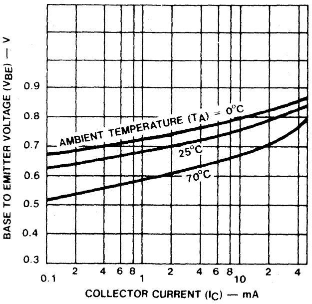
h_{FE} v T_A FOR ANY TRANSISTOR



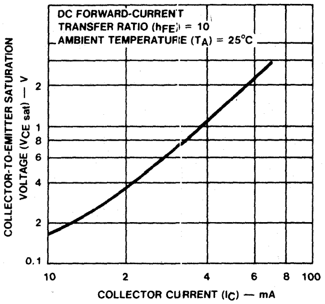
h_{FE} v I_C FOR ANY TRANSISTOR



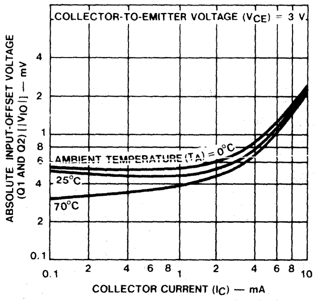
V_{BE} v I_C FOR ANY TRANSISTOR



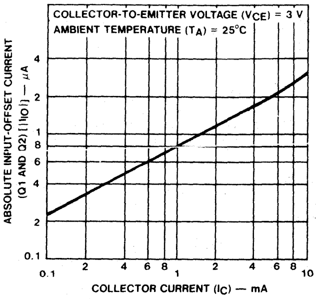
V_{CE} sat v I_C FOR ANY TRANSISTOR



$|V_{IO}|$ v I_C FOR DIFFERENTIAL AMPLIFIER (Q1 AND Q2)



$|I_{IO}|$ v I_C FOR DIFFERENTIAL AMPLIFIER (Q1 AND Q2)



HIGH VOLTAGE/HIGH CURRENT DARLINGTON TRANSISTOR ARRAYS ULN2001/03/04

DESCRIPTION

These high-voltage, high-current Darlington transistor arrays are comprised of seven silicon NPN Darlington pairs on a common monolithic substrate. All units feature open collector outputs and integral suppression diodes for inductive loads. Peak inrush currents to 600mA are allowable, making them ideal for driving tungsten filament lamps also.

The Type ULN-2001 is a general-purpose array which may be used with DTL, TTL, PMOS, CMOS, etc. It is pinned with inputs opposite outputs to facilitate ease of circuit board layout and is priced to compete directly with discrete transistor alternatives.

The Type ULN-2003 has a series base resistor to each Darlington pair, and thus allows operation directly with TTL or CMOS operating at a supply voltage of 5V.

The Type ULN-2004 has an appropriate series input resistor to allow its operation directly from CMOS or PMOS outputs utilizing supply voltages of 6 to 15V. The required input current is below that of the Type ULN-2003.

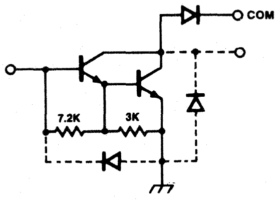
In all cases, the individual Darlington pair collector current rating is 500mA. However, outputs may be paralleled for higher load current capability. All devices are supplied in a 16-pin dual in-line plastic package.

FEATURES

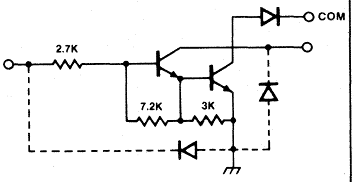
- **Peak inrush current 600mA**
- **Protected internally against inductive loads**
- **Open collector topology**
- **Compatible with most logic technologies**

EQUIVALENT SCHEMATICS

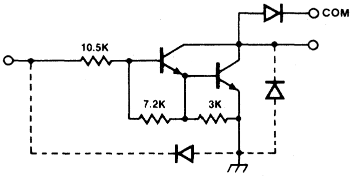
TYPE ULN2001
(each driver)



TYPE ULN2003
(each driver)

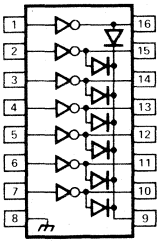


TYPE ULN2004
(each driver)



PIN CONFIGURATION

N,F PACKAGE



TOP VIEW

ORDER NUMBERS
ULN2001N,F
ULN2003N,F
ULN2004N,F

ABSOLUTE MAXIMUM RATINGS

at 25°C Free-Air temperature for any one Darlington pair unless otherwise specified.

PARAMETER		RATING	UNIT
V_{CE}	Output voltage	50	V
V_{IN}	Input voltage	30	V
V_{EBO}	Emitter base voltage	6	V
I_C	Continuous collector current	500	mA
I_B	Continuous base current	25	mA
P_D	Power dissipation	1.3	W
	Derating factor above 25°C	95	°C/W
T_A	Ambient temperature range (operating)	0 to +85	°C
T_S	Storage temperature range	-65 to +150	°C

*NOTE
Under normal operating conditions, these units will sustain 350mA per output with $V_{CE(SAT)}$ = 1.6V at 70°C with a pulse width of 20 ms and a duty cycle of 30%.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.[1,2,3]

PARAMETER		TEST CONDITIONS	Test Fig.	LIMITS			UNIT
				Min	Typ	Max	
I_{CEX}	Output leakage current	$V_{CE} = 50V$, $T_A = 70°C$	1A	—	—	100	μA
	Type ULN-2004	$V_{CE} = 50V$, $T_A = 70°C$, $V_{IN} = 1V$	1B	—	—	500	μA
$V_{CE(SAT)}$	Collector-emitter	$I_C = 350mA$, $I_B = 500\mu A$	2	—	1.25	1.6	V
	Saturation voltage	$I_C = 200mA$, $I_B = 350\mu A$	2	—	1.1	1.3	V
		$I_C = 100mA$, $I_B = 250\mu A$	2	—	0.9	1.1	V
$I_{IN(ON)}$	Input current						
	Type ULN-2003	$V_{IN} = 3.85V$	3	—	0.93	1.35	mA
	Type ULN-2004	$V_{IN} = 5V$	3	—	0.35	0.5	mA
		$V_{IN} = 12V$	3	—	1.0	1.45	mA
$I_{IN(OFF)}$	Input current	$I_C = 500\mu A$, $T_A = 70°C$	4	50	65	—	μA
$V_{IN(ON)}$	Input voltage						
	Type ULN-2003	$V_{CE} = 2V$, $I_C = 200mA$	5	—	—	2.4	V
		$V_{CE} = 2V$, $I_C = 250mA$	5	—	—	2.7	V
		$V_{CE} = 2V$, $I_C = 300mA$	5	—	—	3.0	V
	Type ULN-2004	$V_{CE} = 2V$, $I_C = 125mA$	5	—	—	5.0	V
		$V_{CE} = 2V$, $I_C = 200mA$	5	—	—	6.0	V
		$V_{CE} = 2V$, $I_C = 275mA$	5	—	—	7.0	V
		$V_{CE} = 2V$, $I_C = 350mA$	5	—	—	8.0	V
h_{FE}	D-C forward current transfer ratio Type ULN-2001	$V_{CE} = 2V$, $I_C = 350mA$	2	1000		—	—
C_{IN}	Input capacitance		—	—	15	30	pF
I_R	Clamp diode leakage current	$V_R = 50V$	6	—	—	50	μA
V_F	Clamp diode forward voltage	$I_F = 350mA$	7	—	1.7	2	V

NOTES

1. All limits stated apply to the complete Darlington series except as specified for a single device type.
2. The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
3. The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.[1,2,3]

PARAMETER		TEST CONDITIONS	Test Fig.	LIMITS			UNIT
				Min	Typ	Max	
t_{PLH}	Turn-on delay	0.5 E_{IN} to 0.5 E_{OUT}	—	—	1.0	5	μs
t_{PHL}	Turn-off delay	0.5 E_{IN} to 0.5 E_{OUT}	—	—	1.0	5	μs

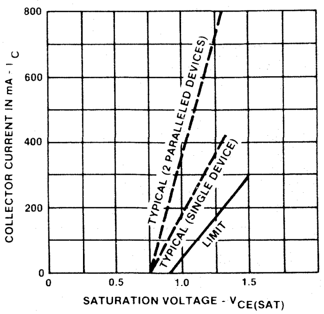
NOTES

1. All limits stated apply to the complete Darlington series except as specified for a single device type.
2. The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
3. The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

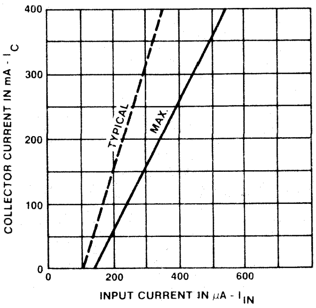
HIGH VOLTAGE/HIGH CURRENT DARLINGTON TRANSISTOR ARRAYS ULN2001/03/04

TYPICAL PERFORMANCE CHARACTERISTICS

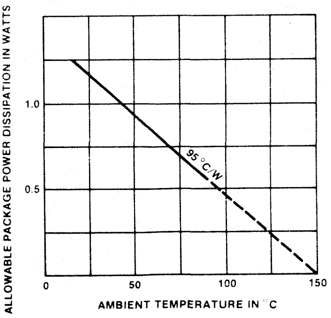
COLLECTOR CURRENT AS A FUNCTION OF SATURATION VOLTAGE



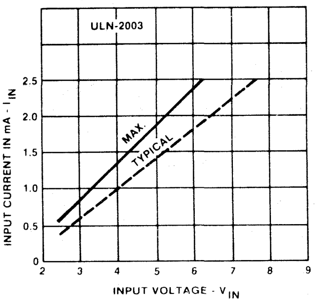
COLLECTOR CURRENT AS A FUNCTION OF INPUT CURRENT



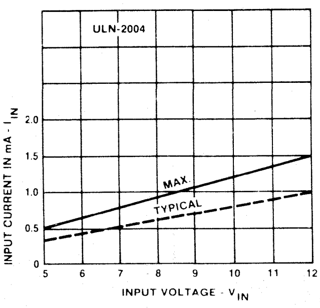
ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE FOR TYPE ULN-2003



INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE FOR TYPE ULN-2004



TEST FIGURES

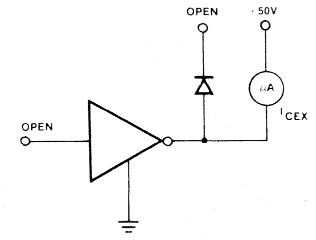


Figure 1A

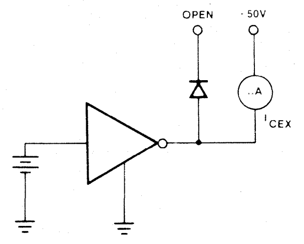


Figure 1B

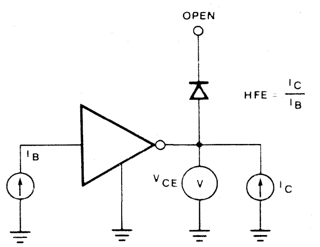


Figure 2

TEST FIGURES (Cont'd)

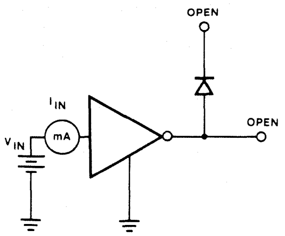


Figure 3

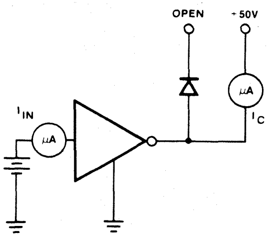


Figure 4

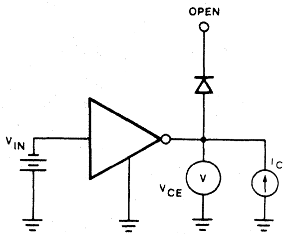


Figure 5

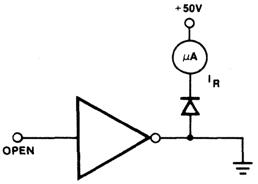


Figure 6

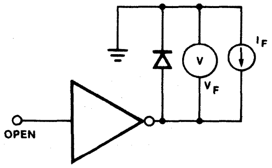
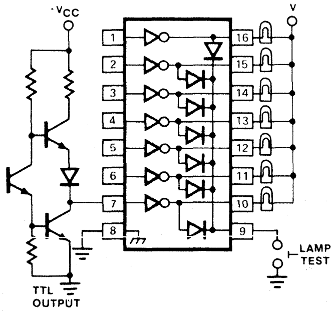


Figure 7

TYPICAL APPLICATIONS

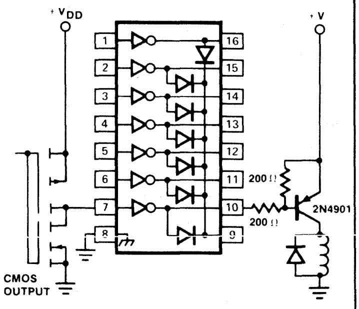
TTL TO LOAD

ULN2003



BUFFER FOR HIGHER CURRENT LOADS

ULN2004



Section 14
Radio Circuits

INDEX

Section 14 — Radio Circuits

14

FM IF SYSTEM CA3089

DESCRIPTION

CA3089 is a monolithic integrated circuit that provides all the functions of a comprehensive FM-IF system. Figure 6 is a block diagram showing the CA3089 features, which include a three-state FM-IF amplifier/limiter configuration with level detectors for each stage, a doubly-balanced quadrature FM detector and an audio amplifier that features the optional use of a muting (squelch) circuit.

The advanced circuit design of the IF system includes desirable features such as delayed AGC for the RF tuner, an AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. In addition, internal power supply regulators maintain a nearly constant current drain over the voltage supply range of +8 to +18 volts.

The CA3089 is ideal for high-fidelity operation. Distortion in a CA3089 FM-IF system is primarily a function of the phase linearity characteristic of the outboard detector coil.

The CA3089 utilizes a 16-lead dual-in-line plastic package and can operate over the ambient temperature range of −40°C to +85°C.

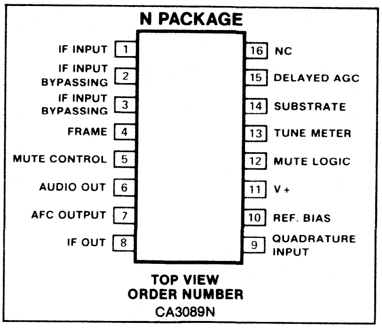
FEATURES

- **Exceptional limiting sensitivity: 10μV typ. at −3dB point**
- **Low distortion: 0.1% typ. (with double-tuned coil)**
- **Single-coil tuning capability**
- **High recovered audio: 400mV typ.**
- **Provides specific signal for control of interchannel muting (squelch)**
- **Provides specific signal for direct drive of a tuning meter**
- **Provides delayed AGC voltage for RF amplifier**
- **Provides a specific circuit for flexible AFC**
- **Internal supply/voltage regulators**

APPLICATIONS

- **High-fidelity FM receivers**
- **Automotive FM receivers**
- **Communications FM receivers**

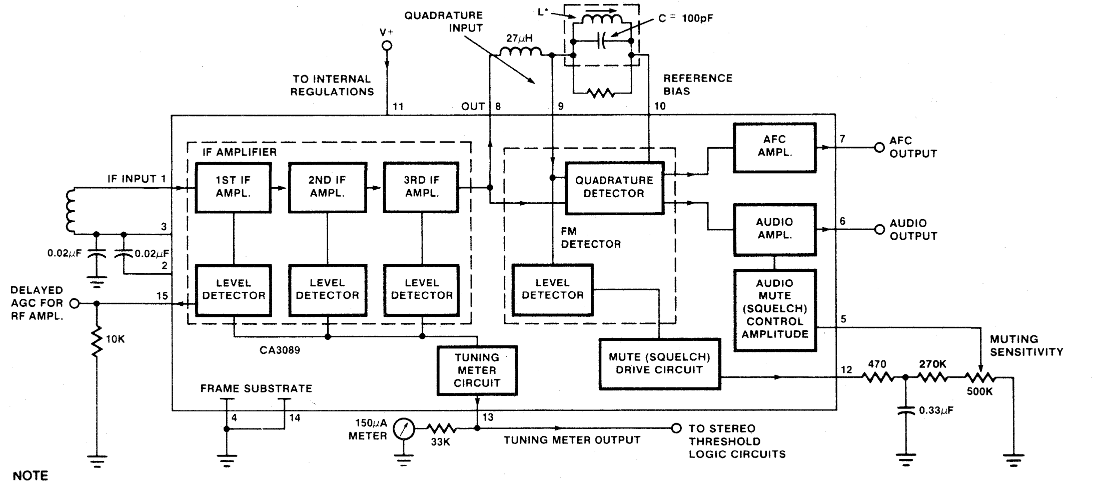
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

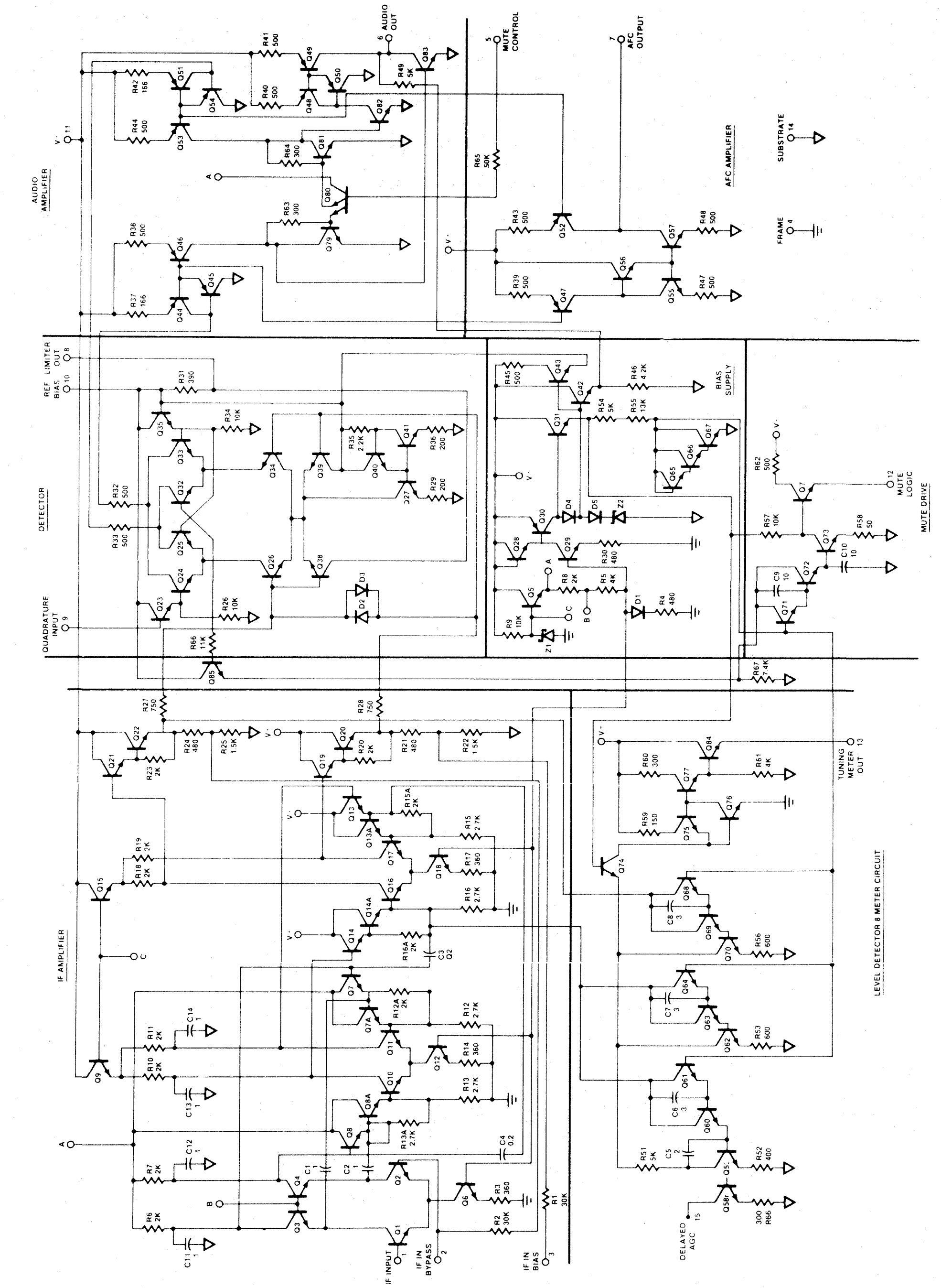
PARAMETER	RATING	UNIT
DC supply voltage:		
Between terminals 11 and 4	18	V
Between terminals 11 and 14	18	V
DC Current (out of terminal 15)	2	mA
Device dissipation:		
Up to T_A = 60°C	600	mW
Above T_A = 60°C	derate linearly 6.7	mW/°C
Ambient temperature range:		
Operating	−40 to +85	°C
Storage	−65 to +150	°C
Lead temperature (during soldering):		
At distance not less than 1/32" (0.79mm) from case for 10 seconds max	+265	°C

BLOCK DIAGRAM



NOTE
All resistors values are typical and in ohms. $Q_0 \simeq 75$ (G.I. EX27825 or equivalent)
*L tunes with 100pF (C) at 10.7MHz

EQUIVALENT SCHEMATIC



NOTE
All resistance values are typical and in ohms.
All capacitance values are in picofarads.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V^+ = 12V$ unless otherwise specified.

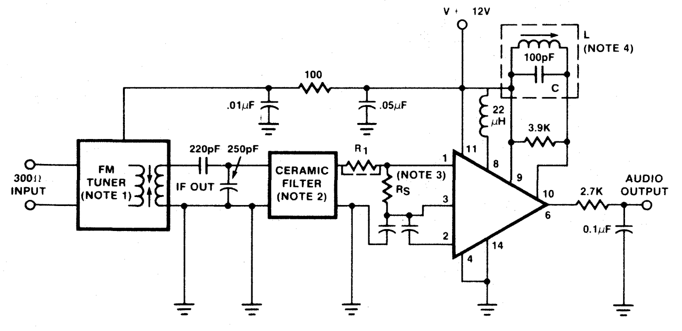
PARAMETER		TEST CONDITIONS	CA3089D2			UNIT
			Min	Typ	Max	
STATIC (DC) CHARACTERISTICS						
I_{11}	Quiescent circuit current	No signal input, non-muted	16	23	30	mA
DC Voltages:[4]						
V_1	Terminal 1 (IF input)	No signal input, non-muted	1.2	1.9	2.4	V
V_2	Terminal 2 (ac return to input)	No signal input, non-muted	1.2	1.9	2.4	V
V_3	Terminal 3 (dc bias to input)	No signal input, non-muted	1.2	1.9	2.4	V
V_6	Terminal 6 (audio output)	No signal input, non-muted	5.0	5.6	6.0	V
V_7	Terminal 7 (A.F.C.)	No signal input, non-muted	5.0	5.6	6.0	V
V_{10}	Terminal 10 (dc reference)	No signal input, non-muted	5.0	5.6	6.0	V
DYNAMIC CHARACTERISTICS						
$V_{I(lim)}$	Input limiting voltage (−3dB point)[3]			10	25	μV
	AMR AM Rejection (terminal 6)[4]	$V_{IN} = 0.1V$, $F_o = 10.7MHz$, $f_{mod} = 400Hz$, AM Mod = 30%	45	55		dB
V_O	Recovered audio voltage (terminal 6)[3]		400	500	600	mV
Total harmonic distortion:[1]						
THD	Single tuned (terminal 6)[3]			0.5	1.0	%
THD	Double tuned (terminal 6)[4]	$f_{mod} = 400Hz$, $V_{IN} = 0.1$		0.1		%
S+N/N	Signal plus noise to noise ratio (terminal 6)[3]	Deviation = ±75kHz $V_{IN} = 0.1V$	60	70		dB
MU_{IN}	Mute input (terminal 5)	$V_5 = 2.5V$	50	70		dB
MU_{OUT}	Mute output (terminal 12)	$V_{IN} = 50\mu V$			.5	V
		$V_{IN} = 0V$	4.0			V
MTR	Meter output (terminal 13)	$V_{IN} = 0.1V$	2.5	3.5		V
		$V_{IN} = 500\mu V$	1.0	1.5		V
		$V_{IN} = 0V$			.7	V
AGC	Delayed AGC (terminal 15)	$V_{IN} = .01V$			.5	V
		$V_{IN} = 10\mu V$	4.0	5.0		V
THD	Double tuned (terminal 6)[4]	$f_{mod} = 400Hz$ $V_{IN} = 0.1$		0.1		%

NOTES
1. THD characteristics and Audio Level are essentially a function of the phase and Q characteristics of the network connected between terminals 8,9, and 10.
2. Test circuit Figure 1.
3. Test circuit Figure 2.
4. Test circuit Figures 1 and 2.

FM IF SYSTEM CA3089

TEST CIRCUITS

TYPICAL FM TUNER (With a single-tuned detector coil.)



NOTES

All resistors values are typical and in ohms.

1. Waller 4SN3FIC or equivalent
2. Murate SFG 10.7mA or equivalent
3. R_S will affect stability depending on circuit layout. To increase stability R_S is decreased. Range of R_S is 330 to 50Ω, $R_1 + R_S \leq 330Ω$
4. L tunes with 100pF (C) at 10.7MHz
   Q_0 unloaded ≃ 75 (G.I. EX27825 or equivalent)

Performance data at f_o = 98MHz, f_{MOD} = 400Hz, deviation =

±74kHz:

−3dB limiting sensitivity	2µV (antenna level)
20dB quieting sensitivity	1µV (antenna level)
30dB quieting sensitivity	1.5µV (antenna level)

Figure 3

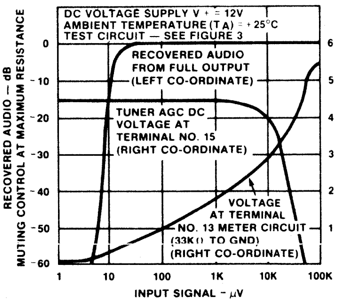
SYSTEM DESIGN CONSIDERATONS

The CA3089 is a very high gain device and therefore careful consideration must be given to the layout of external components to minimize feedback. The input bypass capacitors should be located close to the input terminals and the values should not be large nor should the capacitors be of the type which might introduce inductive reactance to the circuit. An example of good by-pass capacitors would be ceramic disc with values in the range of .01 to .05 microfarad.

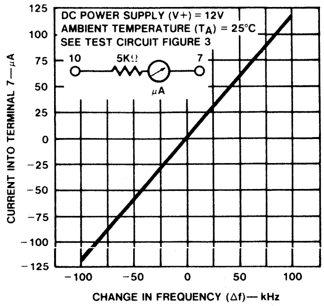
The input impedance of the CA3089 is approximately 10,000 ohms. It is *not* recommended to match this impedance. The value of the input termination resistor should be as low as possible without degrading system operation. The lower the value of this resistor the greater the system stability. An input terminating resistor between 50 and 100 ohms is recommended.

TYPICAL PERFORMANCE CHARACTERISTICS

MUTING ACTION, TUNER AGC
(Tuning meter output as a function of input signal voltage.)



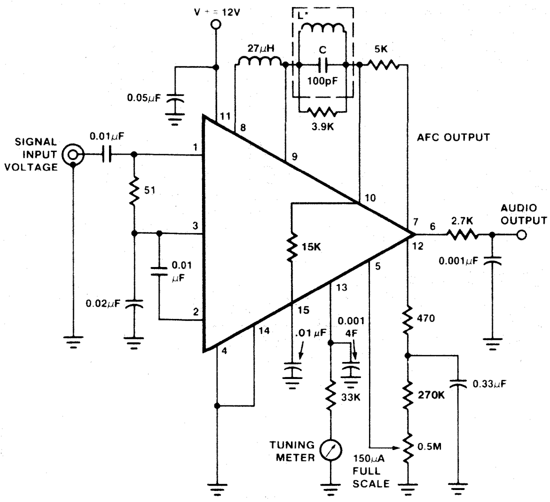
AFC CHARACTERISTICS
(Current at Term. 7 as a function of change in frequency.)



TEST CIRCUITS

TEST CIRCUIT

(Using a single-tuned detector coil.)



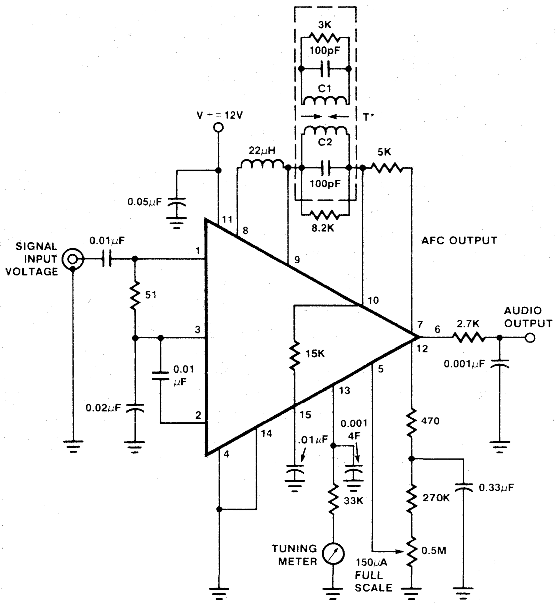
*NOTE

L tunes with 100pF (C) at 10.7MHz.
All resistors values are typical and in ohms.
Q_0 (unloaded) ≃ 75 (G.I. automatic mfg. div. EX27825 or equivalent).

Figure 1

TEST CIRCUIT

(Using a double-tuned detector coil.)



*NOTE

All resistors values are typical and in ohms.
T: Pri. – Q_0 (unloaded) ≃ 75 (tunes with 100pF (C1) 20 † of 34e on 7/32" dia. form)
Sec. – Q_0 (unloaded) ≃ 75 (tunes with 100pF (C2) 20 † of 34e on 7/32" dia. form)
kQ (percent of critical coupling) > 70%
(Adjusted for coil voltage V_C) = 150mV
Above values permit proper operation of mute (squelch) circuit "E" type slugs, spacing 4mm

Figure 2

FM/IF SYSTEM

CA3189

DESCRIPTION

The CA3189 is a monolithic integrated circuit that provides all the functions of a comprehensive FM/IF system. The CA3189 features a three stage FM/IF amplifier/limiter configuration with level detectors for each stage. A doubly balanced quadrature FM detector and an audio amplifier features the optional use of a muting (squelch) circuit. Mute is enabled when either the input signal level is low or when the input frequency changes, through an *external* mute logic circuit between pins 5 and 12. Center channel detect can also be derived via this mute logic circuit.

The CA3189 includes features found in the CA3089, such as delayed AGC for the RF tuner, an AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. Internal power supply regulators maintain a nearly constant current drain over the voltage range of +8V to +16V. The CA3189 FM/IF system distortion is primarily a function of the phase linearity of the outboard detector coil.

FEATURES

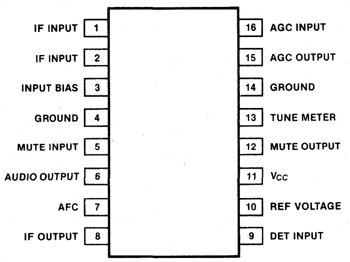
- **AGC threshold controlled externally**
- **Low signal or fre. muting option**
- **Single coil tuning capability**
- **Exceptional limiting sensitivity: 10μV typical at −3dB point**
- **Low distortion: 0.1% with double tuned coil**
- **High recovered audio: 500mV typical**
- **Internal supply/voltage regulators**
- **Mute—center channel detect**

APPLICATIONS

- **Automotive FM receivers**
- **High fidelity FM receivers**
- **Communications FM receivers**

PIN CONFIGURATION

N PACKAGE

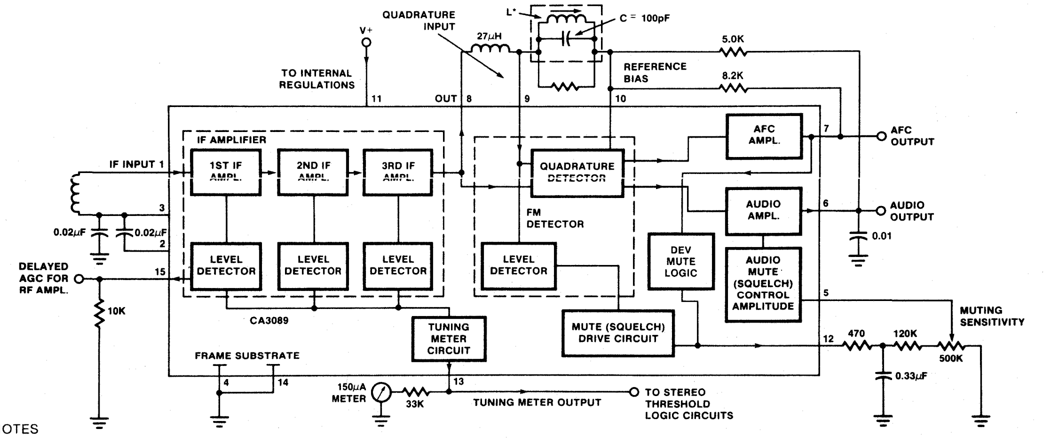


TOP VIEW
ORDER NUMBER
CA3189N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
DC supply voltage:		
Between terminals 11 and 4	18	V
Between terminals 11 and 14	18	V
DC current (out of terminal 15)	2	mA
Device dissipation:		
Up to $T_A = 60°C$	600	mW
Above $T_A = 60°C$	derate linearly 6.7	mW/°C
Ambient temperature range:		
Operating	−40 to +85	°C
Storage	−65 to +150	°C
Lead temperature (during soldering): At distance not less than 1/32″ (0.79mm) from case for 10 seconds max	+265	°C

BLOCK DIAGRAM



NOTES

All resistor values are typical and in ohms.

* L tunes with 100pF (C) at 10.7MHz.

$Q_O \cong 75$ (G.I. EX27825 or equivalent).

STATIC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V^+ = 12V$ unless otherwise specified.

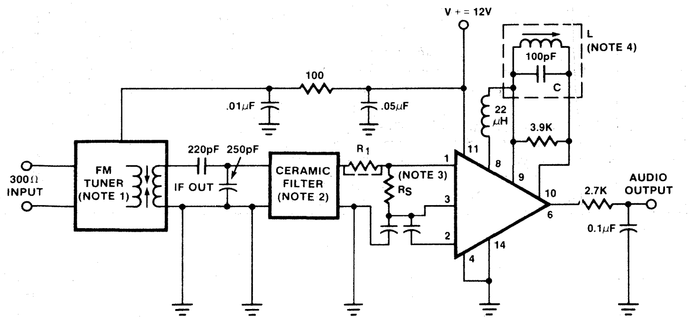
PARAMETER		TEST CONDITIONS	Min	Typ	Max	UNIT
I_{11}	Quiescent circuit current	No signal input, non-muted	16	28	40	mA
DC Voltages:[4]						
V1	Terminal 1 (IF input)	No signal input, non-muted	1.2	1.9	2.4	V
V2	Terminal 2 (AC return to input)	No signal input, non-muted	1.2	1.9	2.4	V
V3	Terminal 3 (DC bias to input)	No signal input, non-muted	1.2	1.9	2.4	V
V7	Terminal 7 (AFC)	No signal input, non-muted	5.0	5.6	6.0	V
V10	Terminal 10 (DC reference)	No signal input, non-muted	5.0	5.6	6.0	V

DYNAMIC CHARACTERISTICS

$V_{I(lim)}$	Input limiting voltage (−3dB point)[3]			10	25	μV
AMR	AM rejection (terminal 6)[3]	$V_{IN} = 0.1V$, $F_o = 10.7MHz$, $f_{mod} = 400Hz$, AM Mod = 30%	45	55		dB
V_O	Recovered audio voltage (terminal 6)[3]		325	500	650	mV
Total harmonic distortion: [1]						
THD	Single tuned (terminal 6)[3]			0.5	1.0	%
THD	Double tuned (terminal 6)[4]	$f_{mod} = 400Hz$, $V_{IN} = 0.1V$		0.1		%
S+N/N	Signal plus noise to noise ratio (terminal 6)[3]	Deviation— ± 75KHz	65	72		dB
MU	Mute (terminal 6)	V5 = 2.5V	50	70		dB
MU_{OUT}	Mute output (terminal 12)	$V_{IN} = 100\mu V$		0.1	0.7	V
		$V_{IN} = 0V$	4.0			
MUF	Deviation mute frequency	$V_{IN} = 0.1V$, f = 10.7KHz		± 40		KHz
MTR	Meteroutput (terminal 13)	$V_{IN} = 0.1V$	3.0	4.0		V
		$V_{IN} = 500\mu V$	1.0	1.5		
		$V_{IN} = 0V$		0.3	0.7	
AGC	Delayed AGC (terminal 15)	V16 > 2.5V		0.2	0.7	V
		V16 < 0.7V	8.0	10.0		
AGC	Threshold (terminal 16)	V15 = low to high		1.25	2.5	V
CS	On-channel step (terminal 12)	$V_{IN} = 0.1V$ f = 10.7MHz; $f_{DEV} <$ ± 15KHz		0	0.7	V
		$f_{DEV} >$ ± 80KHz	4.5	5.6		

TEST CIRCUITS

TYPICAL FM TUNER (With a Single-Tuned Detector Coil)



NOTES: All resistor values are typical and in ohms.

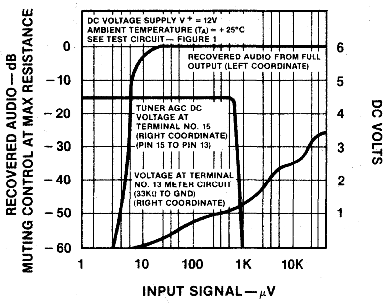
1. Waller 4SN3FIC or equivalent
2. Murate SFG 10.7mA or equivalent
3. R_S will affect stability depending on circuit layout. To increase stability, R_S is decreased. Range of R_S is 330 to 50Ω, $R1 + R_S \leq 330Ω$
4. L tunes with 100pF (C) at 10.7MHz
   Q_O unloaded ≅ 75 (G.I. EX27825 or equivalent)

Performance data at $f_O = 96MHz$, $f_{mod} = 400Hz$, deviation = ± 74KHz:

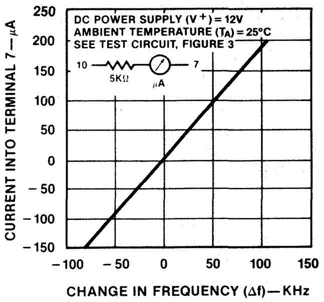
− 3dB limiting sensitivity	2μV (antenna level)
20dB quieting sensitivity	1μV (antenna level)
30dB quieting sensitivity	1.5μV (antenna level)

TYPICAL PERFORMANCE CHARACTERISTICS

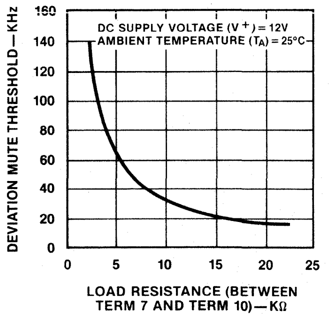
MUTING ACTION, TUNER AGC (Tuning Meter Output as a Function of Input Signal Voltage)



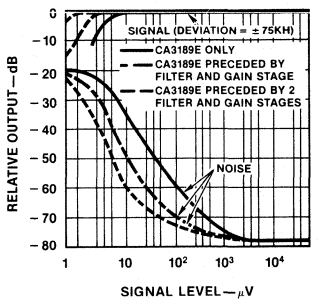
AFC CHARACTERISTICS (Current at Terminal 7 as a Function of Change in Frequency)



DEV MUTE THRESHOLD VS LOAD RESISTANCE

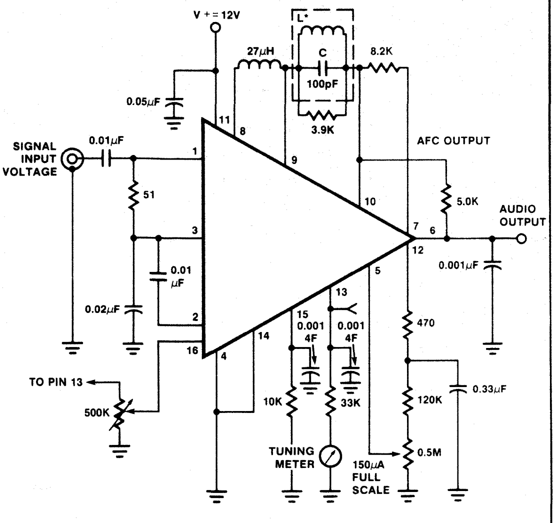


TYPICAL LIMITING AND NOISE CHARACTERISTICS



TEST CIRCUITS

TEST CIRCUIT
(Using a Single-Tuned Detector Coil)



NOTES

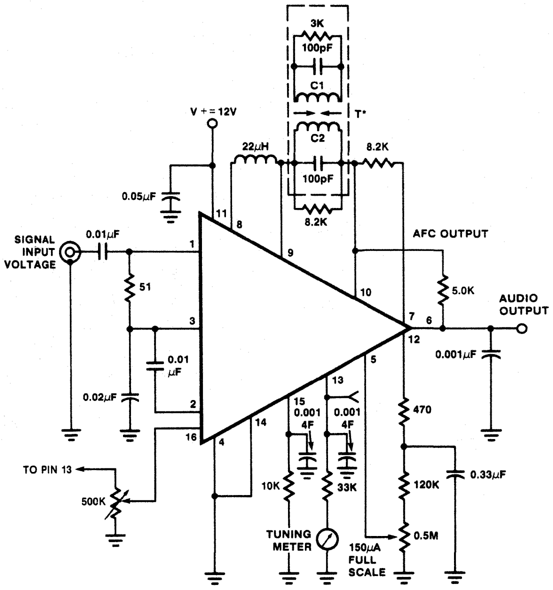
*L tunes with 100pF (C) at 10.7MHz.

All resistor values are typical and in ohms.

Q_O(unloaded) ≅ 75 (G.I. automatic mfg. div. EX27825 or equivalent).

Figure 2

TEST CIRCUIT
(Using a Double-Tuned Detector Coil)



NOTES

All resistor values are typical and in ohms.

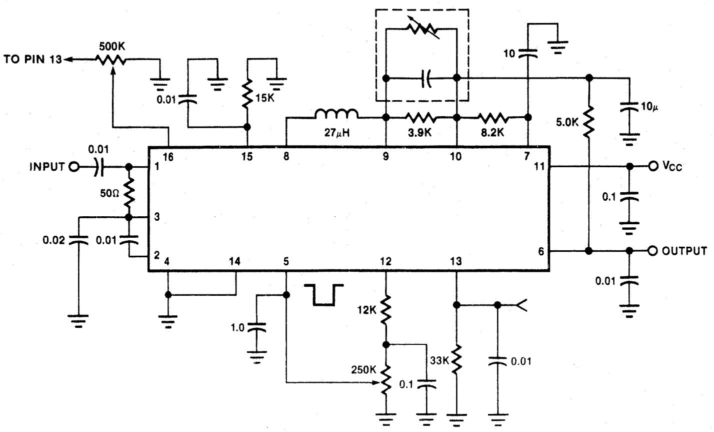
T: Pri.—Q_O (unloaded) ≅ 75 (tunes with 100pF (C1) 20 † of 34e on 7/32″ dia. form).
Sec.—Q_O (unloaded) ≅ 75 (tunes with 100pF (C2) 20 † of 34e on 7/32″ dia. form).
kQ (percent of critical coupling) > 70%.
(Adjusted for coil voltage V_C) = 150mV.

Above values permit proper operation of mute (squelch) circuit "E" type slugs, spacing 4mm.

Figure 4

TEST CIRCUITS

CA3189 TEST CIRCUIT



All capacitors in µf

Figure 3

STEREO DEMODULATOR WITH BLEND LM1870

DESCRIPTION

The LM1870 combination FM Stereo Demodulator and Blend Circuit is a PLL circuit with a D.C. control pin whose purpose is to reduce switching noise by decreasing separation under low signal amplitude conditions. The part is designed specifically for automobile applications where fluctuating signal strength can cause demodulation noise.

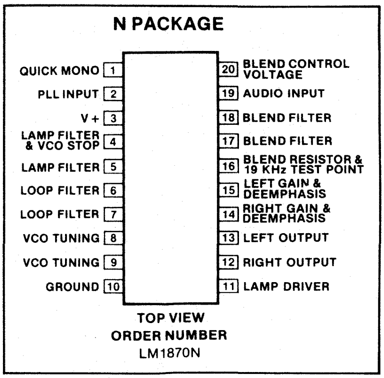
FEATURES

- **Stereo blend control**
- **Wide input dynamic range**
- **Low total harmonic distortion**
- **VCO disable function**
- **Monophonic override pin**
- **Supply range 7V-15V**

APPLICATIONS

- **Auto radios**
- **High fidelity tuners**
- **High performance portable radios**
- **Electronic tuned radios**

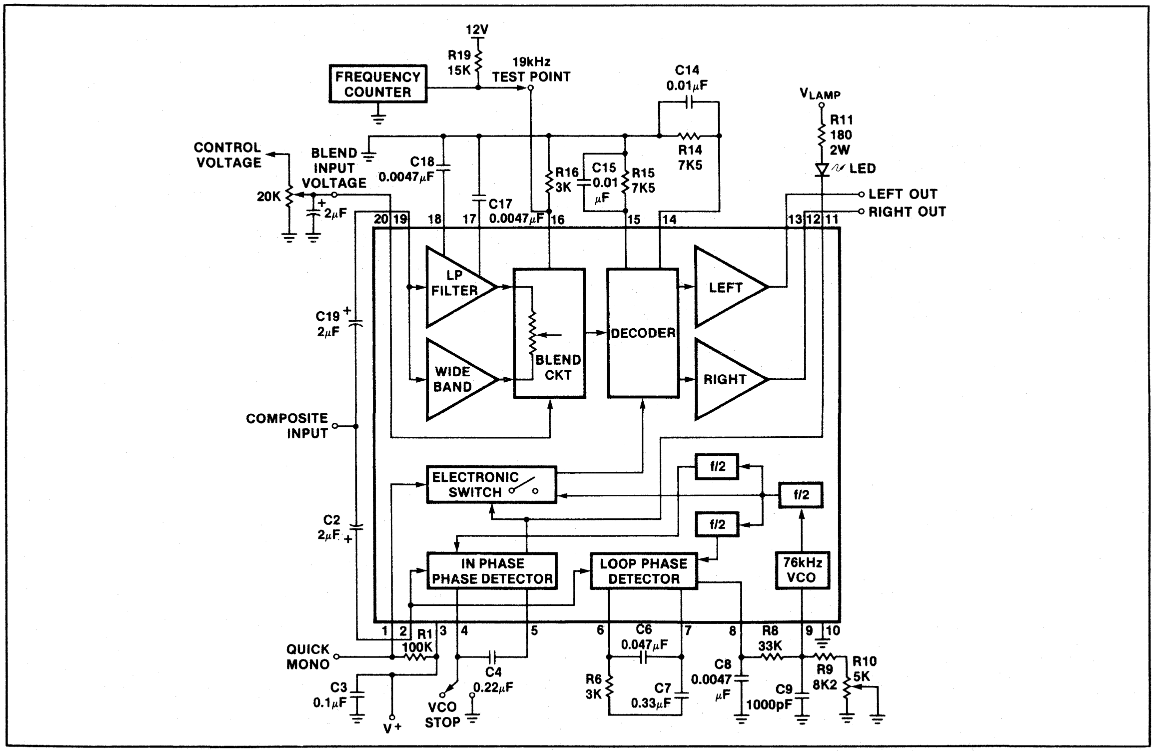
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage, pin 3	15	V
Lamp driver voltage, pin 11	18	V
Output voltage, pin 12, 13 supply off	7	V
Quick mono input (pin 20)	V+ (pin 3)	
Blend input (pin 20)	15	V
Operating temperature range	0°C to +70°C	
Power dissipation (note 1)	1	W
Storage temperature	−65°C to +125°C	
Lead temperature (soldering, 10 seconds)	300°C	

TYPICAL APPLICATION AND TEST CIRCUIT



STEREO DEMODULATOR WITH BLEND

LM1870

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V^+ = 8V$ unless otherwise noted (Figure 1)

SYMBOL AND PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating supply voltage		7	8	15	V
Supply current			26	45	mA
Input DC voltage	Pin 19		4		V
Input DC voltage	Pin 2		1.8		V
Supply rejection		15	30		dB
Lamp leakage current	Lamp off, pin 11 = 16V		0.1	100	μA
Lamp saturation voltage	Lamp on, pin 11 @ 75mA		1.4	2.0	V
VCO stop voltage	Voltage @ pin 4 to stop VCO	0.2	0.4		V
VCO stop current	Pin 4 = 0.2V		– 30	– 100	μA
Blend input bias current			– 2	– 20	μA
Quick mono switch voltage			4		V
Quick mono bias current	Pin 1 = 8V		2		μA
Output leakage	Pin 12 or 13 = 6.5V, pin 3 = 0V		0.1	20	μA

AUDIO ELECTRICAL CHARACTERISTICS

SYMBOL AND PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Mono gain	1kHz	– 4	– 1	+ 2	dB
Mono THD	1kHz @ 200mVrms		0.05	0.25	%
Channel balance			± 0.4	± 1.5	dB
Gain shift	Mono to stereo		± 0.1	± 1.0	dB
Channel separation	Pin 20 ≥ 1.1V	30	45		dB
Output DC shift	Mono to stereo		± 15	± 100	mV
Input resistance	Pin 19	20	40		kΩ
Output resistance	Pin 12, 13		65	200	Ω
Ultrasonic rejection	19kHz + 38kHz		30		dB
SCA rejection	(Note 2)		70		dB
Signal to noise	1kHz @ 200mVrms MONO		68		dB

PLL ELECTRICAL CHARACTERISTICS

SYMBOL AND PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Lamp ON voltage	19kHz on pin 2		15	20	mV
Lamp OFF voltage	19kHz on pin 2	2.5	5		mV
Lamp hysteresis			10		dB
Capture range	25mVrms on pin 2	± 2	± 4	± 6	%
Hold in range	25mVrms on pin 2		± 12		%
Input resistance	Pin 2	8	14		kΩ

STEREO DEMODULATOR WITH BLEND LM1870

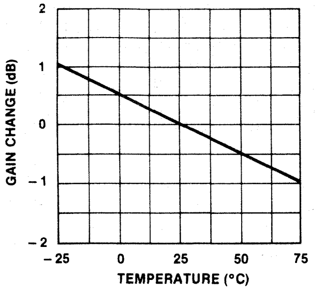
BLEND ELECTRICAL CHARACTERISTICS

SYMBOL AND PARAMETER	TEST CONDITIONS (Pin 20 from 1.1V to 0.2V)	MIN	TYP	MAX	UNIT
Stereo gain change	1kHz L = − R input	− 25	− 35		dB
Mono gain change	1kHz L = R input 10kHz L = R input	− 1.5 − 8	− 0.5 − 14	0.5 − 20	dB dB
Output DC shift			± 40	± 100	mV

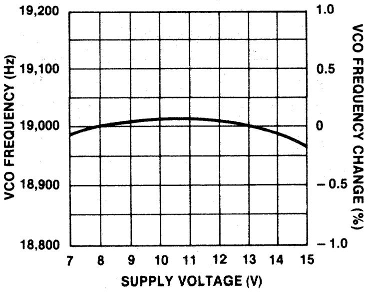
NOTES

1. For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 125°C/W junction to ambient.
2. Input is 10% SCA (74.5kHz), 9% pilot and 1kHz left or right. Rejection is ratio of 1kHz output to 1.5kHz output.

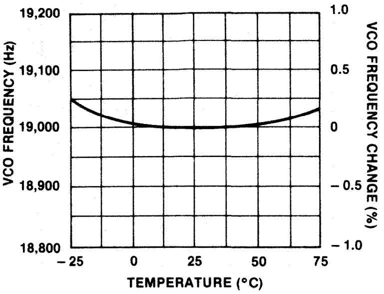
TYPICAL CHARACTERISTICS



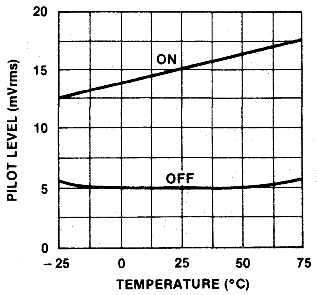
GAIN CHANGE vs TEMPERATURE



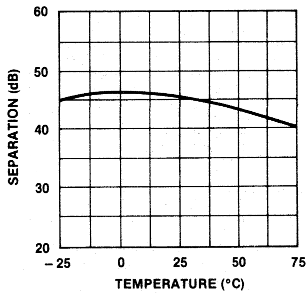
VCO SUPPLY SENSITIVITY



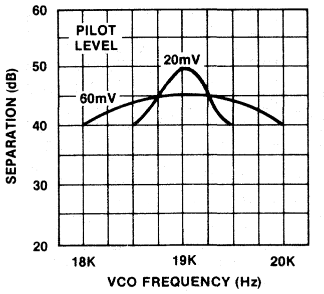
VCO TEMPERATURE STABILITY



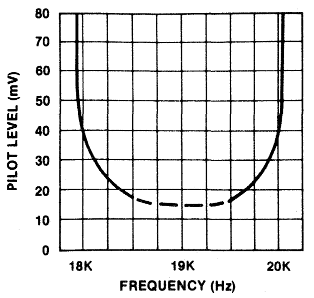
LAMP ON/OFF vs TEMPERATURE



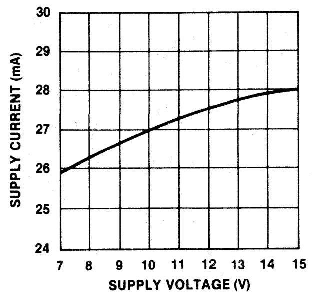
SEPARATION vs TEMPERATURE



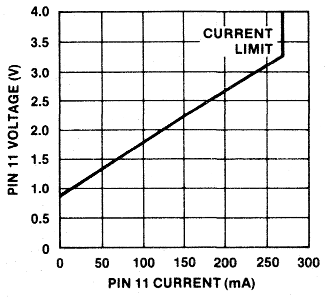
SEPARATION vs VCO TUNING



CAPTURE RANGE vs PILOT LEVEL



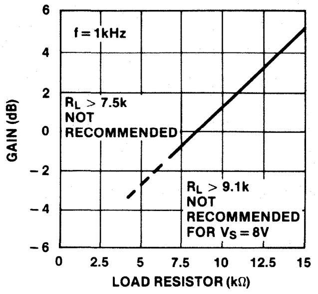
SUPPLY CURRENT vs SUPPLY VOLTAGE



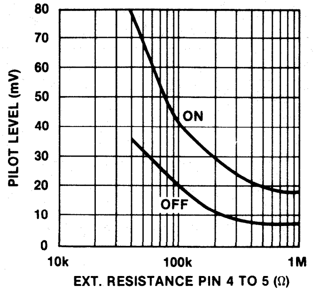
LAMP DRIVER VOLTAGE vs CURRENT

STEREO DEMODULATOR WITH BLEND LM1870

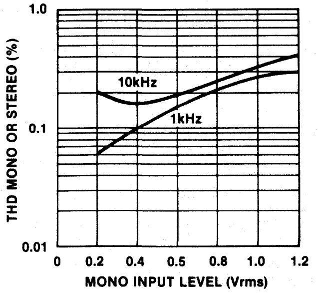
GAIN vs R_L (PIN 14, 15)



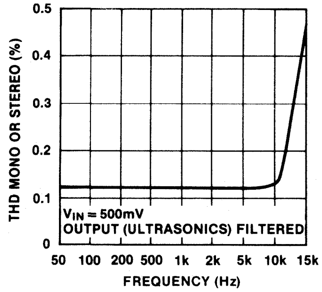
LAMP ON/OFF vs RESISTANCE PIN 4 TO 5



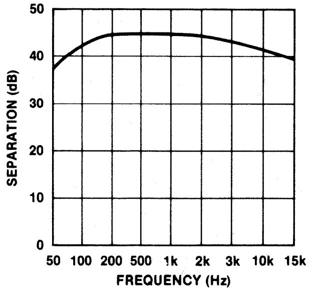
TOTAL HARMONIC DISTORTION vs INPUT LEVEL



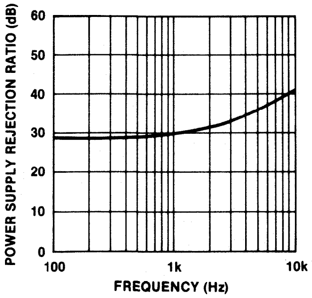
TOTAL HARMONIC DISTORTION vs FREQUENCY



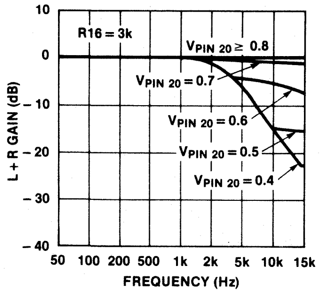
SEPARATION vs FREQUENCY



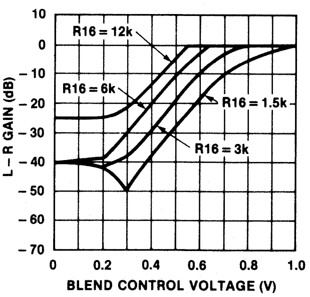
POWER SUPPLY REJECTION RATIO vs FREQUENCY



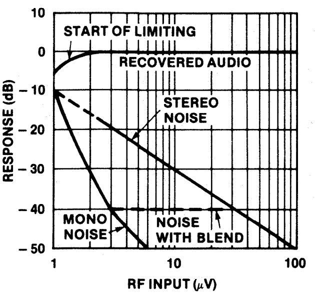
L + R FREQUENCY RESPONSE WITH BLEND CONTROL



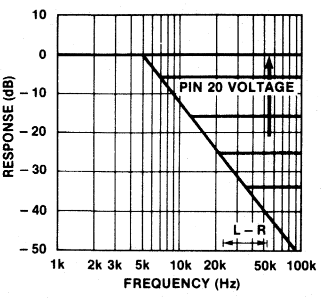
L − R GAIN vs BLEND CONTROL



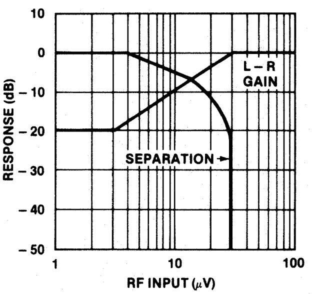
TYPICAL RADIO QUIETING CHARACTERISTIC



BLEND FILTER RESPONSE



L − R GAIN AND SEPARATION vs RF INPUT LEVEL WITH BLEND



BALANCED MODULATOR-DEMODULATOR MC1496/MC1596

DESCRIPTION

The MC1496 is a monolithic Double-Balanced Modulator/Demodulator designed for use where the output voltage is a product of an input voltage (signal) and a switched function (carrier). The MC1596 will operate over the full military temperature range of -55°C to +125°C. The MC 1496 is intended for applications within the range of 0°C to +70°C.

FEATURES

- **Excellent carrier suppression**
  - **65dB typ @ 0.5MHz**
  - **50dB typ @ 10MHz**
- **Adjustable gain and signal handling**
- **Balanced inputs and outputs**
- **High common-mode rejection—85dB typ**

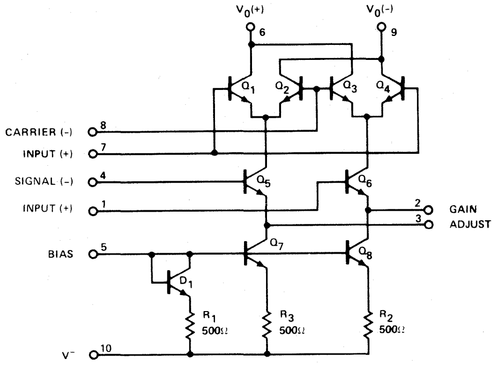
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Applied voltage[1,2]	30	V
Differential input signal (V_7-V_8)	±5.0	V
Differential input signal (V_4-V_1)	$(5 \pm I_5 R_e)$	V
Input signal (V_2-V_1, V_3-V_4)	5.0	V
Bias current (I_5)	10	mA
Power dissipation (pkg. limitation)		
N package	900	mW
Operating temperature range		
MC1496	0 to +70	°C
MC1596	-55 to +125	°C
Storage temperature range	-65 to +150	°C

NOTES

1. Voltage applied between pins 6-7, 8-1, 9-7, 9-8, 7-4, 7-1, 8-4, 6-8, 2-5, 3-5.
2. Pin number references pertain to H package pinout only.

EQUIVALENT SCHEMATIC



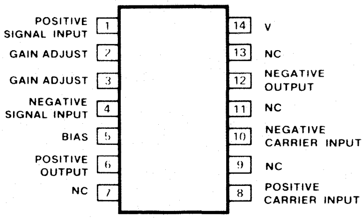
(Pinout for H pkg. shown)

APPLICATIONS

- **Suppressed carrier and amplitude modulation**
- **Synchronous detection**
- **FM detection**
- **Phase detection**
- **Sampling**
- **Single sideband**
- **Frequency doubling**

PIN CONFIGURATIONS

F, N PACKAGE

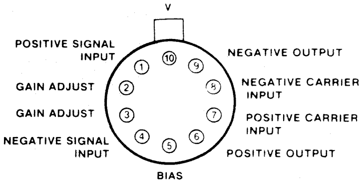


TOP VIEW

ORDER NUMBERS

MC1496F,N MC1596F

H PACKAGE



ORDER NUMBERS

MC1496H MC1596H

*Metal cans (H) not recommended for new designs

BALANCED MODULATOR-DEMODULATOR MC1496/MC1596

DC ELECTRICAL CHARACTERISTICS

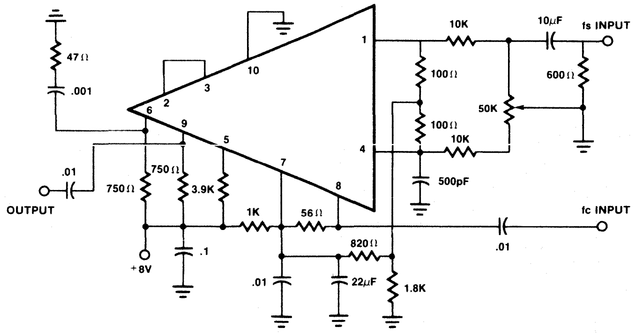
$V^+ = +12Vdc$, $V^- = -8.0Vdc$, $I_5 = 1.0mAdc$, $R_L = 3.9k\Omega$, $R_e = 1.0k\Omega$, $T_A = 25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	MC1596			MC1496			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Single-ended input impedance	Signal port, f = 5.0MHz							
R_{ip}	Parallel input resistance			200			200		kΩ
C_{ip}	Parallel input capacitance			2.0			2.0		pF
	Single-ended output impedance	f = 10MHz							
R_{op}	Parallel output resistance			40			40		kΩ
C_{op}	Parallel output capacitance			5.0			5.0		pF
	Input bias current								μA
I_{bS}	$I_{bS} = \frac{I_1 + I_4}{2}$			12	25		12	30	
I_{bC}	$I_{bS} = \frac{I_7 + I_8}{2}$			12	25		12	30	μA
	Input offset current								μA
I_{ioS}	$I_{ioS} = I_1 - I_4$			0.7	5.0		0.7	7.0	
I_{ioC}	$I_{ioC} = I_7 - I_8$			0.7	5.0		0.7	7.0	μA
$T_{cI_{io}}$	Average temperature coefficient of input offset current			2.0			2.0		nA/°C
	Output offset current								
I_{oo}	$I_6 - I_9$			14	50		15	80	μA
$T_{cI_{oo}}$	Average temperature coefficient of output offset current			90			90		nA/°C
V_o	Common-mode quiescent Output voltage (Pin 6 or Pin 9)			8.0			8.0		Vdc
	Power supply current								mAdc
I_{D+}	$I_6 + I_9$			2.0	3.0		2.0	4.0	
I_{D-}	I_{10}			3.0	4.0		3.0	5.0	
P_D	DC power dissipation			33			33		mW

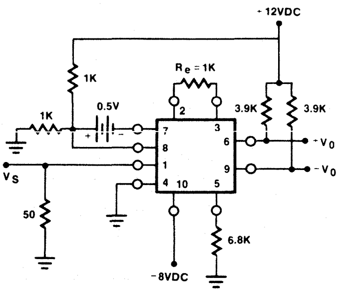
NOTE

Pin number references pertain to H package pinout only.

CARRIER REJECTION AND SUPPRESSION



SIGNAL GAIN AND OUTPUT SWING



BALANCED MODULATOR-DEMODULATOR MC1496/MC1596

AC ELECTRICAL CHARACTERISTICS

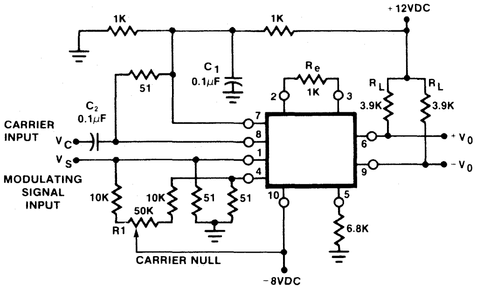
$V^+ = +12Vdc$, $V^- = -9.0Vdc$, $I_5 = 1.0mAdc$, $R_L = 3.9k\Omega$, $R_e = 1.0k\Omega$, $T_A = +25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	MC1596			MC1496			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CFT}	Carrier feedthrough	V_c = 60mVrms sinewave and offset adjusted to zero							
		f_C = 1.0kHz		40			40		µVrms
		f_C = 10MHz		140			140		
		V_c = 300mVp-p squarewave:							
		Offset adjusted to zero f_C = 1.0kHz		0.04	0.2		0.04	0.4	mVrms
		Offset not adjusted f_C = 1.0kHz		20	100		20	200	
V_{CS}	Carrier suppressions	f_S = 10kHz, 300mVrms sinewave							
		f_C = 500kHz, 60mVrms sinewave	50	65		40	65		dB
		f_C = 10MHz, 60mVrms sinewave		50			50		
BW_{3dB}	Transadmittance bandwidth (Magnitude) ($R_L = 50\Omega$)	Carrier input port, V_C = 60mVrms sinewave f_S = 1.0kHz, 300mVrms sinewave		300			300		MHz
		Signal input port, V_S = 300mVrms sinewave $\lvert V_C \rvert$ = 0.5Vdc		80			80		MHz
AV_S	Signal gain	V_S = 100mVrms; f = 1.0kHz $\lvert V_C \rvert$ = 0.5Vdc	2.5	3.5		2.5	3.5		V/V
CMV	Common-mode input swing	Signal port, f_s = 1.0kHz		5.0			5.0		Vp-p
ACM	Common-mode gain	Signal port, f_S = 1.0kHz $\lvert V_C \rvert$ = 0.5Vdc		-85			-85		dB
DV_{OUT}	Differential output voltage swing capability			8.0			8.0		Vp-p

NOTE

Pin number references pertain to H package pinout only.

CARRIER REJECTION AND SUPPRESSION



AM RECEIVER CIRCUIT

TCA440

DESCRIPTION

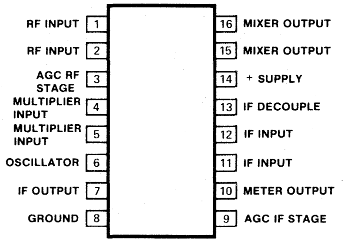
TCA440 is a monolithic IC, especially developed for AM receivers up to 30MHz. It includes a RF stage with AGC, a balanced mixer, separate oscillator and an IF amplifier with AGC. Because of its low current consumption and of its internal stabilization the TCA440 is perfectly suited for battery operated portables, car and home radios.

FEATURES

- **Balanced circuit**
- **Separately controllable prestage**
- **Multiplicative push-pull mixer with separate oscillator**
- **High signal handling capability even with 4.5V supply voltage**
- **100dB feedback control range in 5 stages**
- **Direct connection for tuning meter**
- **Minimum external components**

PIN CONFIGURATION

N PACKAGE



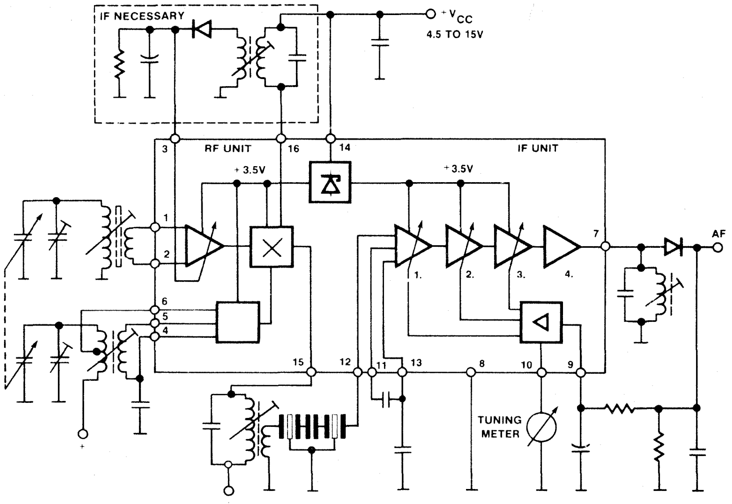
TOP VIEW

ORDER NUMBER
TCA440N

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	15	V
T_{amb}	Ambient temperature in operation	-15 to +80	°C
T_s	Storage temperature	-30 to +125	°C
V_{CC}	Range of operation	4.5 to 15	V

BLOCK DIAGRAM



TUNING METER

Recommended instruments:

or $500\mu A$ ($R_1 = 800\Omega$)
$300\mu A$ ($R_1 = 1.5k\Omega$)

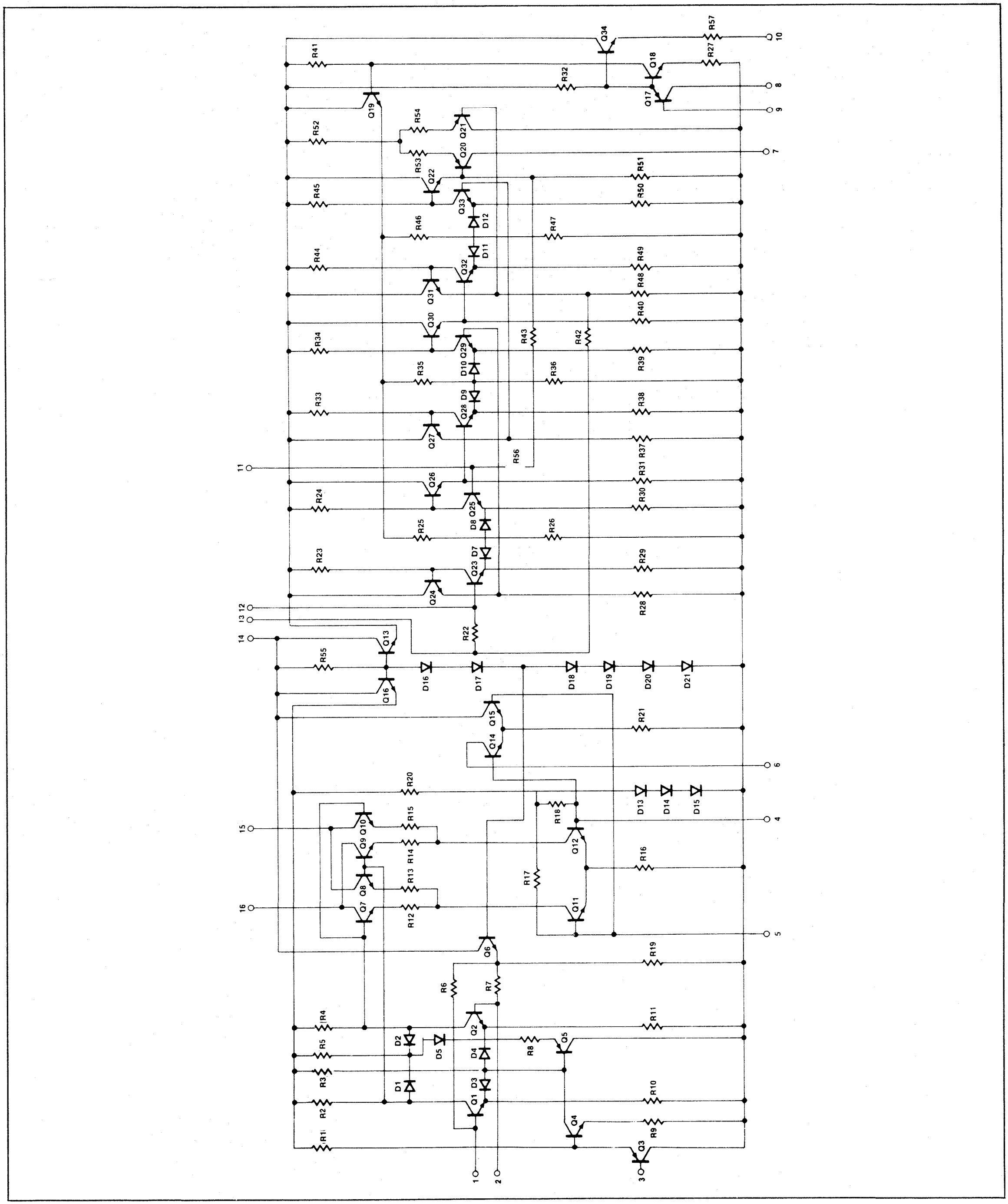
The IC offers at pin 10 a tuning meter voltage of 600 mV_{EMP} max. with a source impedance of approx. 400Ω.

FUNCTION

As pictured in the circuit diagram the TCA440 comprises two control loops independent of each other which control the RF stage and the IF stages. By AGCing the RF stage, excellent signal handling is obtained. A voltage of $2.6V_{pp}$ on the IC input can be handled with very low distortion. The push-pull mixer operates multiplicatively, thereby resulting in few harmonic mixing products and whistling points. The oscillator which is separated from the mixer is also apted excellently for short waves. From the AGC of the RF amplifier a voltage is derived for a tuning meter which can be connected directly to the meter. The symmetric composition of the circuit provides high stability against oscillation and, at the same time, an AGC range of more than 100dB. The bridge circuit of the mixer provides good isolation of the oscillator.

AM RECEIVER CIRCUIT TCA440

EQUIVALENT SCHEMATIC



AM RECEIVER CIRCUIT
TCA440

DC ELECTRICAL CHARACTERISTICS V_{CC} = 9V, T_A = 25°C unless otherwise specified.

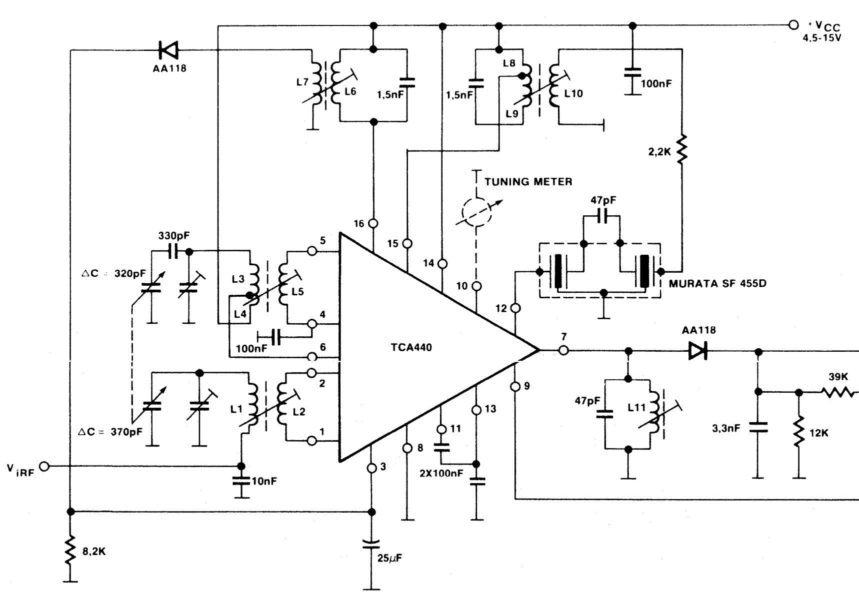
PARAMETER		TEST CONDITIONS	TCA 440			UNIT
			Min	Typ	Max	
I_{CC}	Total current consumption at:	V_{CC} = 4.5V V_{CC} = 9V V_{CC} = 15V		7 10.5 12		mA mA mA

AC ELECTRICAL TEST V_{CC} = 9V, T_A = 25°C, f_C = 1MHz, f_{MOD} = 1kHz unless otherwise specified.

PARAMETER		TEST CONDITIONS	TCA 440			UNIT
			Min	Typ	Max	
V_O	Audio output voltage	m = 30% V_{IN} = 1.0mV		100		mV
SEN	Input sensitivity (f_C = 1MHz, m = 30%/0%, R_G = 540Ω)	V_O = 30mV		10		μV
	Noise	V_{IN} = 1.0mV NO MOD.		1.5		mV
M_O	Meter Output	V_{IN} = 4μV		150		μV

TYPICAL APPLICATIONS

APPLICATION EXAMPLE FOR BROADCAST BAND



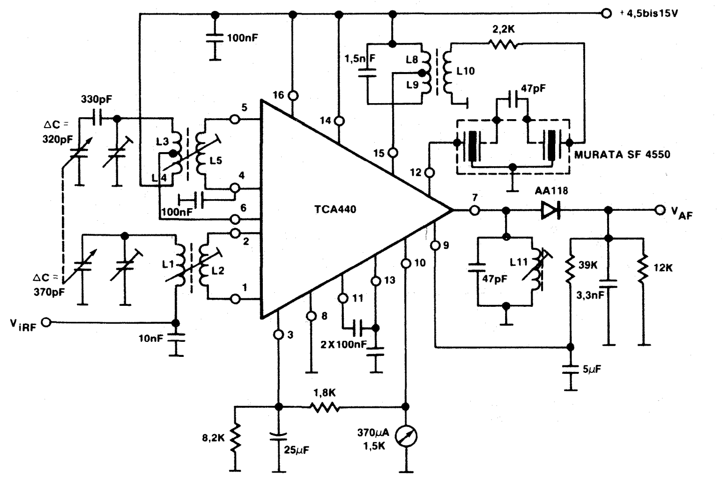
L1-L2 with V_{ogt} coil set D21-2375.1
L3-L1 with V_{ogt} coil set D41-2519

L1	105 turns	12 x 0.04 CuLS
L2	7 turns	0.10 CuL
L3	80 turns	12 x 0.04 CuLS
L4	35 turns	12 x 0.04 CuLS
L5	15 turns	0.10 CuL
L6	70 turns	12 x 0.04 CuLS
L7	35 turns	12 x 0.04 CuLS
L8	20 turns	12 x 0.04 CuLS
L9	50 turns	12 x 0.04 CuLS
L10	22 turns	12 x 0.04 CuLS
L11	400 turns	0.06 CuL

AM RECEIVER CIRCUIT TCA440

TYPICAL APPLICATIONS (Cont'd)

APPLICATION EXAMPLE FOR BROADCAST BAND

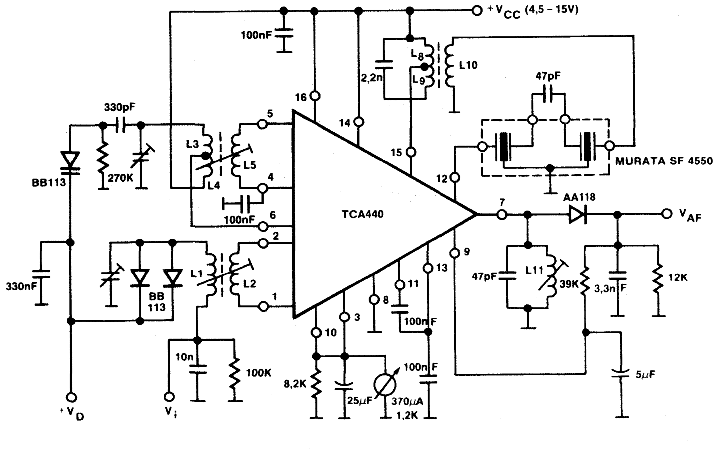


Prestage control is derived from IF control

L1	105 turns	12 x 0.04 CuLS
L2	7 turns	0.10 CuL
L3	80 turns	12 x 0.04 CuLS
L4	35 turns	12 x 0.04 CuLS
L5	15 turns	0.10 CuL
L8	20 turns	12 x 0.04 CuLS
L9	50 turns	12 x 0.04 CuLS
L10	22 turns	12 x 0.04 CuLS
L11	400 turns	0.04 CuL

L1-L2 with V_{ogt} coil set D21-23751
L3-L11 with V_{ogt} coil set D41-2519

APPLICATION EXAMPLE FOR AM USING VARICAP DIODES BB 113



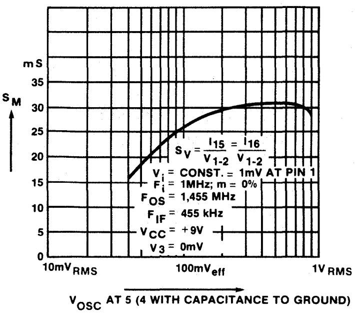
L1	105 turns	12 x 0.04 CuLS
L2	7 turns	0.10 CuL
L3	80 turns	12 x 0.04 CuLS
L4	35 turns	12 x 0.04 CuLS
L5	15 turns	0.10 CuL
L8	20 turns	12 x 0.04 CuLS
L9	50 turns	12 x 0.04 CuLS
L10	22 turns	12 x 0.04 CuLS
L11	400 turns	0.06 CuL

L1-L2 with Vogt coil set D21-23751
L3-L11 with Vogt coil set D41-2519

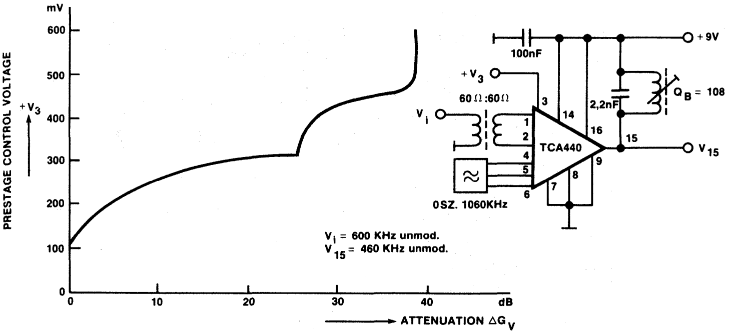
$V_D = 8.5V \rightarrow f_i = 800kHz$
$V_D = 30V \rightarrow f_i = 1620kHz$

TYPICAL APPLICATIONS (Cont'd)

CONVERSION CONDUCTANCE vs OSCILLATOR VOLTAGE

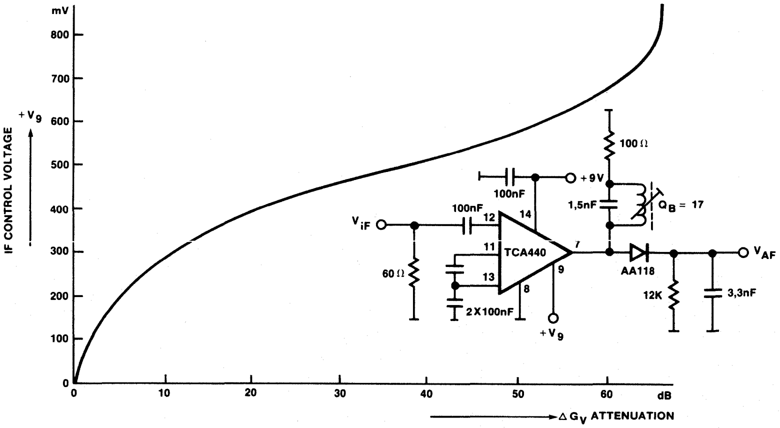


RF STAGE CONTROL



The input is not power matched and can be driven with a higher resistance, V_i is chosen so that a constant V_{15} is obtained ($50mV_{pp}$).

IF CONTROL

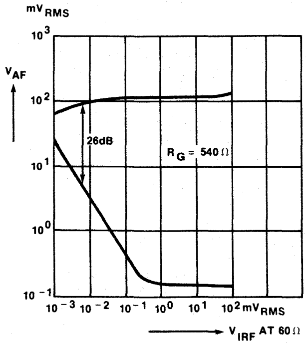


V_{IF} (469kHz; m = 80%; f_{mod} = 1kHz) is chosen so that always a constant V_{AF} is obtained ($200mV_{RMS}$)

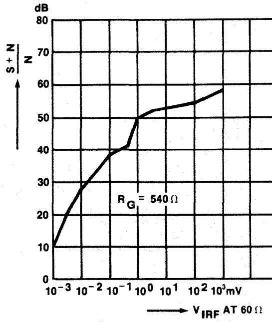
AM RECEIVER CIRCUIT TCA440

TYPICAL PERFORMANCE CHARACTERISTICS

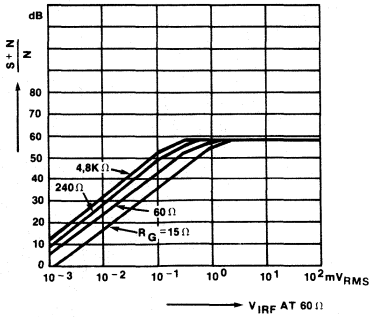
AF OUTPUT VOLTAGE AND NOISE FIGURE vs RF INPUT VOLTAGE (switching position 1)



SIGNAL TO NOISE RATIO vs RF INPUT VOLTAGE (switching position 2)



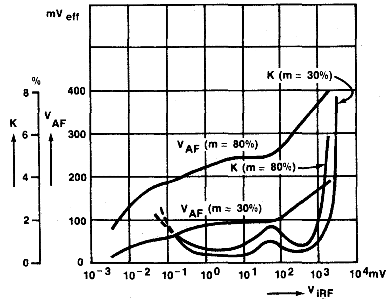
SIGNAL TO NOISE RATIO vs RF INPUT VOLTAGE (parameter is generator impedance) (switching position 1)

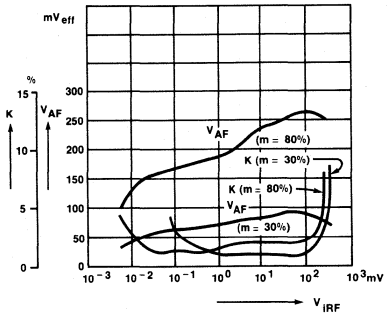


TEST FIGURES FOR APPLICATION EXAMPLE FOR AM USING BB 113

f_i = 1MHz, f_{mod} = 1kHz, f_{IF} = 455 kHz,
V_{CC} = 9V, V_{IRF} measured symmetrically at pins 1 and 2

TEST FIGURES FOR APPLICATION EXAMPLE FOR MW HARMONIC DISTORTION AND AF OUTPUT VOLTAGE vs RF INPUT VOLTAGE MEASURED SYMMETRICALLY AT PINS 1 AND 2 f_i = 1MHz, f_{mod} = 1kHz, f_{IF} = 455kHz, V_{CC} = 9V



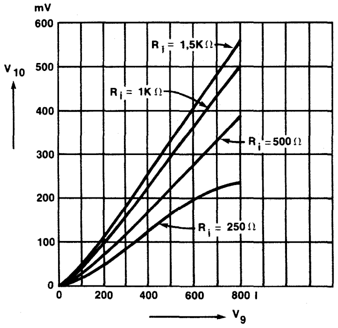


Example for moving coil instruments

Ri for full-scale deflection

1.5kΩ	100µA
1.5kΩ	170µA
2kΩ	200µA
350Ω	500µA

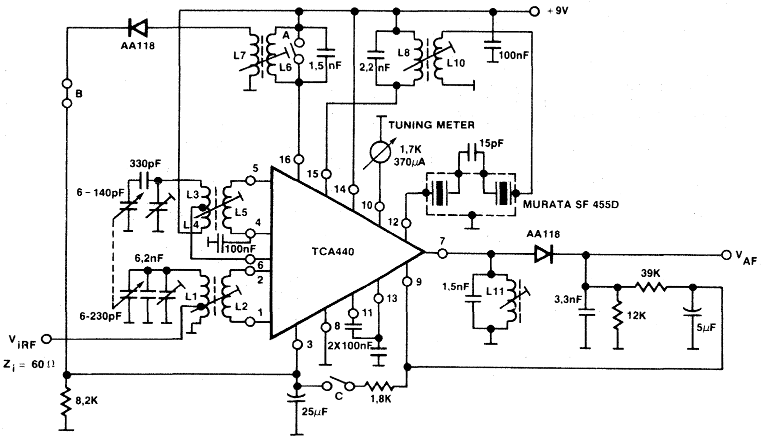
TUNING METER VOLTAGE vs IF CONTROL VOLTAGE (parameter is impedance of tuning meter)



AM RECEIVER CIRCUIT TCA440

TEST CIRCUITS

TEST CIRCUIT FOR NOISE FIGURE



L1-L2 M25 pot core
L3-L11 with Vogt coil set D41-2519

L1	2 + 6	turns	6 x 12 x 0.04 CuLS
L2	n		0.15 CuL
L3	90	turns	12 x 0.04 CuLS
L4	35	turns	12 x 0.04 CuLS
L5	15	turns	0.10 CuL
L6	70	turns	12 x 0.04 CuLS
L7	35	turns	12 x 0.04 CuLS
L8	60	turns	12 x 0.04 CuLS
L10	22	turns	12 x 0.04 CuLS
L11	68	turns	0.06 CuL

	switch		
A	B	C	
off	on	off	separate RF stage control
on	off	on	RF stage control voltage derived from IF control voltage

f_i = 1MHz; m = 30%

n(turns)	$R_{Generator}(\Omega)$
1	15
2	60
4	240
6	540
9	1,2K
12	2,2K
18	4,8K

FM STEREO MULTIPLEX DECODER, PHASE LOCKED LOOP µA758

DESCRIPTION

The µA758 is a monolithic phase-locked loop FM stereo multiplex decoder. The device decodes an FM stereo multiplex signal into right and left audio channels while inherently suppressing SCA information when it is contained in the composite input signal. The device includes automatic mono-stereo mode switching and drive for an external lamp to indicate stereo mode operation.

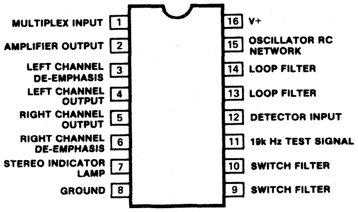
The µA758 operates over a large voltage range and requires a minimum number of extèrnal components. A simple setting of an external potentiometer adjusts the oscillator frequency. No coils are required.

FEATURES

- **45dB channel separation**
- **Automatic stereo/mono switching**
- **70dB SCA rejection**
- **10V to 16V supply range**
- **High impedance input—low impedance output**

PIN CONFIGURATION

N PACKAGE



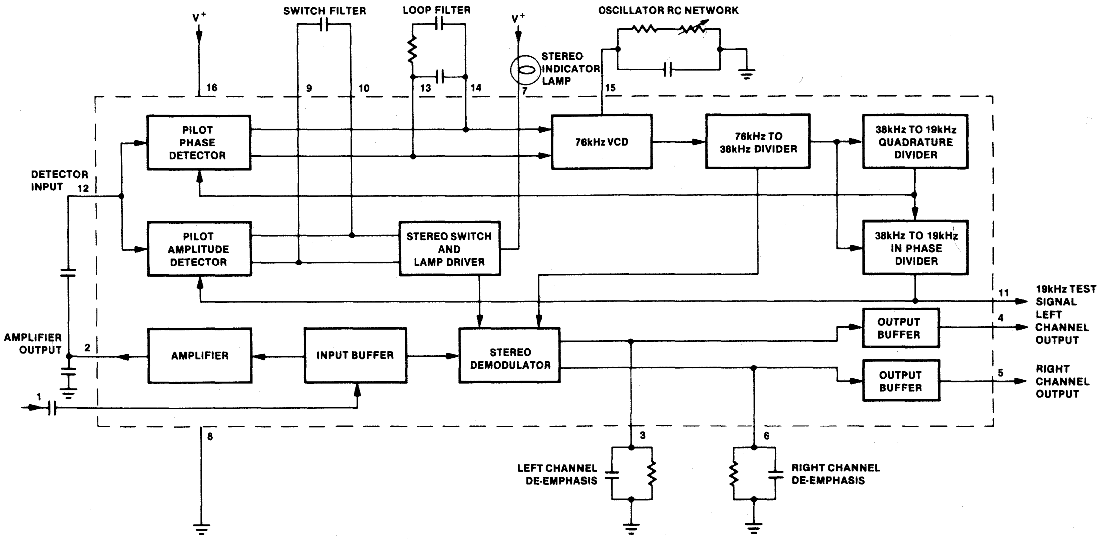
TOP VIEW

ORDER NUMBERS
µA758N

ABSOLUTE MAXIMUM RATINGS

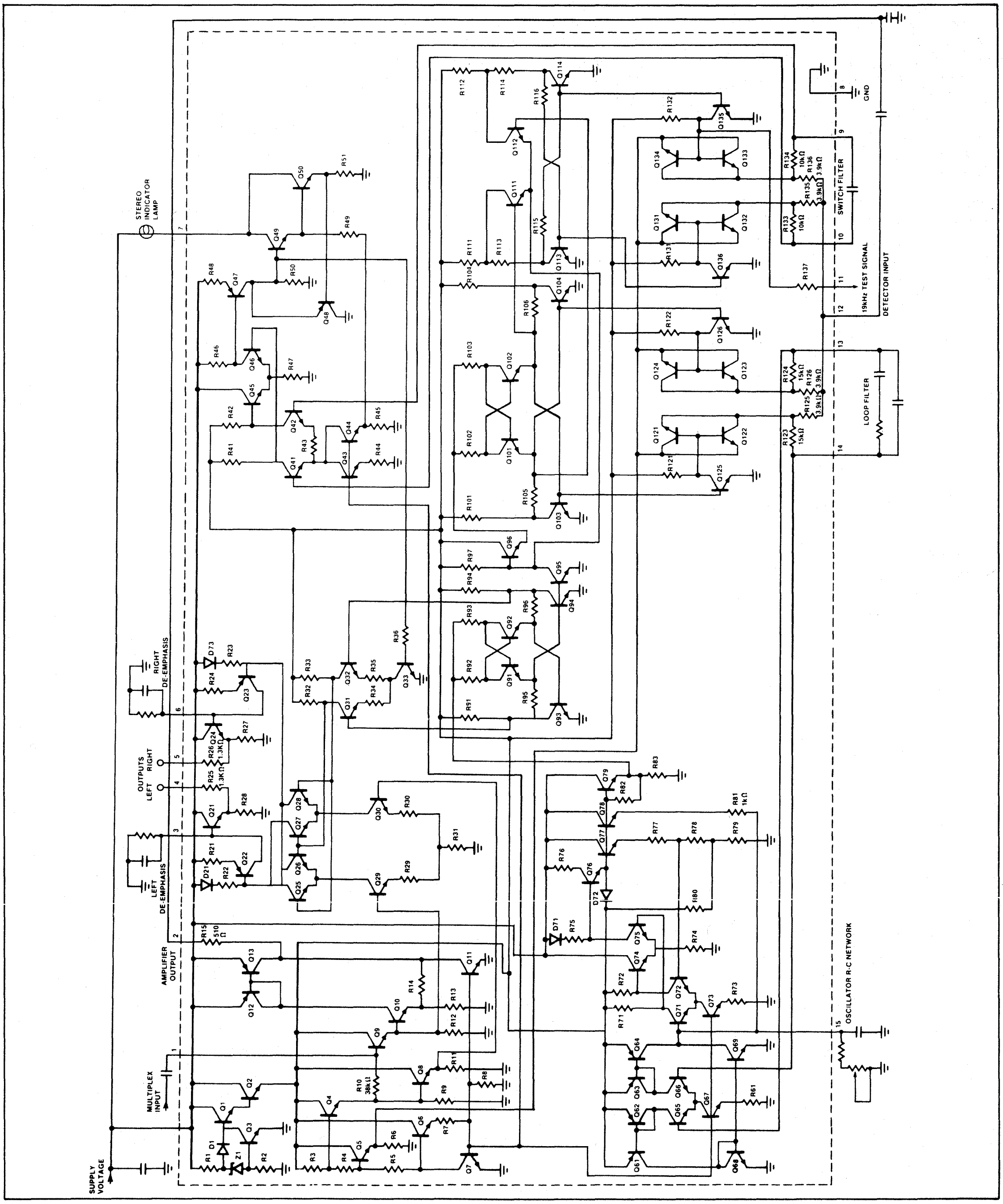
PARAMETER	RATING	UNIT
Supply voltage	+18	V
Supply voltage (≤ 15 seconds)	+22	V
Voltage at lamp driver terminal (Lamp OFF)	+22	V
Internal power dissipation	730	mW
Operating temperature range	-40 to +85	°C
Storage temperature range	-55 to +125	°C
Lead temperature (60sec)	300	°C

BLOCK DIAGRAM



FM STEREO MULTIPLEX DECODER, PHASE LOCKED LOOP μA758

EQUIVALENT SCHEMATIC



FM STEREO MULTIPLEX DECODER, PHASE LOCKED LOOP μA758

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V+ = +12V$, 19kHz pilot level = 30mV$_{RMS}$, multiplex signal (L = R, pilot OFF) = 300mV$_{RMS}$, modulation frequency = 400Hz or 1Hz, test circuit 1, unless otherwise specified.

PARAMETER		TEST CONDITIONS	μA758			UNIT
			Min	Typ	Max	
I_{CC}	Supply current	Lamp OFF		31	38	mA
I_L	Maximum available lamp current		75	150		mA
V_7	Voltage at lamp driver terminal	Lamp = 50mA		1.3	1.8	V
r_i	Input resistance		20	35		kΩ
r_o	Output resistance		0.9	1.3	2.0	kΩ

AC ELECTRICAL CHARACTERISTICS

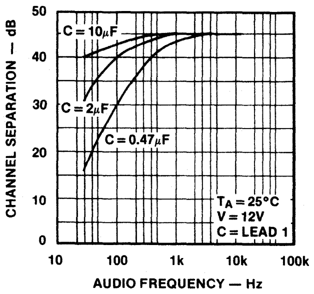
PARAMETER		TEST CONDITIONS	μA758			UNIT
			Min	Typ	Max	
$\Delta(V_4\&V_5)$	DC voltage shift at either output terminal	Stereo to mono operation		30	150	mV
$P_{S.R.R.}$	Power supply ripple rejection	200Hz, 200mV$_{RMS}$	35			dB
SEP	Channel separation	100Hz		40		dB
		400Hz	30	45		dB
		10kHz		45		dB
BAL.	Channel balance			0.3	1.5	dB
A_V	Voltage gain	1kHz	0.5	0.9	1.4	V/V
	Pilot input level	Lamp turn-on		18	25	mV$_{RMS}$
		Lamp turn-off	2.0	7.0		mV$_{RMS}$
	Pilot input level hysteresis	Lamp turn-off to turn-on	3.0	7.0		dB
	Capture range		2.0	4.0	6.0	%
T.H.D.	Total harmonic distortion	Multiplex level = 600mV$_{RMS}$ pilot OFF		0.4	1.0	%
	19kHz rejection		25	35		dB
	38kHz rejection		25	45		dB
	SCA rejection[1]			70		dB
VCO	Tuning resistance[2]		21.0	23.3	25.5	kΩ
VCO	Frequency drift	$0°C \leq T_A \leq 25°C$		+0.1	±2	%
		$25°C \leq T_A \leq 70°C$		-0.4	±2	%

NOTES

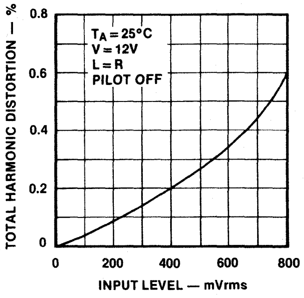
1. Measured with a stereo composite signal consistency of 80% stereo, 10% pilot and 10% SCA as defined in the FCC Rules on Broadcasting.
2. Total resistance from pin 15 to ground, in test circuit, required to set reference frequency at pin 11 to 19kHz ± 10hz.

TYPICAL PERFORMANCE CHARACTERISTICS

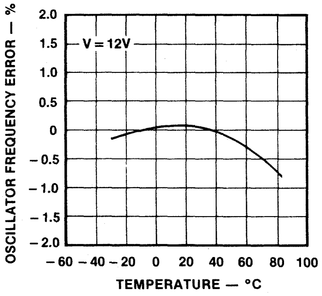
CHANNEL SEPARATION vs AUDIO FREQUENCY



HARMONIC DISTORTION vs INPUT LEVEL



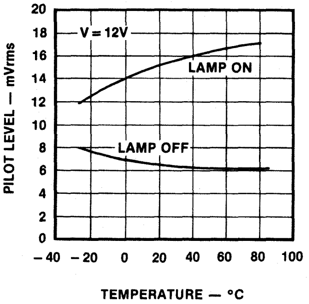
OSCILLATOR FREE RUNNING FREQUENCY ERROR vs AMBIENT TEMPERATURE



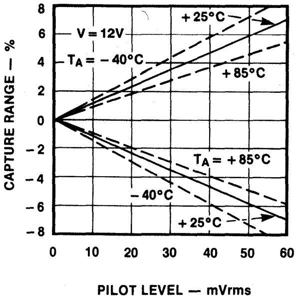
FM STEREO MULTIPLEX DECODER, PHASE LOCKED LOOP μA758

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

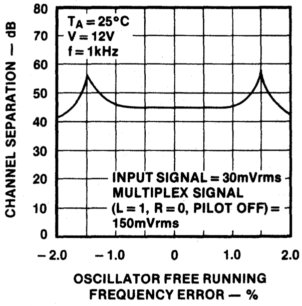
LAMP TURN ON & TURN OFF SENSITIVITY vs AMBIENT TEMPERATURE



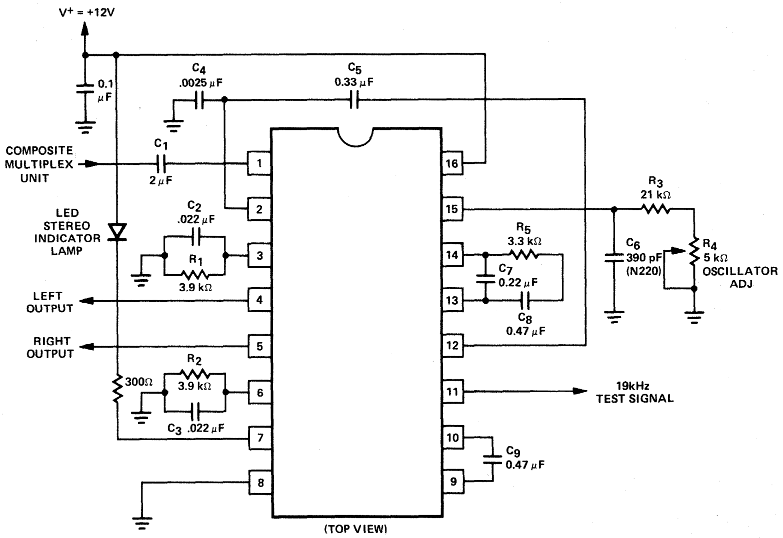
CAPTURE RANGES vs PILOT LEVEL



CHANNEL SEPARATION vs OSCILLATOR FREE RUNNING FREQUENCY ERROR



TEST CIRCUIT AND TYPICAL APPLICATION



NOTE

Tolerance on resistors is ±5% and tolerance on capacitors is ±20% unless otherwise specified. C_1 tolerance = +100%; -20%, C_6 tolerance = ±1% in test circuit and ±5% in typical applications, R_3 tolerance = ±1%, R_4 tolerance = ±10%, R_1 and R_2 tolerances = ±1% in test circuit and ±5% in typical application.

Section 15
Audio Circuits

INDEX

Section 15 — Audio Circuits

DUAL LOW-NOISE PREAMP LM387

DESCRIPTION

The LM387 is a dual preamplifier for the amplification of low level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with an internal power supply decoupler-regulator, providing 110dB supply rejection and 60dB channel separation. Other outstanding features include high gain (104dB), large output voltage swing (V_{CC} - 2V p-p), and wide power bandwidth (75kHz, 20V p-p). The LM387 operates from a single supply across the wide range of 9 to 40V.

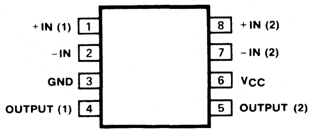
The amplifiers are internally compensated for all gains greater than 10. The LM387 is available in an 8 lead dual-in-line package.

FEATURES

- **Low noise—0.8μV total input noise**
- **High gain—104dB open loop**
- **Single supply operation**
- **Wide supply range 9 to 40V**
- **Power supply rejection—110dB**
- **Large output voltage swing (VCC - 2V p-p)**
- **Wide bandwidth 15MHz unity gain**
- **Power bandwidth 75kHz, 20V p-p**
- **Internally compensated**
- **Short circuit protected**

PIN CONFIGURATION

N PACKAGE

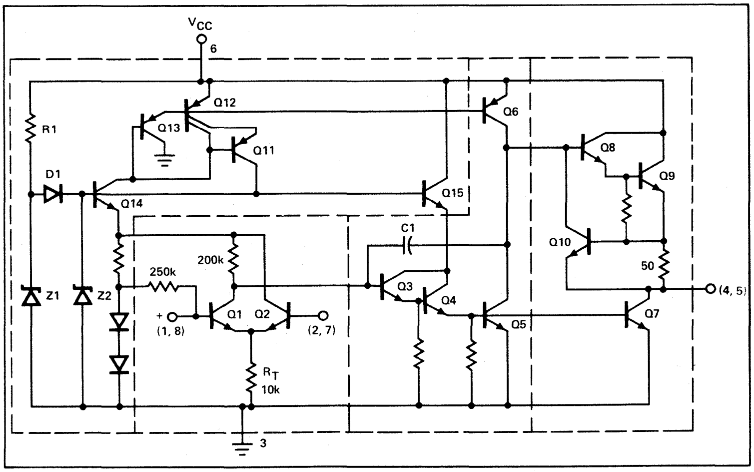


TOP VIEW
ORDER NUMBER
LM387N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	+40	V
Power dissipation	500	mW
Operating temperature range	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	+300	°C

EQUIVALENT CIRCUIT



DUAL LOW-NOISE PREAMP LM387

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = 14V$ unless otherwise specified.

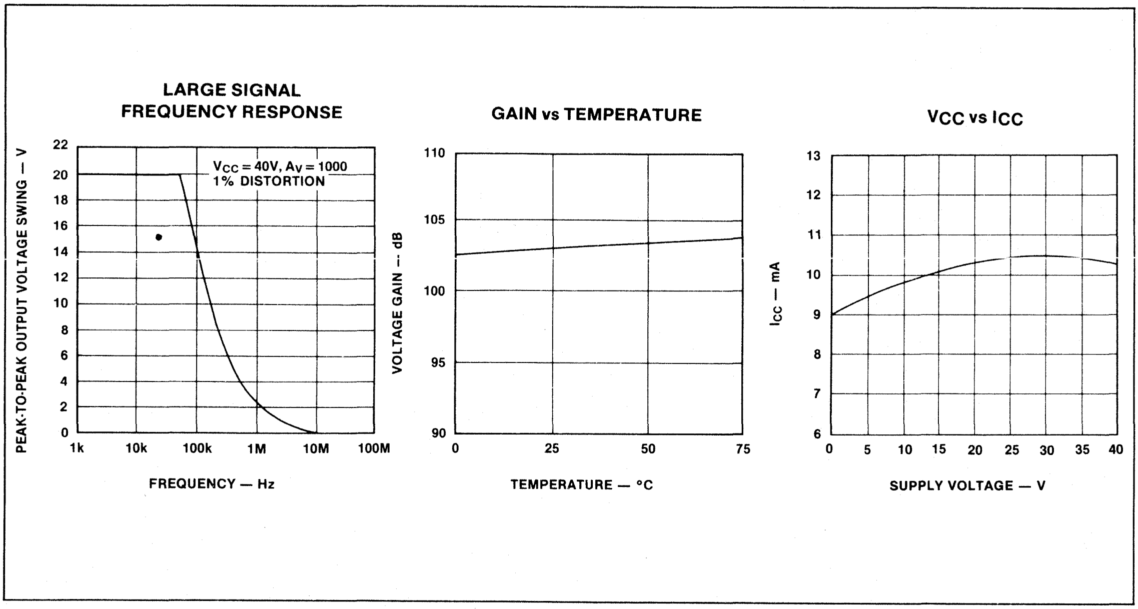
PARAMETER	TEST CONDITIONS	LM387			UNIT
		Min	Typ	Max	
Voltage gain	Open loop		160,000		V/V
Supply current	V_{CC} 9 to 40V, $R_L = \infty$		10		mA
Input resistance	Positive input		100		kΩ
	Negative input		200		kΩ
Input current	Negative input		0.5		μA
Output resistance	Open loop		150		Ω
Output current	Source		8		mA
	Sink		2		mA
Output voltage swing	Peak-to-peak		V_{CC}-2		V

AC ELECTRICAL CHARACTERISTICS

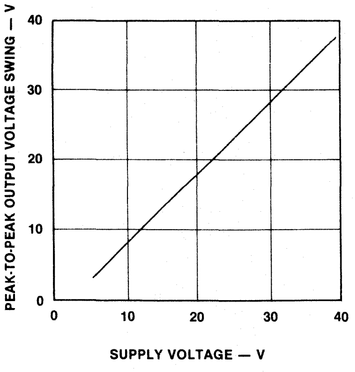
$T_A = 25°C$, $V_{CC} = 14V$ unless otherwise specified.

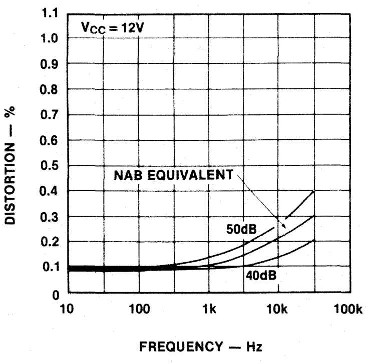
PARAMETER	TEST CONDITIONS	LM387			UNIT
		Min	Typ	Max	
Small signal bandwidth			15		MHz
Power bandwidth	20V p-p ($V_{CC} = 24V$)		75		kHz
Maximum input voltage	Linear operation			300	μVrms
Supply rejection ratio	f = 1kHz		110		dB
Channel separation	f = 1kHz		60		dB
Total harmonic distortion	75dB gain, f = 1kHz		0.1		%
Total equivalent input noise	$R_S = 600\Omega$, 100-10,000Hz		0.8	1.4	μVrms
Noise figure	50kΩ, 100-10,000Hz		1.0		dB
	10kΩ, 100-10,000Hz		1.6		dB
	5kΩ, 100-10,000Hz		2.8		dB

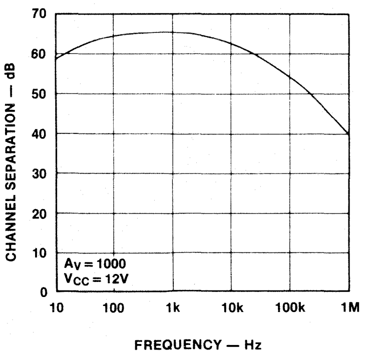
TYPICAL PERFORMANCE CHARACTERISTICS

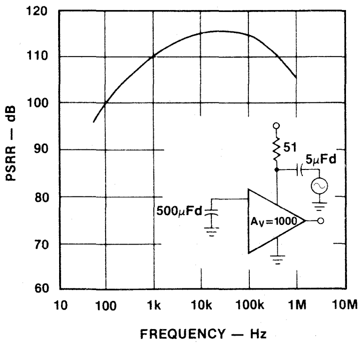


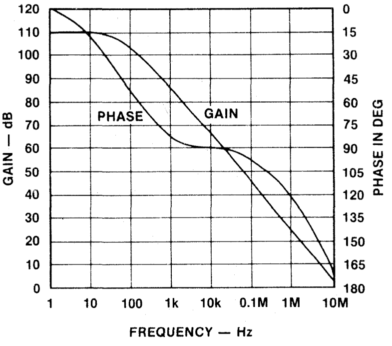
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

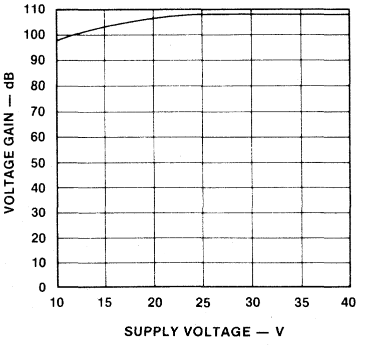

P-P OUTPUT VOLTAGE SWING vs V_{CC}

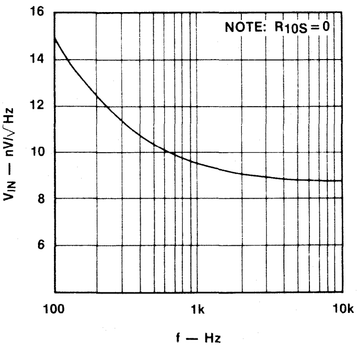

% DISTORTION

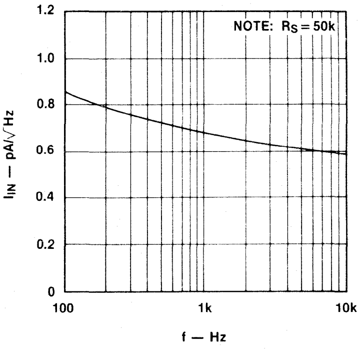

CHANNEL SEPARATION

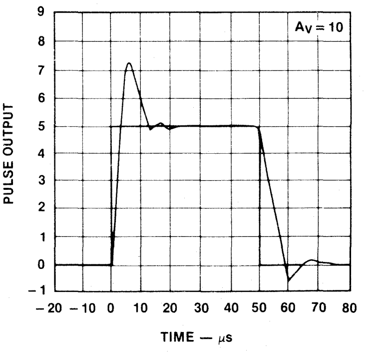

PSRR vs FREQUENCY


GAIN AND PHASE RESPONSE


VOLTAGE GAIN vs SUPPLY VOLTAGE


NOISE VOLTAGE vs FREQUENCY

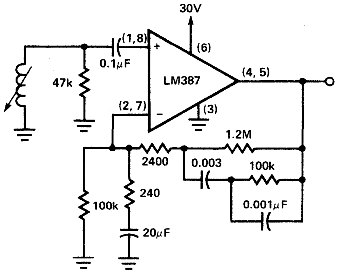

NOISE CURRENT vs FREQUENCY


PULSE RESPONSE

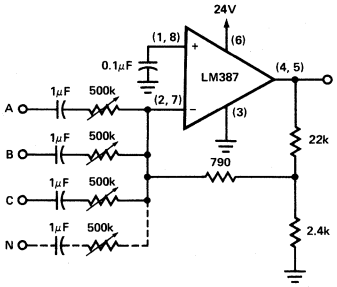
DUAL LOW-NOISE PREAMP LM387

TYPICAL APPLICATIONS

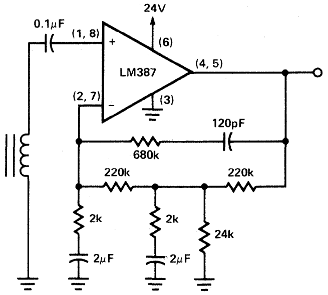
TYPICAL MAGNETIC PHONO PREAMPLIFIER



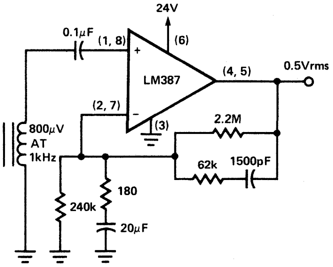
AUDIO MIXER



TWO-POLE FAST TURN-ON NAB TAPE PREAMPLIFIER



TYPICAL TAPE PLAYBACK AMPLIFIER



POWER DRIVER NE/SE540

DESCRIPTION

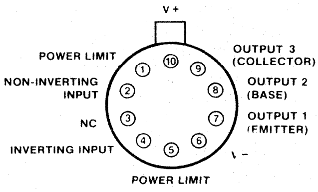
The NE/SE540 is a monolithic, class AB power amplifier designed specifically to drive a pair of complementary output transistors. The device features low standby current yet retains a high output current drive capability with internal current limiting. A wide power bandwidth and excellent linearity make this device ideal for use an audio power amplifier.

FEATURES

- **Internal current limiting**
- **Low standby current**
- **High output current capability**
- **Wide power bandwidth**
- **Low distortion**

PIN CONFIGURATION

H PACKAGE

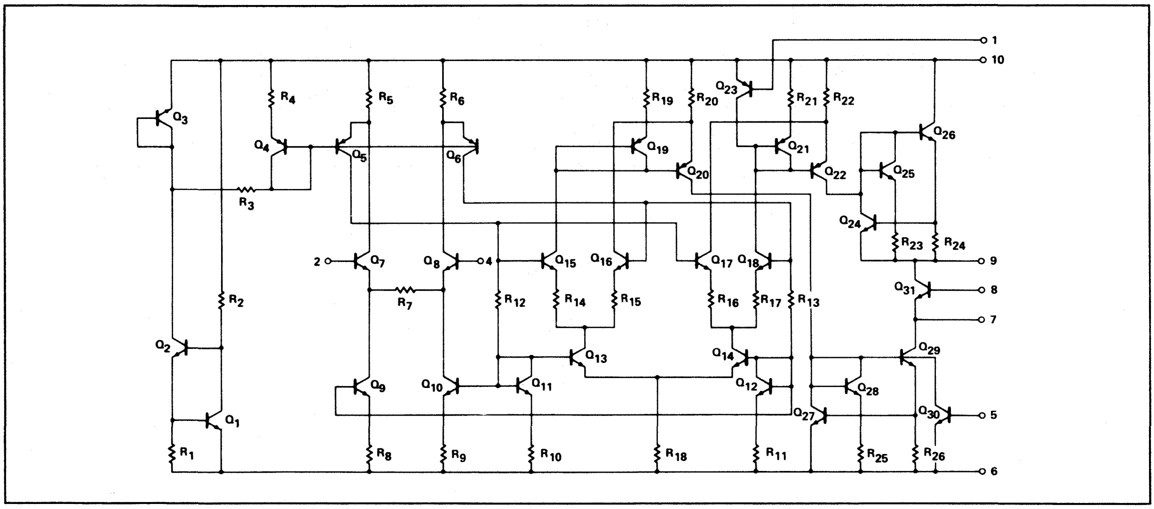


ORDER NUMBERS
NE540H, SE540H

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
SE540	±27	V
NE540	±22	V
Operating temperature range		
SE540	-55 to +125	°C
NE540	0 to +70	°C
Storage temperature range	-65 to +150	°C
Output short circuit duration (Not exceeding maximum dissipation.)	Indefinite	

EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ and $V_{CC} = ±20V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE540			NE540			UNIT
		Min	Typ	Max	Min	Typ	Max	
Operating supply voltage		±5		±25	±5		±20	V
Quiescent current			13	20		13	20	mA
Input offset voltage			5	7		7	10	mV
Input offset current			0.3	0.7		0.5	1	μA
Input bias current			1.5	3		2	5	μA
Input impedance			20			20		kΩ
Current gain		80	100		70	90		dB
Gain variation over temperature range	40dB gain		±0.1			±0.1		dB
Power supply rejection ratio	40dB gain	80	90		60	80		dB
Common mode rejection ratio			110			90		dB
Output drive current		±120	±150		±80	±100		mA

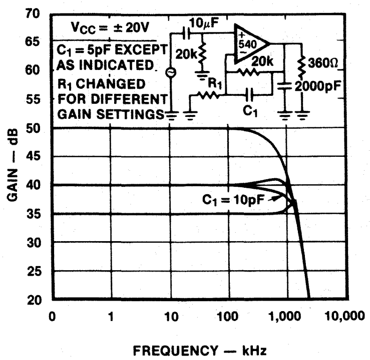
AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ and $V_{CC} = ±20V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE540			NE540			UNIT
		Min	Typ	Max	Min	Typ	Max	
Frequency response	40dB gain ±1dB		500			100		kHz
Distortion	40dB gain, Output 3dB below clipping		0.25	0.5		0.5	1.0	%
	$R_L = 600Ω$							
	$R_L = 2kΩ$		0.06			0.06		
Equivalent input noise voltage	$R_S = 600Ω$ 50Hz to 500kHz		10			10		μV
Slew rate	$V_{CC} = ±20V$ $V_{OUT} = ±15V$		200			200		V/μs

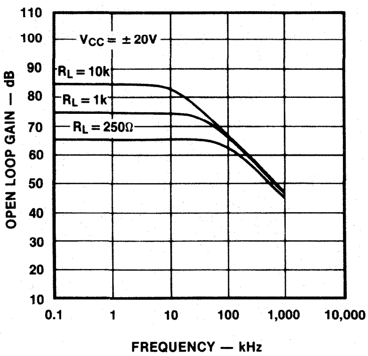
POWER DRIVER NE/SE540

TYPICAL PERFORMANCE CHARACTERISTICS

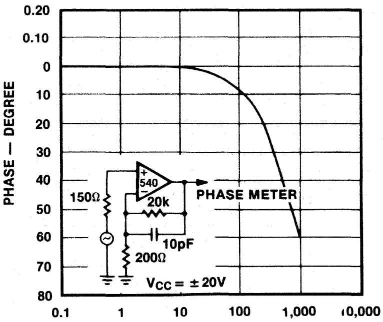
CLOSED LOOP FREQUENCY RESPONSE



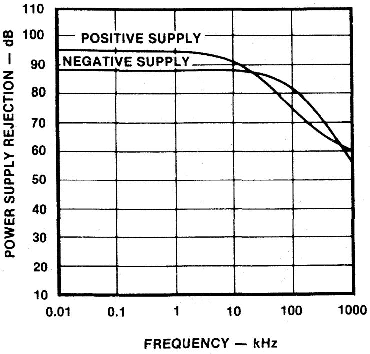
OPEN LOOP GAIN AND FREQUENCY RESPONSE



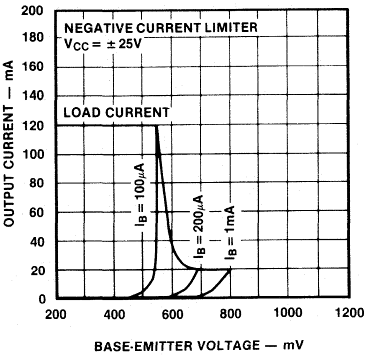
PHASE RESPONSE vs FREQUENCY



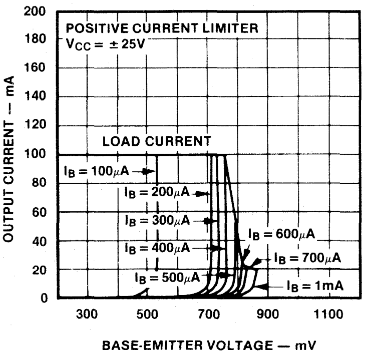
POWER SUPPLY REJECTION vs FREQUENCY



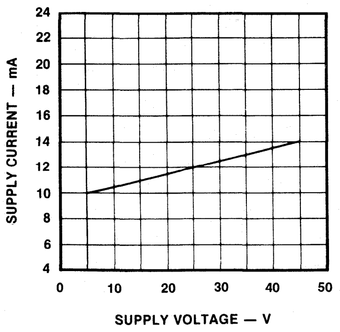
OUTPUT CURRENT vs I_B/V_{BE} OF CURRENT LIMITER



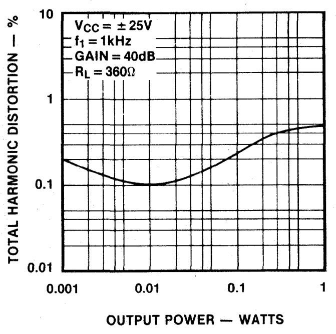
OUTPUT CURRENT vs I_B/V_{BE} OF CURRENT LIMITER



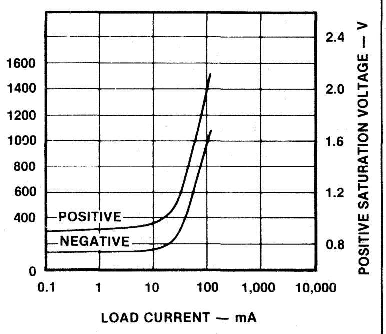
QUIESCENT CURRENT vs SUPPLY VOLTAGE



TOTAL HARMONIC DISTORTION vs OUTPUT



OUTPUT SATURATION VOLTAGE vs LOAD



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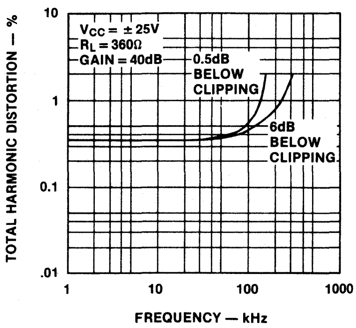
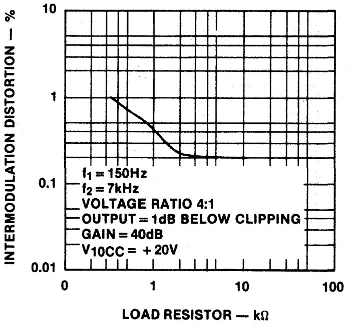
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

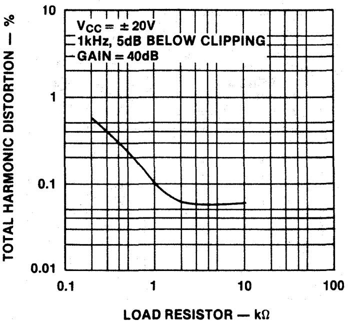
TOTAL HARMONIC DISTORTION vs FREQUENCY



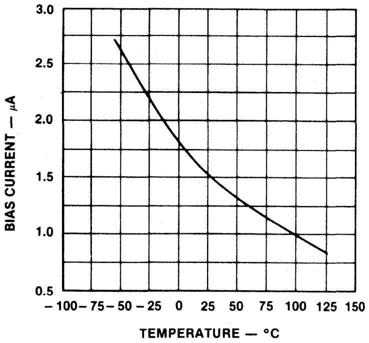
INTERMODULATION DISTORTION vs LOAD



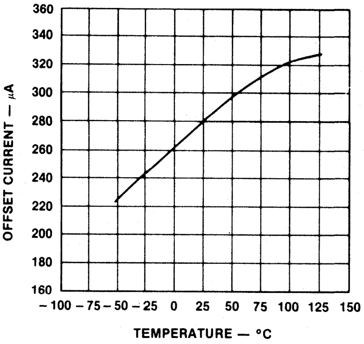
TOTAL HARMONIC DISTORTION vs LOAD



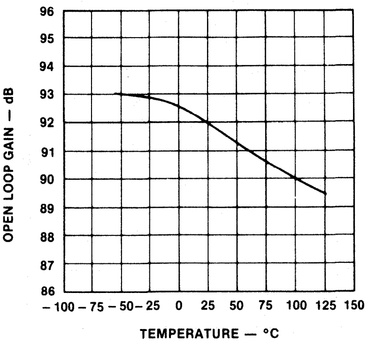
BIAS CURRENT vs TEMPERATURE



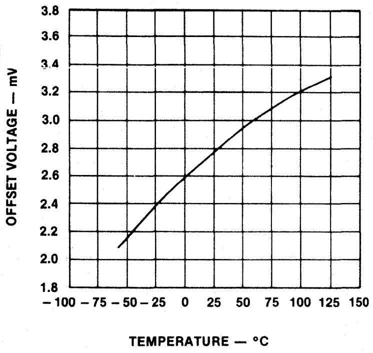
OFFSET CURRENT vs TEMPERATURE



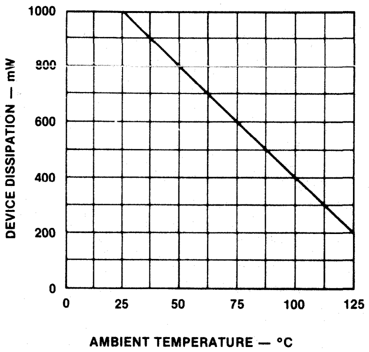
OPEN LOOP GAIN vs TEMPERATURE



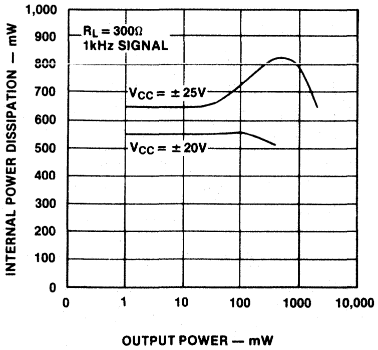
OFFSET VOLTAGE vs TEMPERATURE



MAXIMUM DISSIPATION vs AMBIENT TEMPERATURE



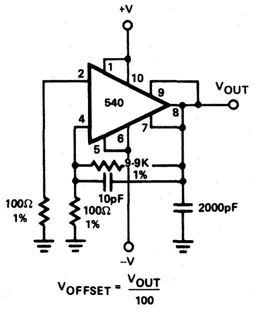
INTERNAL POWER DISSIPATION vs LOAD POWER



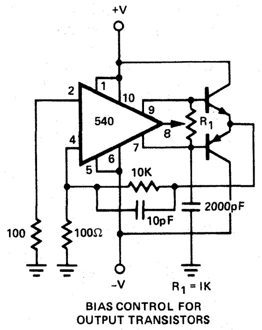
POWER DRIVER NE/SE540

TEST CIRCUITS

OFFSET VOLTAGE MEASUREMENT

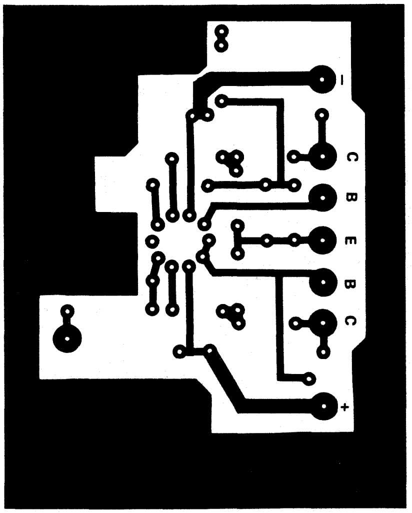


OUTPUT BIAS CONTROL

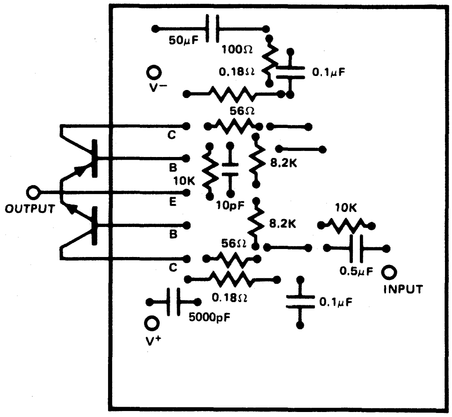


35 WATT AMPLIFIER

P.C. BOARD LAYOUT (Bottom View)



PARTS LAYOUT (Top View)



DUAL LOW-NOISE PREAMP NE542

DESCRIPTION

The NE542 is a dual preamplifier for the amplification of low level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with individual internal power supply decoupler-regulator, providing 110dB supply rejection and 70dB channel separation. Other outstanding features include high gain (104dB), large output voltage swing (V_{CC} -2Vp-p), and internal compensation to 10dB. The NE542 operates from a single supply across the wide range of 9 to 24V.

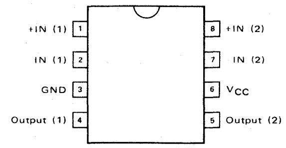
The NE542 is ideal for use in stereo phono, tape, or microphone preamps and other applications requiring low noise amplication of small signals.

FEATURES

- **Low noise—.7μV total input noise**
- **High gain—104dB open loop**
- **Single supply operation**
- **Wide supply range 9 to 24V**
- **Power supply rejection 110dB**
- **Large output voltage swing (V_{CC} -2V p-p)**
- **Wide bandwidth 15MHz unity gain**
- **Power bandwidth 100kHz (15V p-p)**
- **Internally compensated (stable at 10dB)**
- **Short circuit protected**
- **High slew rate 5V/μs**

PIN CONFIGURATION

N PACKAGE



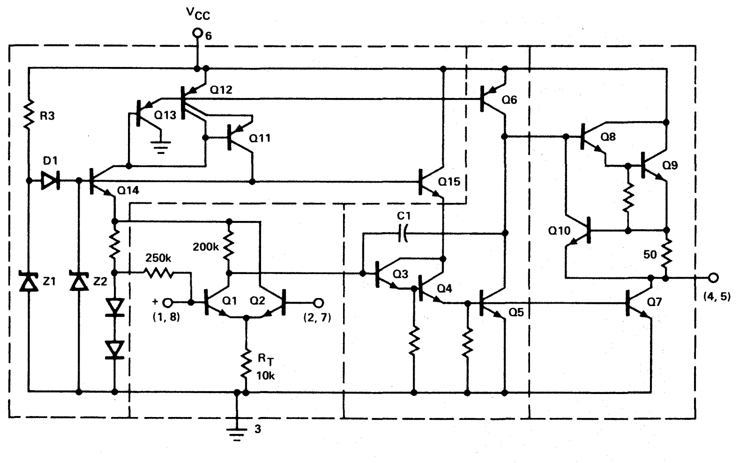
TOP VIEW

ORDER NUMBER
NE542N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	+24	V
Power dissipation	500	mW
Operating temperature range	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	+300	°C

EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = 14V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	NE542			UNIT
		Min	Typ	Max	
Supply voltage		9		24	V
Supply current	$V_{CC} = 9$ to 18V, $R_L = \infty$		9	15	mA
Input resistance					
Positive input			100		kΩ
Negative input			200		kΩ
Output resistance	Open loop		150		Ω

DUAL LOW-NOISE PREAMP NE542

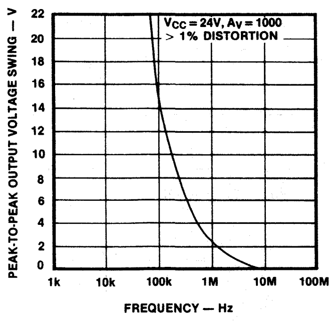
AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = 14V$ unless otherwise specified.

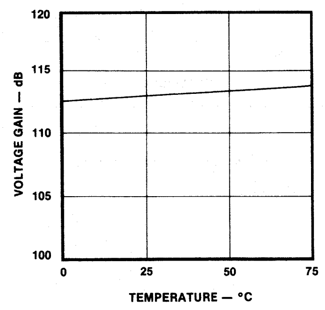
PARAMETER	TEST CONDITIONS	NE542			UNIT
		Min	Typ	Max	
Voltage gain	Open loop		160,000		V/V
Input current Negative input			.5		μA
Output current	Source Sink (linear operation)	8 2	14 3		mA mA
Output voltage swing		V_{CC} -2.5	V_{CC} -2		V
Small signal bandwidth			15		MHz
Slew rate			5		V/μs
Power bandwidth	15V p-p		100		kHz
Maximum input voltage	Linear operation			300	mVrms
Supply rejection ratio	f=60, 120Hz f = 1kHz		100 110		dB dB
Channel separation	f = 1kHz		70		dB
Total harmonic distortion	75dB gain, f = 1kHz		.1		%
Total equivalent input Noise	RS = 600Ω, 100 - 10,000Hz		.7	1.2	μVrms
Noise figure	RS = 50kΩ, 10 - 10,000Hz RS = 20kΩ, 10 10,000Hz RS = 10kΩ, 10 - 10,000Hz RS = 5kΩ, 10 - 10,000Hz		1.2 1.2 1.5 2.4		dB dB dB dB

TYPICAL PERFORMANCE CHARACTERISTICS

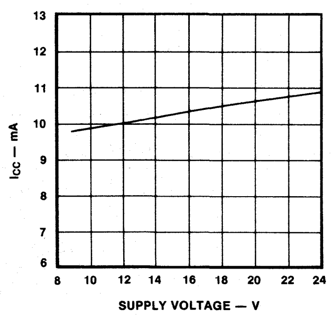
LARGE SIGNAL FREQUENCY RESPONSE



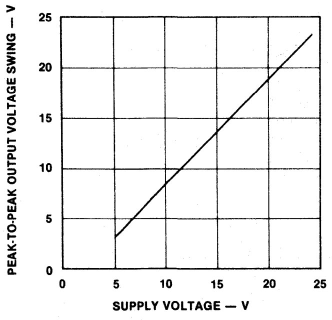
GAIN vs TEMPERATURE



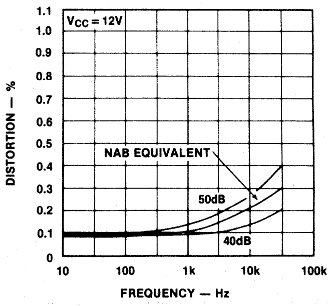
V_{CC} vs I_{CC}



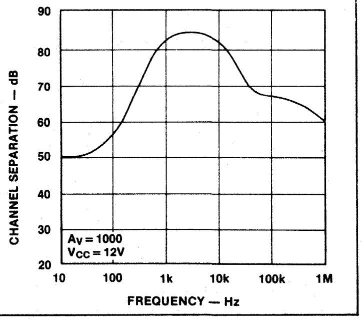
P-P OUTPUT VOLTAGE SWING vs V_{CC}



% DISTORTION

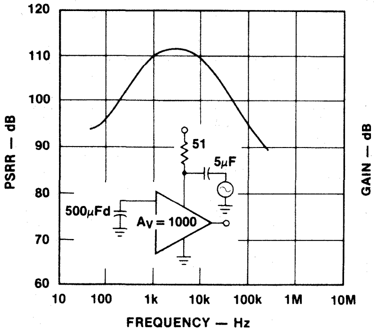


CHANNEL SEPARATION

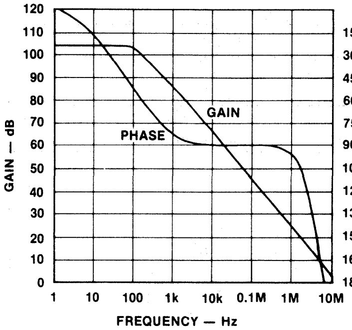


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

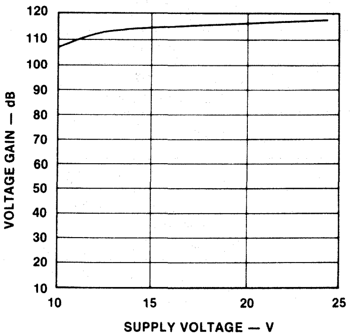
PSRR vs FREQUENCY



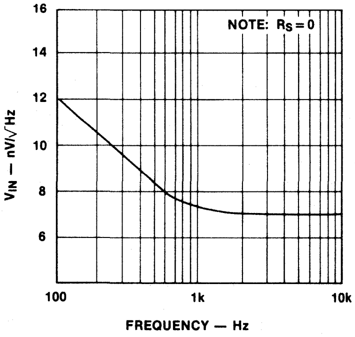
GAIN AND PHASE RESPONSE



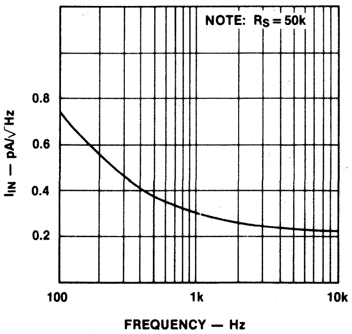
VOLTAGE GAIN vs SUPPLY VOLTAGE



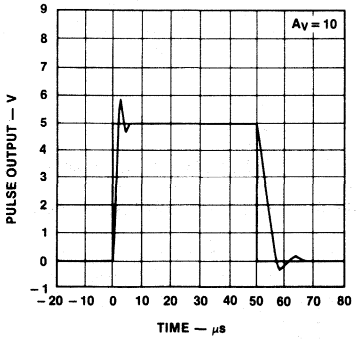
NOISE VOLTAGE vs FREQUENCY



NOISE CURRENT vs FREQUENCY

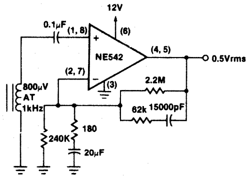


PULSE RESPONSE

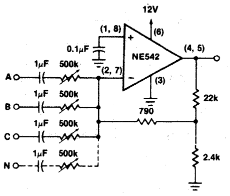


TYPICAL APPLICATIONS

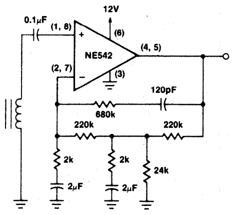
TYPICAL TAPE PLAYBACK AMPLIFIER



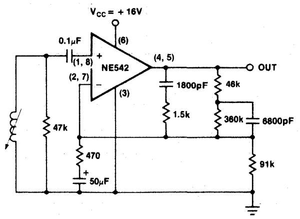
AUDIO MIXER



TWO-POLE FAST TURN-ON NAB TAPE PREAMP



RIAA MAGNETIC PHONO PREAMP



NOTE: All resistors values are typical and in ohms.

COMPANDOR NE570/571/SA571

DESCRIPTION

The NE570/571 is a versatile low cost dual gain control circuit in which either channel may be used as a dynamic range compressor or expandor. Each channel has a full wave rectifier to detect the average value of the signal; a linerarized, temperature compensated variable gain cell; and an operational amplifier.

The NE570/571 is well suited for use in telephone subscriber and trunk carrier systems, communications systems and hi-fi audio systems.

FEATURES

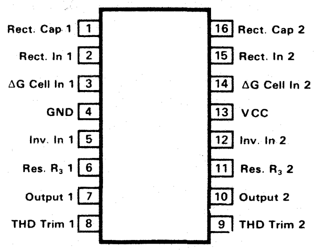
- **Complete compressor and expandor in 1 IC**
- **Temperature compensated**
- **Greater than 110dB dynamic range**
- **Operates down to 6Vdc**
- **System levels adjustable with external components**
- **Distortion may be trimmed out**

APPLICATIONS

- **Telephone trunk compandor—570**
- **Telephone subscriber compandor—571**
- **High level limiter**
- **Low level expandor—noise gate**
- **Dynamic noise reduction systems**
- **Voltage controlled amplifier**
- **Dynamic filters**

PIN CONFIGURATION

F, N PACKAGE



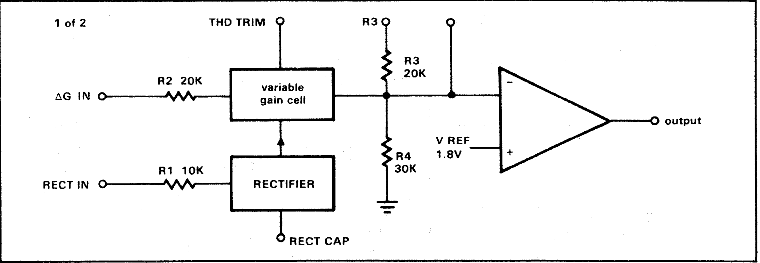
TOP VIEW

ORDER NUMBERS
NE570F,N NE571F,N
SA571F,N

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
	Positive supply		Vdc
	570	24	
	571	18	
T_A	Operating temperature range		
	NE	0 to 70	°C
	SA	-40 to +85	°C
P_D	Power dissipation	400	mW

BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The NE570/571 compandor building blocks, as shown in the block diagram, are a full wave rectifier, a variable gain cell, an operational amplifier and a bias system. The arrangement of these blocks in the IC result in a circuit which can perform well with few external components, yet can be adapted to many diverse applications.

The full wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at V_{REF}. The rectified current is averaged on an external filter capacitor tied to the C_{RECT} terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively coupled voltage inputs as shown in the following equation. Note that for capacitively coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than .1μA.

$$G \propto \frac{|V_{IN} - V_{REF}|\ ave}{R_1}$$

or

$$G \propto \frac{|V_{IN}|\ ave}{R_1}$$

The speed with which gain changes to follow changes in input signal levels is determined by the rectifier filter capacitor. A small capacitor will yield rapid response but will not fully filter low frequency signals. Any ripple on the gain control signal will modulate the signal passing through the variable gain cell. In an expandor or compressor application, this would lead to third harmonic distortion, so there is a tradeoff to be made between fast attack and decay times, and distortion. For step changes in amplitude, the change in gain with time is shown by this equation.

$$G(t) = (G_{initial} - G_{final})\ e^{-t/\tau}$$

$$+ G_{final};\ \tau = 10K \times C_{RECT}$$

The variable gain cell is a current in, current out device with the ratio I_{OUT}/I_{IN} controlled by the rectifier. I_{IN} is the current which flows from the ΔG input to an internal summing node biased at V_{REF}. The following equation applies for capacitively coupled inputs. The output current, I_{OUT}, is fed to the summing node of the op amp.

$$I_{IN} = \frac{V_{IN} - V_{REF}}{R_2} = \frac{V_{IN}}{R_2}$$

A compensation scheme built into the ΔG cell compensates for temperature, and cancels out odd harmonic distortion. The only distortion which remains is even harmonics, and they exist only because of internal offset voltages. The THD trim terminal provides a means for nulling the internal offsets for low distortion operation.

The operational amplifier (which is internally compensated) has the non-inverting input tied to V_{REF}, and the inverting input connected to the ΔG cell output as well as brought out externally. A resistor, R_3, is brought out from the summing node and allows compressor or expandor gain to be determined only by internal components.

COMPANDOR

NE570/571/SA571

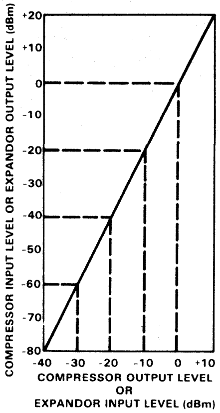
The output stage is capable of ±20mA output current. This allows a +13dBm (3.5V rms) output into a 300Ω load which, with a series resistor and proper transformer, can result in +13dBm with a 600Ω output impedance.

A band gap reference provides the reference voltage for all summing nodes, a regulated supply voltage for the rectifier and ΔG cell, and a bias current for the ΔG cell. The low tempco of this type of reference provides very stable biasing over a wide temperature range.

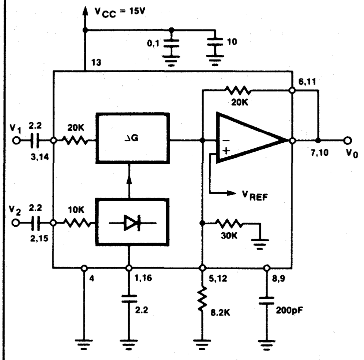
The typical performance characteristics illustration shows the basic input-output transfer curve for basic compressor or expandor circuits.

TYPICAL PERFORMANCE CHARACTERISTICS

BASIC INPUT-OUTPUT TRANSFER CURVE



TYPICAL TEST CIRCUIT



DC ELECTRICAL CHARACTERISTICS $T_A = 25°C, V_{CC} = 15V$[1]

PARAMETER	TEST CONDITIONS	NE570			NE/SA571[6]			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{CC} Supply voltage		6		24	6		18	V
I_{CC} Supply current	No signal		3.2	4.0		3.2	4.8	mA
Output current capability		±20						mA
Output slew rate			±.5					V/us
Gain cell distortion[2]	Untrimmed		.3	1.0		.5	2.0	%
	Trimmed		.05			.1		
Resistor tolerance			±5	±15				%
Internal reference voltage		1.7	1.8	1.9	1.65	1.8	1.95	V
Output dc shift[3]	Untrimmed		±20	±50		±30	±100	mV
Expandor output noise	No signal, 20Hz-20kHz		20					µV
			−15					dBRNC
Unity gain level		−1	0	+1	−1.5	0	+1.5	dBm
Gain change[2],[4]	−40°C < T < 70°C		±.1			±.1		dB
	0°C < T < 70°C		±.1	±.2		±.1	±.4	
Reference drift[4]	−40°C < T < 70°C		+2, −25	-10, −40		+2, −25	+20, −50	mV
	0°C < T < 70°C		±5	±10		±5	±20	
Resistor drift[4]	−40°C < T < 70°C		+8,−0					%
	0°C < T < 70°C		+1,−0					
Tracking error [5], input V_1 = OdBm	Rectifier input, V_2 =							dB
	+6dBm		±.2					
	−10dBm		+.2	−.2,+.4		+.2	−.2,+.5	
	−20dBm		+.2	−.3,+.6		+.2	−.4,+.7	
	−30dBm		+.2	−.5,+1		+.2	−1,+1.5	
	−40dBm		+.2,−.4			+.2,−.4		

NOTES

1. Except where indicated, the 571 specifications are identical to the 570
2. Measured at OdBm,1kHz
3. Expandor ac input change from no signal to OdBm
4. Relative to value at T_A = 25°C
5. Relative to OdBm
6. Electrical characteristics for the SA571 only are specified over −40 to +85°C temperature range.

PROGRAMMABLE ANALOG COMPANDOR NE572

DESCRIPTION

The NE572 is a dual channel, high performance gain control circuit in which either channel may be used for dynamic range compression or expansion. Each channel has a full wave rectifier to detect the average value of input signal; a linearized, temperature compensated variable gain cell (ΔG) and a dynamic time constant buffer. The buffer permits independent control of dynamic attack and recovery time with minimum external components and improved low frequency gain control ripple distortion over previous compandors.

The NE572 is intended for noise reduction in high performance audio systems. It can also be used in a wide range of communication systems and video recording applications.

FEATURES

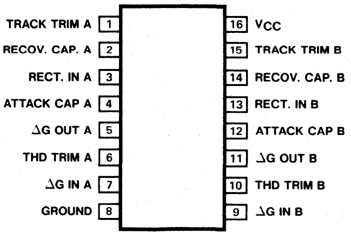
- **Independent control of attack and recovery time.**
- **Improved low frequency gain control ripple**
- **Complementary gain compression and expansion with external Op Amp**
- **Wide dynamic range—greater than 110dB**
- **Temperature compensated gain control**
- **Low distortion gain cell**
- **Low noise—6μV typical**
- **Wide supply voltage range—6V-22V**
- **System level adjustable with external components.**

APPLICATIONS

- **Dynamic noise reduction system**
- **Voltage control amplifier**
- **Stereo expandor**
- **Automatic level control**
- **High level limiter**
- **Low level noise gate**
- **State variable filter**

PIN CONFIGURATION

N PACKAGE



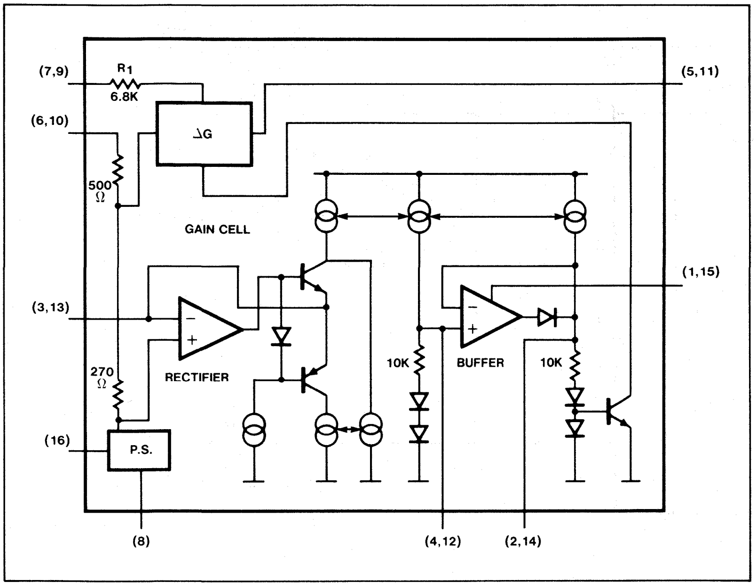
TOP VIEW

ORDER NUMBER
NE572N

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	22	VDC
T_A	Operating temperature range	0 to 70	°C
P_D	Power dissipation	500	mW

BLOCK DIAGRAM

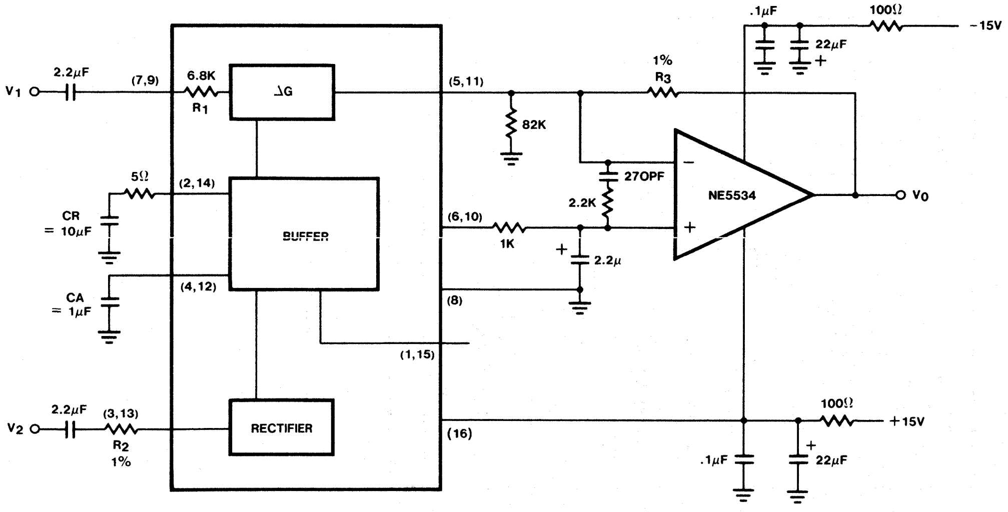


ELECTRICAL CHARACTERISTICS

Standard Test Conditions (unless otherwise noted) V_{CC} = 15V TA = 25°C Expandor mode (see test circuit) Input signals at unity gain level = 100mV RMS at 1KHz, $V_1 = V_2$, R_2 = 3.3K R_3 = 17.3K

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		6		22	V_{DC}
I_{CC}	Supply current	No Signal			6	mA
	Internal voltage reference		2.3	2.5	2.7	V_{DC}
THD	(untrimmed)	1kHz $C_A = 1.0\mu F$		.2	1.0	%
THD	(trimmed)	1kHz $C_R = 10\mu F$		.05		%
THD	(trimmed)	100Hz		.25		%
	No signal output noise	Input to V_1 and V_2 grounded (20-20kHz)		6	25	uV
	DC level shift (untrimmed)	Input change from no signal to 100mV RMS		±20	±50	MV
	Unity gain level		−1	0	+1	dB
	Large signal distortion	$V_1 = V_2$ = 400mV		0.7	3.0	%
	Tracking error measured relative to value at unity gain output	Rectifier input V_2 = +6dB		±.2		dB
		−30dB		±.5	−1.5 +.8	
	Channel crosstalk	200mV RMS into channel A, measured output on channel B	60			dB
	Power supply rejection ratio	120Hz		70		dB

TEST CIRCUIT



DOLBY NOISE REDUCTION CIRCUIT NE645/46

DESCRIPTION

The NE645/646 is a monolithic audio noise reduction circuit designed as a direct replacement device for the NE645B/NE646B in Dolby* B- and C-Type noise reduction systems. The NE645/646 is used to reduce the level of background noise introduced during recording and playback of audio signals on magnetic tape, and to improve the noise level in FM broadcast reception. This circuit is available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, California.

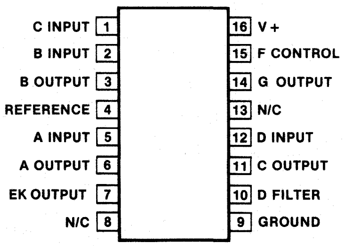
NOTE
*T.M. Dolby Laboratories Licensing Corporation.

FEATURES

- **Accurate record mode frequency response**
- **Excellent frequency response tracking with temperature and V_{CC} ±0.4 dB typical**
- **Excellent back-to-back dynamic response — D.C. shift less than 20 mV typical**
- **Improved stability of all op amps**
- **High reliability packaging**

PIN CONFIGURATION

N PACKAGE



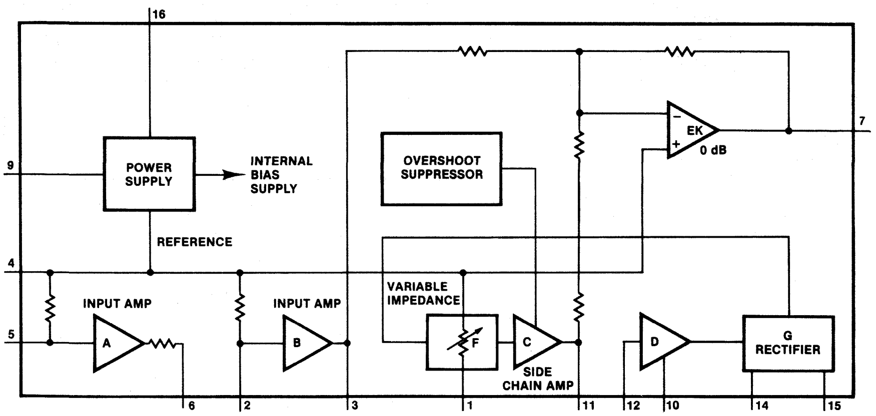
TOP VIEW

ORDER NUMBERS
NE645N, NE646N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	24	V
Temperature range		
Operating	0 to +70	°C
Storage	−65 to +150	°C
Lead temperature (soldering, 60 sec)	+300	°C

BLOCK DIAGRAM



DOLBY NOISE REDUCTION CIRCUIT

NE645/46

ELECTRICAL CHARACTERISTICS

V_{CC} = 12 volts, f = 20 Hz to 20 kHz.
All levels referenced to 580 mVrms (0 dB) at Pin 3, T_A = +25°C
Unless otherwise noted.

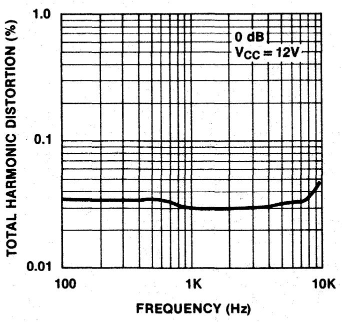
PARAMETER	TEST CONDITIONS	NE645			NE646			UNIT
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage Range		8		20	8		20	V
Supply Current, I_{CC}	V_{CC} = 12V		16	24		16	24	mA
Voltage gain (Pins 5-3)	f = 1 kHz (Pins 6 and 2 connected)	24.5	26	27.5	24.5	26	27.5	dB
Voltage gain (Pins 3-7)	f = 1 kHz, 0 dB at pin 3, noise reduction out	–0.5	0	+0.5	–0.5	0	+0.5	dB
Distortion								
THD, 2nd and 3rd harmonic	f = 20 Hz – 10 kHz, 0dB		0.05	0.1		0.05	0.2	%
	f = 20 Hz – 10 kHz, +10 dB		0.15	0.3		0.2	0.5	%
Signal handling[1] (V_{CC} = 12V)	1% dist at 1 kHz	+12	+15		+12	+15		dB
Signal-to-noise ratio[2]	Record mode	67	72		64	72		dB
	Playback mode	77	82		74	82		dB
Record mode Frequency response (at pin 7) referenced to encode monitor point (pin 3)	f = 1.4kHz							
	0dB	–1	0	+1	–1.5	0	+1.5	dB
	–20dB	–16.6	–15.6	–14.6	–17.1	–15.6	–14.1	dB
	–30dB	–23.5	–22.5	–21.5	–24.0	–22.5	–21.0	dB
	f = 5kHz							
	0dB	–0.7	+0.3	+1.3	–1.2	+0.3	+1.8	dB
	–20dB	–17.8	–16.8	–15.8	–18.3	–16.8	–15.3	dB
	–30dB	–22.8	–21.8	–20.8	–23.3	–21.8	–20.3	dB
	–40dB	–30.2	–29.7	–28.7	–30.2	–29.7	–28.2	dB
	f = 20kHz							
	0dB	–0.3	+0.7	+1.7	–0.8	+0.7	+2.2	dB
	–20dB	–18.3	–17.3	–16.3	–18.8	–17.3	–15.8	dB
	–30dB	–24.5	–23.5	–22.5	–25.0	–23.5	–22.0	dB
Back-to-back frequency response	Using typical record mode frequency response test points	–1	0	+1	–1.5	0	+1.5	dB
Input resistance	Pin 5	35	50	65	35	50	65	kΩ
	Pin 2	3.1	4.2	5.3	3.1	4.2	5.3	kΩ
Output resistance	Pin 6	1.9	2.4	3.1	1.9	2.4	3.1	kΩ
	Pin 3		80	120		80	120	Ω
	Pin 7		80	120		80	120	Ω
Back-to-back frequency response shift								
Versus temperature	0°-70°C		±0.4			±0.4		dB
Versus supply voltage	8-20V		±0.4			±0.4		dB

NOTES
1. See maximum signal handling versus supply voltage characteristics.
2. All noise levels are measured CCIR/ARM weighted using a 10K source with respect to Dolby level. See Dolby Laboratories Bulletin 19.

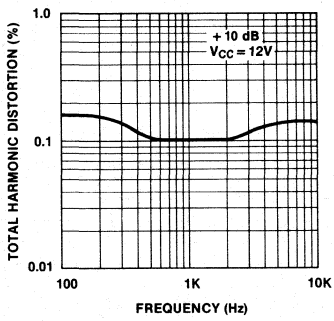
DOLBY NOISE REDUCTION CIRCUIT NE645/46

PERFORMANCE CHARACTERISTICS

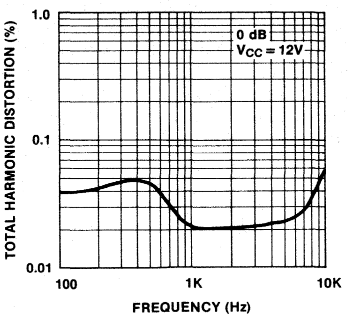
THD vs FREQUENCY RECORD MODE



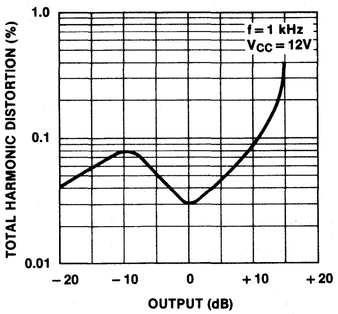
THD vs FREQUENCY RECORD MODE



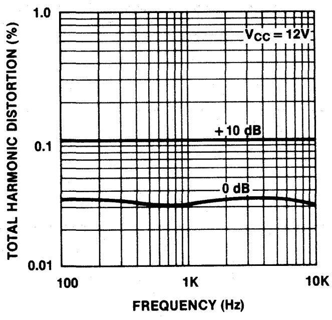
THD vs FREQUENCY PLAY MODE



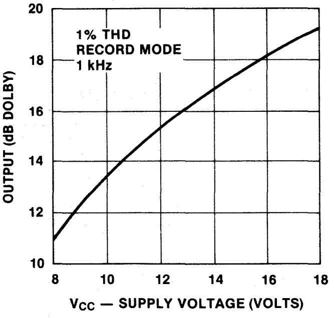
THD vs OUTPUT RECORD MODE



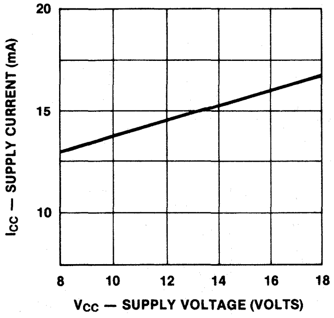
THD vs FREQUENCY NOISE REDUCTION (NR) OFF



MAXIMUM SIGNAL HANDLING vs SUPPLY VOLTAGE



SUPPLY CURRENT vs SUPPLY VOLTAGE



DOLBY NOISE REDUCTION CIRCUIT NE645/46

APPLICATION INFORMATION

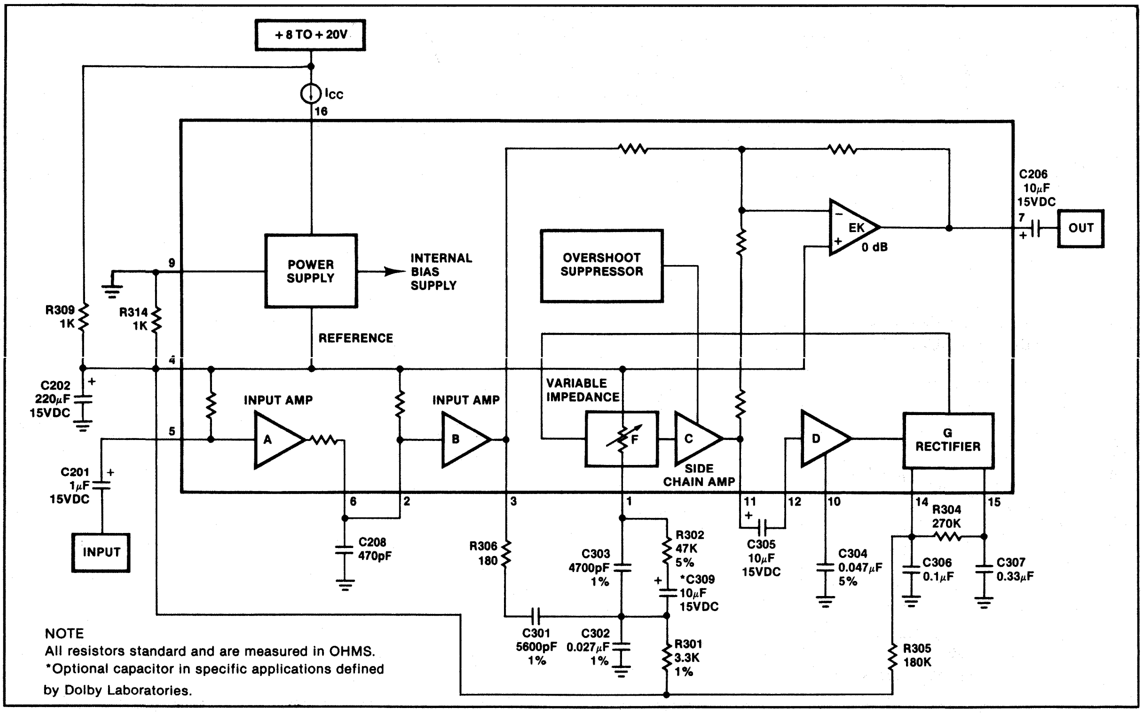
The NE645/646 is a direct replacement for the NE645B/646B. The NE645/646 incorporates improved design techniques to insure excellent performance required in Dolby B and C Type Audio Noise Reduction Systems. Critical component values are unchanged except for C309 on Pin 1 which is now an optional component in specific applications defined by Dolby Laboratories. All circuit parameters are guaranteed at 12V V_{CC}.

DOLBY ENCODER Output for constant level input (single tone frequency response)

Frequency (kHz)	Input Level (dB)								
	0 (Dolby Level)	-5	-10	-15	-20	-25	-30	-35	-40
0.1	0	0.1	0	0.1	0	0	0	0	0
0.14	0	0.2	0.2	0.2	0.2	0.2	0.1	0.2	0.1
0.2	0	0.3	0.4	0.5	0.5	0.6	0.6	0.5	0.5
0.3	0	0.3	0.6	1.1	1.3	1.3	1.3	1.3	1.3
0.4					2.0	2.1	2.2	2.3	2.1
0.5	0	0.3	0.8	1.8	2.6	2.9	2.9	3.0	2.9
0.6						3.6	3.7	3.8	3.7
0.7	0	0.4	0.9	2.1	3.5	4.3	4.4	4.5	4.4
0.8						4.8	5.0	5.3	5.1
0.9							5.6	5.8	5.6
1.0	0	0.4	1.0	2.3	4.2	5.7	6.1	6.3	6.2
1.2							6.9	7.1	7.1
1.4	0	0.3	0.9	2.3	4.4	6.6	7.5	7.7	7.7
2.0	0.1	0.4	0.9	2.2	4.3	7.0	8.5	8.9	8.9
3.0	0.2	0.6	0.9	1.9	3.9	6.6	8.8	9.7	9.7
5.0	0.3	0.6	1.0	1.7	3.2	5.4	8.2	10.0	10.3
7.0	0.3	0.6	1.0	1.7	2.8	4.7	7.3	9.7	10.4
10.0	0.4	0.7	1.1	1.7	2.6	4.2	6.5	9.1	10.4
14.0	0.5	0.8	1.1	1.8	2.7	4.4	6.5	8.7	10.3
20.0	0.7	0.7	1.2	1.9	2.7	4.4	6.5	8.7	10.3

NOTE
The figures given in this table are the average response of many of Dolby Laboratories' professional encoders, and are not intended to be taken as required consumer equipment performance characteristics. Thus, no inference should be drawn on the tolerances which licensees must retain in consumer equipment. The figures can, however, be used to plot typical characteristics.

TEST CIRCUIT NE645/646



NOTE
All resistors standard and are measured in OHMS.
*Optional capacitor in specific applications defined by Dolby Laboratories.

LOW VOLTAGE DOLBY NOISE REDUCTION CIRCUIT NE648/49

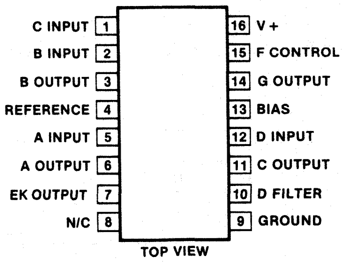
DESCRIPTION

The NE648/649 is an audio noise reduction circuit designed for use in low voltage entertainment systems. The circuit is used to reduce the level of background noise introduced during the recording and playback of audio signals on magnetic tape and improve the noise level in FM broadcast reception. The circuit is intended for use in automotive and portable cassette Dolby* B and C Type noise reduction systems. This circuit is available only to licensees of Dolby Laboratories Licensing Corp., San Francisco.

NOTE
*T.M. Dolby Laboratories Licensing Corporation

PIN CONFIGURATION

N PACKAGE

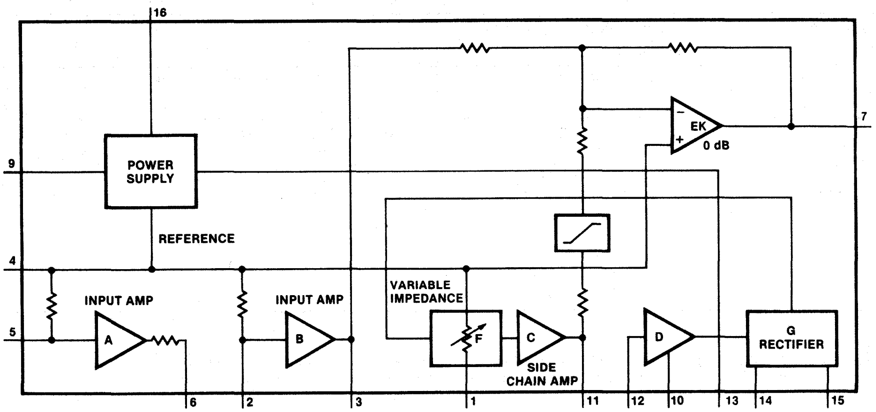


ORDER NUMBERS
NE648N, NE649N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	16	V
Temperature range		
Operating	– 40 to + 85	°C
Storage	– 65 to + 150	°C
Lead temperature (soldering 60sec)	+ 300	°C

BLOCK DIAGRAM



LOW VOLTABE DOLBY NOISE REDUCTION CIRCUIT NE648/49

DC ELECTRICAL CHARACTERISTICS V_{CC} = 9V, f = 20Hz to 20kHz.

All levels referenced to 580mVrms (0dB) at pin 3, T_A = +25°C unless otherwise noted.

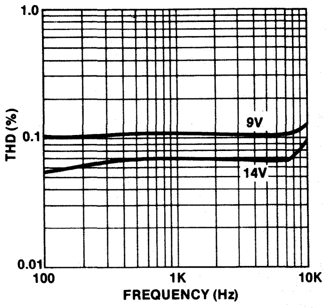
PARAMETER	TEST CONDITIONS	NE648			NE649			UNIT
		Min	Typ	Max	Min	Typ	Max	
Supply voltage range^3		6	9	14	6	9	14	V
Minimum voltage supply for 8dB headroom 10dB headroom	f = 1.4kHz THD < 1%	6.5 7.5			6.5 7.5			V V
Supply Current, I_{CC}			11	18		11	18	mA
Supply Current,^{1} I_{CC}				20			20	mA
Voltage gain (pins 5-3)	f = 1kHz (pins 6 and 2 connected)	24.5	26	27.5	24.5	26	27.5	dB
Voltage gain (pins 3-7)	f = 1kHz, 0dB at pin 3, noise reduction out	−0.5	0	+0.5	−0.5	0	+0.5	dB
Distortion	f = 20kHz to 10kHz, 0dB f = 20Hz to 10kHz, +10dB		0.05 0.2	0.1 0.3		0.05 0.2	0.2 0.5	% %
Signal Handling (See Performance Characteristics)								
Signal-to-noise ratio^2	Record (pins 6 and 2 connected)	67	72		64	72		dB
	Playback (pins 6 and 2 connected)	77	82		74	82		dB
Record mode frequency response (at pin 7) referenced to encode monitor point (pin 3)	f = 1.4kHz							
	0dB	−1	0	+1	−1.5	0	+1.5	dB
	−20dB	−16.6	−15.6	−14.6	−17.1	−15.6	−14.1	dB
	−30dB	−23.5	−22.5	−21.5	−24.0	−22.5	−21.0	dB
	f = 5kHz							
	0dB	−0.7	+0.3	+1.3	−1.2	+0.3	+1.8	dB
	−20dB	−17.8	−16.8	−15.8	−18.3	−16.8	−15.3	dB
	−30dB	−22.8	−21.8	−20.8	−23.3	−21.8	−20.3	dB
	−40dB	−30.2	−29.7	−28.7	−30.2	−29.7	−28.2	dB
	f = 20kHz							
	0dB	−0.3	+0.7	+1.7	−0.8	+0.7	+2.2	dB
	−20dB	−18.3	−17.3	−16.3	−18.8	−17.3	−15.8	dB
	−30dB	−24.5	−23.5	−22.5	−25.0	−23.5	−22.0	dB
Back-to-back frequency response	Using typical record mode response		± 1.0			± 1.5		dB
Input resistance	Pin 5	35	50	65	35	50	65	kΩ
	Pin 2	3.1	4.2	5.3	3.1	4.2	5.3	kΩ
Output resistance	Pin 6	1.9	2.4	3.1	1.9	2.4	3.1	kΩ
	Pin 3		80	120		80	120	Ω
	Pin 7		80	120		80	120	Ω
Record mode frequency response shift								
Versus temperature	0 to 70°C		± 0.3					dB
	− 40 to 85°C		± 0.5					dB
Versus V_{CC}	6 to 14V		0.2					dB/V

NOTES

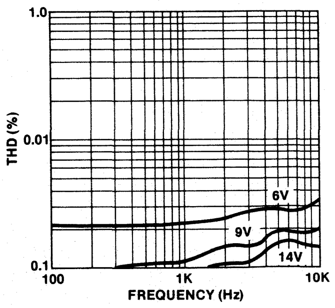
1. With electronic switching.
2. All noise levels are measured CCIR/ARM weighted using a 10K source with respect to Dolby level. See Dolby Laboratories Bulletin 19.
3. The circuit will function as low as V_{CC} = 4.5V (i.e. output signal present). See graphs of I_{CC} and signal handling vs V_{CC}.

PERFORMANCE CHARACTERISTICS

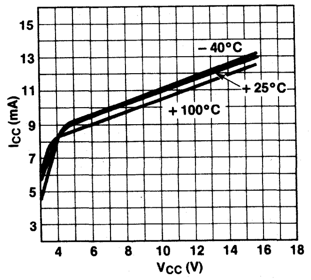
(+10dB) THD vs FREQUENCY



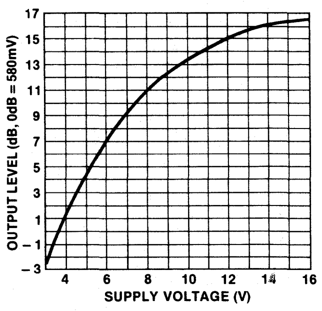
(0dB) THD vs FREQUENCY



CURRENT vs SUPPLY VOLTAGE



MAXIMUM SIGNAL HANDLING vs SUPPLY VOLTAGE FOR 1% THD (RECORD)



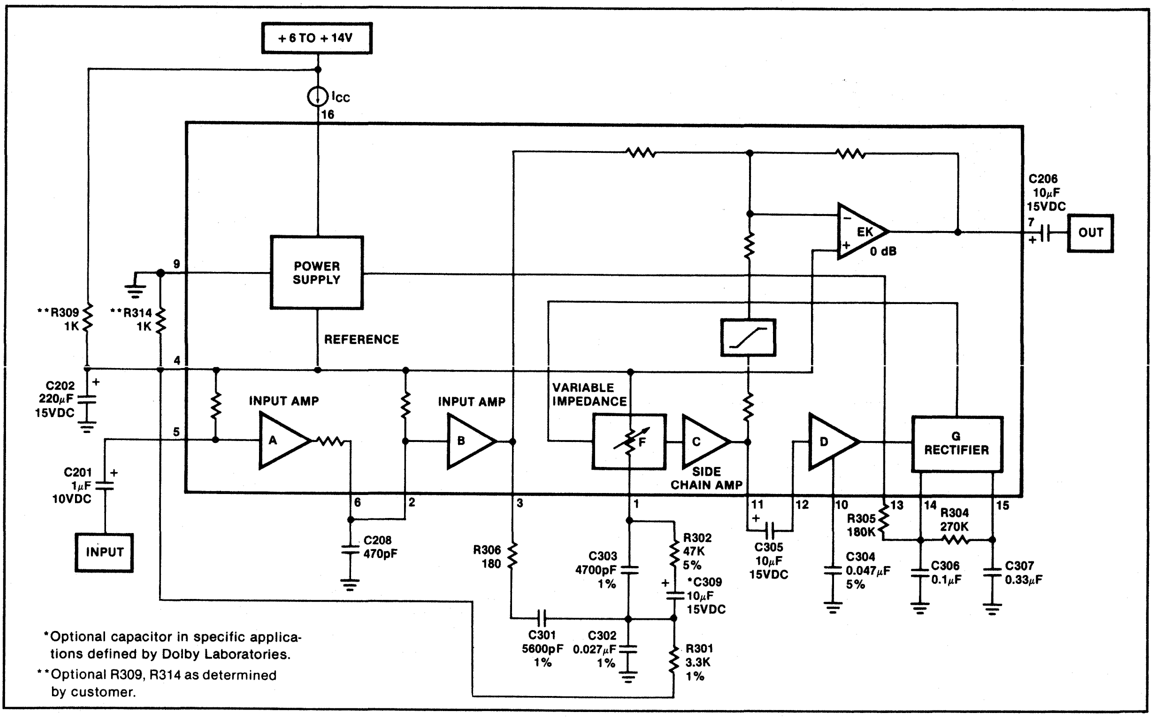
LOW VOLTABE DOLBY NOISE REDUCTION CIRCUIT NE648/49

DOLBY ENCODER Output for constant level input (single tone frequency response)

Frequency (kHz)	Input Level (dB)								
	0 (Dolby Level)	-5	-10	-15	-20	-25	-30	-35	-40
0.1	0	0.1	0	0.1	0	0	0	0	0
0.14	0	0.2	0.2	0.2	0.2	0.2	0.1	0.2	0.1
0.2	0	0.3	0.4	0.5	0.5	0.6	0.6	0.5	0.5
0.3	0	0.3	0.6	1.1	1.3	1.3	1.3	1.3	1.3
0.4					2.0	2.1	2.2	2.3	2.1
0.5	0	0.3	0.8	1.8	2.6	2.9	2.9	3.0	2.9
0.6						3.6	3.7	3.8	3.7
0.7	0	0.4	0.9	2.1	3.5	4.3	4.4	4.5	4.4
0.8						4.8	5.0	5.3	5.1
0.9							5.6	5.8	5.6
1.0	0	0.4	1.0	2.3	4.2	5.7	6.1	6.3	6.2
1.2							6.9	7.1	7.1
1.4	0	0.3	0.9	2.3	4.4	6.6	7.5	7.7	7.7
2.0	0.1	0.4	0.9	2.2	4.3	7.0	8.5	8.9	8.9
3.0	0.2	0.6	0.9	1.9	3.9	6.6	8.8	9.7	9.7
5.0	0.3	0.6	1.0	1.7	3.2	5.4	8.2	10.0	10.3
7.0	0.3	0.6	1.0	1.7	2.8	4.7	7.3	9.7	10.4
10.0	0.4	0.7	1.1	1.7	2.6	4.2	6.5	9.1	10.4
14.0	0.5	0.8	1.1	1.8	2.7	4.4	6.5	8.7	10.3
20.0	0.7	0.7	1.2	1.9	2.7	4.4	6.5	8.7	10.3

NOTE
The figures given in this table are the average response of many of Dolby Laboratories' professional encoders, and are not intended to be taken as required consumer equipment performance characteristics. Thus, no inference should be drawn on the tolerances which licensees must retain in consumer equipment. The figures can, however, be used to plot typical characteristics.

TEST CIRCUIT NE648/49



*Optional capacitor in specific applications defined by Dolby Laboratories.
**Optional R309, R314 as determined by customer.

DOLBY B/C TYPE NOISE REDUCTION CIRCUIT NE650

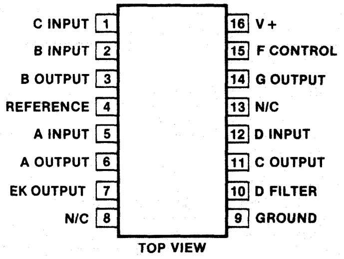
DESCRIPTION

The NE650 is a monolithic audio noise reduction circuit designed for use in Dolby* B/C Type noise reduction systems. The NE650 is used to reduce the level of background noise introduced during recording and playback of audio signals on magnetic tape. The NE650 features excellent dynamic characteristics over a wide range of operating conditions and is pin compatible with NE645/646. This circuit is available only to licensees of Dolby Laboratories Licensing Corp., San Francisco.

NOTE
*T.M. Dolby Laboratories Licensing Corporation.

PIN CONFIGURATION

N PACKAGE

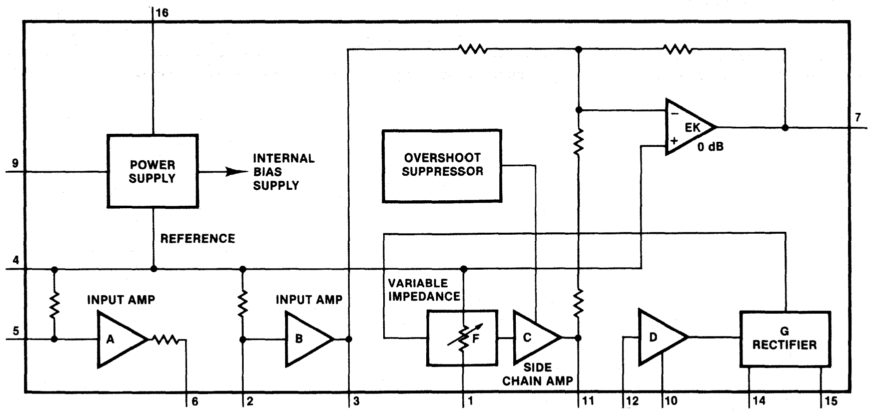


ORDER NUMBER
NE650N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	24	V
Temperature range		
Operating	0 to +70	°C
Storage	−65 to +150	°C
Lead temperature (soldering 60sec)	+300	°C

BLOCK DIAGRAM



DOLBY B/C TYPE NOISE REDUCTION CIRCUIT NE650

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 12V, f = 20Hz to 20kHz.
All levels referenced to 580mVrms (0dB) at pin 3, T_A = +25°C unless otherwise noted.

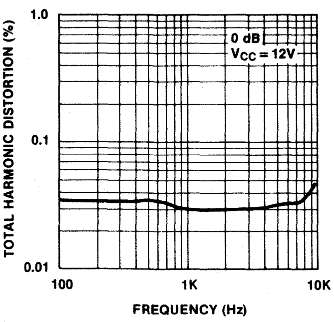
PARAMETER	TEST CONDITIONS	NE650			UNIT
		Min	Typ	Max	
Supply voltage range		8		20	V
Supply current, I_{CC}	Electronic switching on		16	24	mA
Voltage gain (pins 5-3)	f = 1kHz (pins 6 and 2 connected)	25.5	26	26.5	dB
Voltage gain (pins 3-7)	f = kHz, 0dB at pin 3, noise reduction out	−0.5	0	+0.5	dB
Voltage gain (pins 2-3)	f = 1kHz		13		dB
Distortion THD; 2nd and 3rd harmonic	f = 20Hz to 10kHz, 0dB		0.05	0.1	%
	f = 20Hz to 10kHz, +10dB		0.15	0.3	%
Signal handling	1% distortion at 1kHz	+12	+15		dB
Signal-to-noise ratio*	Record mode	68	72		dB
	Playback mode	78	82		dB
Back-to-back frequency response	Using typical record mode response		±0.5		dB
Record mode frequency response (at pin 7) referenced to encode monitor point (pin 3)	f = 1.4kHz				
	0dB	−0.5	0	+0.5	dB
	−20dB	−16.1	−15.6	−15.1	dB
	−30dB	−23.5	−22.5	−21.5	dB
	f = 5kHz				
	0dB	−0.7	+0.3	+1.3	dB
	−20dB	−17.3	−16.8	−16.3	dB
	−30dB	−22.3	−21.8	−21.3	dB
	−40dB	−30.2	−29.7	−29.2	dB
	f = 20kHz				
	0dB	−0.3	+0.7	+1.7	dB
	−20dB	−18.3	−17.3	−16.3	dB
	−30dB	−24.5	−23.5	−22.5	dB
Input resistance	Pin 5	35	50	65	kΩ
	Pin 2	3.1	4.2	5.3	kΩ
Output resistance	Pin 6	1.9	2.4	3.1	kΩ
	Pin 3		80	120	Ω
	Pin 7		80	120	Ω
Back-to-back frequency response shift					
Versus T_A	0°C to −70°C		±0.4		dB
Versus V_{CC}	8 to 20V		±0.4		dB

*All noise levels are measured CCIR/ARM weighted using a 10K source with respect to Dolby level. See Dolby Laboratories Bulletin 19.

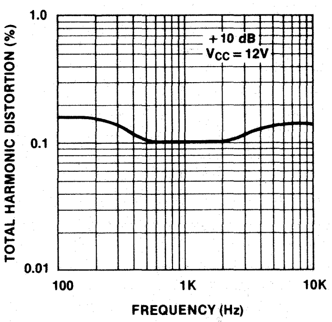
DOLBY B/C TYPE NOISE REDUCTION CIRCUIT NE650

PERFORMANCE CHARACTERISTICS

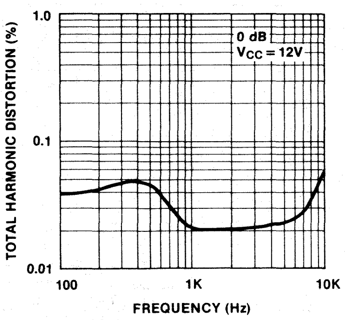
THD vs FREQUENCY RECORD MODE



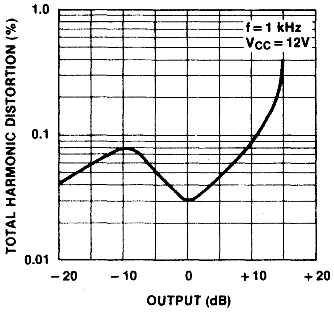
THD vs FREQUENCY RECORD MODE



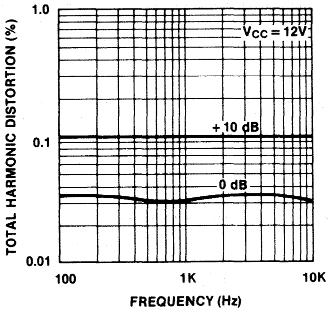
THD vs FREQUENCY PLAY MODE



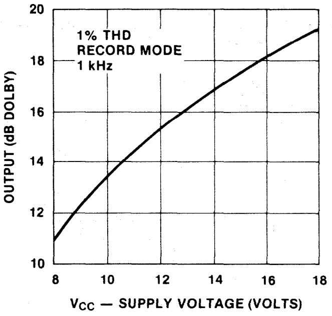
THD vs OUTPUT RECORD MODE



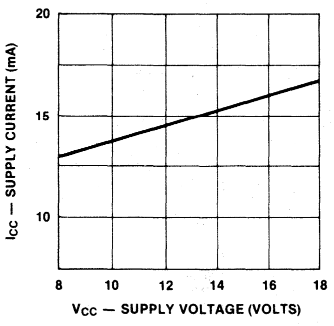
THD vs FREQUENCY
NOISE REDUCTION (NR) OFF



MAXIMUM SIGNAL HANDLING vs
SUPPLY VOLTAGE



SUPPLY CURRENT vs
SUPPLY VOLTAGE



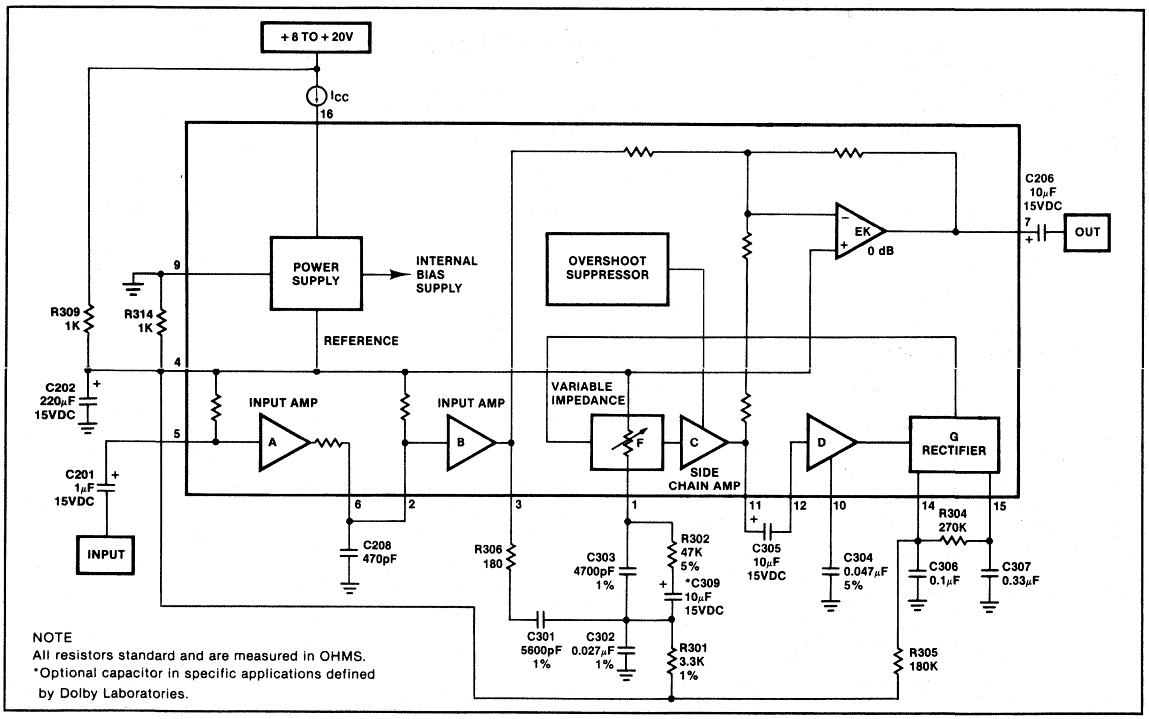
DOLBY B/C TYPE NOISE REDUCTION CIRCUIT NE650

DOLBY ENCODER Output for constant level input (single tone frequency response)

Frequency (kHz)	Input Level (dB)								
	0 (Dolby Level)	-5	-10	-15	-20	-25	-30	-35	-40
0.1	0	0.1	0	0.1	0	0	0	0	0
0.14	0	0.2	0.2	0.2	0.2	0.2	0.1	0.2	0.1
0.2	0	0.3	0.4	0.5	0.5	0.6	0.6	0.5	0.5
0.3	0	0.3	0.6	1.1	1.3	1.3	1.3	1.3	1.3
0.4					2.0	2.1	2.2	2.3	2.1
0.5	0	0.3	0.8	1.8	2.6	2.9	2.9	3.0	2.9
0.6						3.6	3.7	3.8	3.7
0.7	0	0.4	0.9	2.1	3.5	4.3	4.4	4.5	4.4
0.8						4.8	5.0	5.3	5.1
0.9							5.6	5.8	5.6
1.0	0	0.4	1.0	2.3	4.2	5.7	6.1	6.3	6.2
1.2							6.9	7.1	7.1
1.4	0	0.3	0.9	2.3	4.4	6.6	7.5	7.7	7.7
2.0	0.1	0.4	0.9	2.2	4.3	7.0	8.5	8.9	8.9
3.0	0.2	0.6	0.9	1.9	3.9	6.6	8.8	9.7	9.7
5.0	0.3	0.6	1.0	1.7	3.2	5.4	8.2	10.0	10.3
7.0	0.3	0.6	1.0	1.7	2.8	4.7	7.3	9.7	10.4
10.0	0.4	0.7	1.1	1.7	2.6	4.2	6.5	9.1	10.4
14.0	0.5	0.8	1.1	1.8	2.7	4.4	6.5	8.7	10.3
20.0	0.7	0.7	1.2	1.9	2.7	4.4	6.5	8.7	10.3

NOTE
The figures given in this table are the average response of many of Dolby Laboratories' professional encoders, and are not intended to be taken as required consumer equipment performance characteristics. Thus, no inference should be drawn on the tolerances which licensees must retain in consumer equipment. The figures can, however, be used to plot typical characteristics.

TEST CIRCUIT NE650



NOTE
All resistors standard and are measured in OHMS.
*Optional capacitor in specific applications defined by Dolby Laboratories.

Section 16
Phase Locked Loops

INDEX

Section 16 — Phase Locked Loops

PHASE-LOCKED LOOPS—SYMBOLS AND DEFINITIONS

T_A

Ambient temperature range. Range of the surrounding environment of the operating device.

T_J

Junction Temperature. The maximum temperature of the device. 150°C is standard for silicon devices.

T_{STG}

Storage temperature range. Temperature range that the device can be stored in a non-operating condition.

T_{SOLD}

Soldering Temperature. The temperature which can be applied to the lead frame of the device for short periods of time (normally specified for a duration of 10 sec).

Truth Tables

0 is logic level low
1 is logic level high
X - don't care condition - has no effect under circuit conditions listed.

Absolute Maximum Rating

Operating safe zones exceeding these limits could cause permanent damage to the device and are not meant to imply that devices can operate at these limits.

Power Dissipation

The power that the device can safely handle at 25°C. The dissipation must be derated as indicated for the individual package type.

Package Type Designation

See full package designations in Appendix.

V_{CC} ($-V_{CC}$)

Supply Voltage. The range of power supply voltage over which the device will operate safely.

FREE-RUNNING FREQUENCY (f_O', ω_O').

Also called the *center frequency*, this is the frequency at which the loop VCO operates when not locked to an input signal. The "prime" superscripts are used to distinguish the free-running frequency from f_O' and ω_O' which are used for the general oscillator frequency. (Many references use f_O' and ω_O' for both the free-running and general oscillator frequency and leave the proper choice for the reader to infer from the context). The appropriate units for f_O' and ω_O' are Hz and radians per second respectively.

LOCK RANGE ($2f_L$, $2\omega_L$).*

The range of frequencies over which the loop will remain in lock. Normally the lock range is centered at the free-running frequency unless there is some nonlinearity in the system which limits the frequency deviation on one side of f_O'. The deviations from f_O' are referred to as the *Tracking Range* or *Hold-in Range.* (See figure 1.6). The tracking range is therefore one-half of the lock range.

CAPTURE RANGE ($2f_C$, $2\omega_C$).**

Although the loop will remain in lock throughout its lock range, it may not be able to acquire lock at the tracking range extremes because of the selectivity afforded by the low-pass filter. The capture range also is centered at f_O' with the equal deviations called the *Lock-in* or *Pull-in Ranges.* The capture range can never exceed the lock range.

LOCK-UP TIME (t_L).***

The transient time required for a free-running loop to lock. This time depends principally upon the bandwidth selectivity designed into the loop with the low-pass filter. The lock-up time is inversely proportional to the selectivity bandwidth. Also, lock-up time exhibits a statistical spreading due to random initial phase relationships between the input and oscillator phases.

PHASE COMPARATOR CONVERSION GAIN (K_d).

The conversion constant relating the phase comparators output voltage to the phase difference between input and VCO signals when the loop is locked. At low input signal levels, K_d is also a function of signal amplitude. K_d has units of volts per radian (V/rad).

VCO CONVERSION GAIN (K_O).

The conversion constant relating the oscillators frequency shift from f_O' to the applied input voltage. K_O has units of radians per second per volt (rad/sec/volt). K_O is a linear function of ω_O' and must be obtained using a formula or graph provided or experimentally measured at the desired ω_O.

LOOP GAIN (K_V).

The product of K_d, K_O, and the low-pass filters gain at dc. K_d is evaluated at the appropriate input signal level and K_O at the appropriate ω_O'. K_V has units of $(\text{sec})^{-1}$.

CLOSED LOOP GAIN (CLG).

The output signal frequency and phase can be determined from a product of the CLG and the input signal where the CLG is given by

$$\text{CLG} = \frac{K_V}{1 + K_V} \qquad \text{(Equation 1.4)}$$

NATURAL FREQUENCY (ω_n).

The characteristic frequency of the loop, determined mathematically by the final pole positions in the complex plane or determined experimentally as the modulation frequency for which an underdamped loop gives the maximum frequency deviation from f_O' and at which the phase error swing is the greatest.

DAMPING FACTOR (ζ).

The standard damping constant of a second order feedback system. For the PLL, ζ refers to the ability of the loop to respond quickly to an input frequency step without excessive overshoot.

LOOP NOISE BANDWIDTH (B_L).

A loop property relating ω_n and τ which describes the effective bandwidth of the received signal. Noise and signal components outside this bandwidth are greatly attenuated.

* Also called Synchronization Range.
** Also called Acquisition Range.
*** Also called Acquisition Time.

NOTE
Refer to Section 10 of the 1979 Analog Applications Manual for an in-depth explanation of Phase Locked Loops and their applications.

PHASE LOCKED LOOP NE/SE564

DESCRIPTION

The NE564 is a versatile, high guaranteed frequency Phase Locked Loop designed for operation up to 50MHz. As shown in the block diagram, the NE564 consists of a VCO, limiter, phase comparator, and post detection processor.

APPLICATIONS

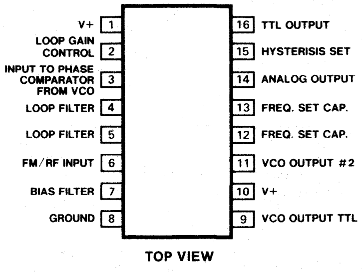
- **High speed modems**
- **FSK receivers and transmitters**
- **Frequency synthesizers**
- **Signal generators**
- **Various satcom/TV systems**

FEATURES

- **Operation with single 5V supply**
- **TTL compatible inputs and outputs**
- **Guaranteed operation to 50MHz**
- **External loop gain control**
- **Reduced carrier feedthrough**
- **No elaborate filtering needed in FSK applications**
- **Can be used as a modulator**
- **Variable loop gain (Externally Controlled)**

PIN CONFIGURATION

D, F, N PACKAGE



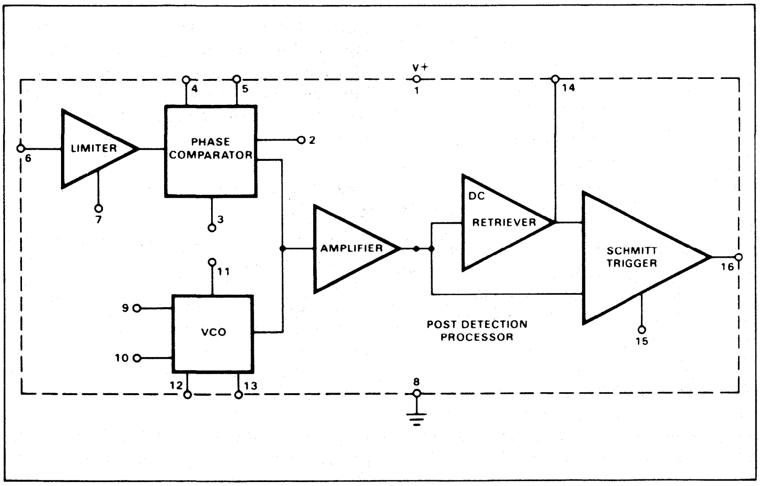
ORDER NUMBERS

NE/SE564F NE/SE564N
NE/SE564D

ABSOLUTE MAXIMUM RATINGS

PARAMETER			RATING	UNIT
V+	Supply voltage			V
	Pin 1		14	
	Pin 10		6	
P_D	Power dissipation		400	mW
T_A	Operating temperature	NE	0 to 70	°C
	Operating temperature	SE	−55 to +125	
t_{stg}	Storage temperature		−65 to 150	°C

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The NE564 is a monolithic phase locked loop with a post detection processor. The use of Schottky clamped transistors and optimized device geometries extends the frequency of operation to greater than 50MHz. In addition to the classical PLL applications, the NE564 can be used as a modulator with a controllable frequency deviation.

The output voltage of the PLL can be written as shown in the following equation:

$$V_O = \frac{(f_{in} - f_o)}{K_{vco}} \qquad \text{Equation 1}$$

K_{VCO} = conversion gain of the VCO (see figure 7)
f_{in} = frequency of the input signal
f_o = free running frequency of the VCO

The process of recovering FSK signals involves the conversion of the PLL output into logic compatible signals. For high data rates, a considerable amount of carrier will be present at the output of the PLL due to the wideband nature of the loop filter. To avoid the use of complicated filters, a comparator with hysterisis or Schmitt trigger is required. With the conversion gain of the VCO fixed, the output voltage as given by Equation 1 varies according to the frequency deviation of f_{in} from f_O. Since this differs from system to system, it is necessary that the hysterisis of the Schmitt trigger be capable of being changed, so that it can be optimized for a particular system. This is accomplished in the 564 by varying the voltage at pin 15 which results in a change of the hysterisis of the Schmitt trigger.

For FSK signals, an important factor to be considered is the drift in the free running frequency of the VCO itself. If this changes due to temperature, according to Equation 1 it will lead to a change in the dc levels of the

ELECTRICAL CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$, $f_o = 5MHz$, $I_B = 400\mu A$ unless otherwise specified

PARAMETER	TEST CONDITIONS	SE564			NE564			UNIT
		Min	Typ	Max	Min	Typ	Max	
VCO frequency	$C_1 = 6pF$	50	65		45	60		MHz
Lock range	Input ≥ 200mVrms $T_A = 25°C$	40	70		40	70		% of f_o
	$= 125°C$	20	30					
	$= -55°C$	70	90					
	$= 0°C$				50	70		
	$= 70°C$				25	40		
Capture range	Input ≥ 200mVrms, $R_2 = R_3 = 27\Omega$	20	30		20	30		% of f_o
VCO frequency drift with temperature	$f_o = 5MHz$, $T_A = -55°C$ to $125°C$		400	1000				PPM/°C
	$= 0°C$ to $70°C$					400	1250	
	$f_o = 500KHz$, $T_A = -55°C$ to $125°C$		250	500				
	$= 0°C$ to $70°C$					400	850	
VCO free running frequency	$f_o = \frac{1}{25R_CC_1}$, $C_1 = 80pF$ $R_C = 100\Omega$ "Internal"	4	5	6	3.5	5	7	MHz
VCO frequency change with supply voltage	$V_{CC} = 4.5V$ to $5.5V$		3	8		3	8	% of f_o
Demodulated output voltage	Modulation frequency: 1KHz $f_o = 5MHz$, input deviation:							
	$2\% T = 25°C$	18	24		18	24		mVrms
	$1\% T = 25°C$	8	14		8	14		mVrms
	$= 0°C$				9.0	13		mVrms
	$= -55°C$	6	10					mVrms
	$= 70°C$				11.0	15		mVrms
	$= 125°C$	12	16					mVrms
Distortion	Deviation: 1% to 8%		1			1		%
Signal to noise ratio	Std. condition, 1% to 10% dev.		40			40		dB
AM rejection	Std. condition, 30% AM		35			35		dB
Demodulated Output at operating voltage	Modulation frequency: 1KHz $f_o = 5MHz$, input deviation: 1%							
	$V_{CC} = 4.5V$	7	12		7	12		mVrms
	$V_{CC} = 5.5V$	8	14		8	14		mVrms
Supply current	$V_{CC} = 5V$ I_1, I_{10}		45	60		45	60	mA
Output								
"1" output leakage current	$V_{OUT} = 5V$, Pin 16, 9		1	20		1	20	μA
"0" output voltage	$I_{OUT} = 2mA$, Pin 16, 9		0.3	0.6		0.3	0.6	V
	$I_{OUT} = 6mA$, Pin 16, 9		0.4	0.8		0.4	0.8	V

PLL output, and consequently to errors in the digital output signal. This is especially true for narrow band signals where the deviation in f_{in} itself may be less than the change in f_o due to temperature. This effect can be eliminated if the dc or average value of the signal is retrieved and used as the reference to the comparator. In this manner, variations in the dc levels of the PLL output do not affect the FSK output.

VCO Section

Due to its inherent high frequency performance, an emitter coupled oscillator is used in the VCO. In the circuit, shown in the equivalent schematic, transistors Q_{21} and Q_{23} with current sources $Q_{25}-Q_{26}$ form the basic oscillator. The free running frequency of the oscillator is shown in the following equation:

$$f_o = \frac{1}{16R_cC_1} \qquad \text{Equation 2}$$

$R_c = R_{19} = R_{20} = 100\Omega$ (INTERNAL)
C_1 = external frequency setting capacitor

Variation of V_d (phase detector output voltage) changes the frequency of the oscillator. As indicated by Equation 2, the frequency of the oscillator has a negative temperature coefficient due to the positive temperature coefficient of the monolithic resistor. To compensate for this, a current I_R with negative temperature coefficient is introduced to achieve a low frequency drift with temperature.

Phase Comparator Section

The phase comparator consists of a double balanced modulator with a limiter amplifier to improve AM rejection. Schottky clamped vertical PNPs are used to obtain TTL level inputs. The loop gain can be varied by changing the current in Q_4 and Q_{15} which effectively changes the gain of the differential amplifiers. This can be accomplished by introducing a current at pin 2.

Post Detection Processor Section

The post detection processor consists of a unity gain transconductance amplifier and comparator. The amplifier can be used as a dc retriever for demodulation of FSK signals, and as a post detection filter for linear FM demodulation. The comparator has adjustable hysterisis so that phase jitter in the output signal can be eliminated.

As shown in the equivalent schematic, the dc retriever is formed by the transductance amplifier $Q_{42}-Q_{43}$ together with an external capacitor which is connected at the amplifier output (pin 14). This forms an integrator whose output voltage is shown in the following equation:

$$V_O = \frac{g_m}{C_2} V_{in}dt \qquad \text{Equation 3}$$

g_m = transconductance of the amplifier
C_2 = capacitor at the output (pin 14)
V_{in} = signal voltage at amplifier input

With proper selection of C_2, the integrator time constant can be varied so that the output voltage is the dc or average value of the input signal for use in FSK, or as a post detection filter in linear demodulation.

The comparator with hysterisis is made up of $Q_{49}-Q_{50}$ with positive feedback being provided by $Q_{47}-Q_{48}$. The hysterisis is varied by changing the current in Q_{52} with a resulting variation in the loop gain of the comparator. This method of hysterisis control, which is a dc control, provides symmetric variation around the nominal value.

Design Formula

The free running frequency of the VCO is shown by the following equation:

$$f_o = \frac{1}{16R_cC_1} \text{ in Hz} \qquad \text{Equation 4}$$

R_c = 100Ω
C_1 = external cap in farads

The loop filter diagram shown is explained by the following equation:

$$F(s) = \frac{1}{1 + sRC_3} \qquad \text{Equation 5}$$

$R = R_{12} = R_{13} = 1.3\text{k}\Omega$ (INTERNAL)

By adding capacitors to pins 4 and 5, two poles are added to the loop transfer function

at $\omega = \frac{1}{RC_3}$.

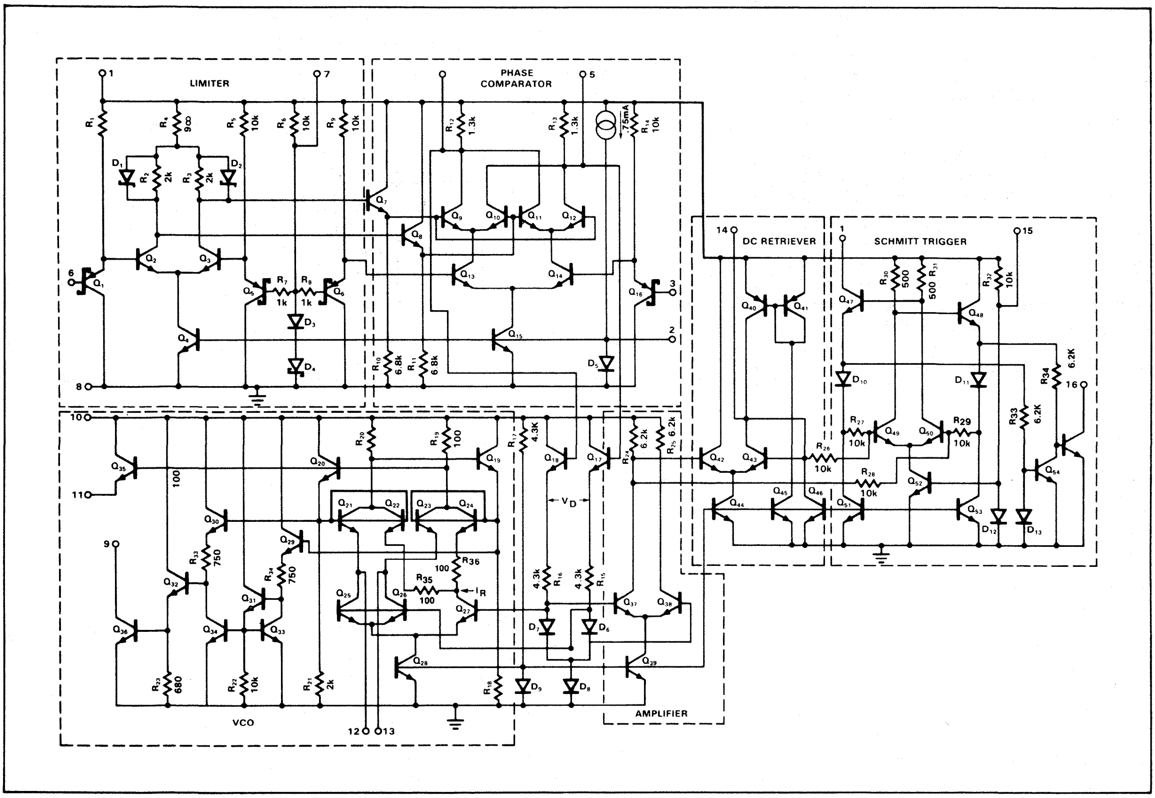
FM DEMODULATOR

The NE564 can be used as an FM demodulator. The connections for operation at 5V and 12V are shown in figures 2 and 3 respectively. The input signal is ac coupled with the output signal being extracted at pin 14. Loop filtering is provided by the capacitors at pins 4 and 5 with additional filtering being provided by the capacitor at pin 14. Since the conversion gain of the VCO is not very high, to obtain sufficient demodulated output signal the frequency deviation in the input signal should be fairly high (1% or higher).

MODULATION TECHNIQUES

The NE564 phase locked loop can be modulated at either the loop filter ports (pins 4 and 5) or the input port (pin 6) as shown in figure 4. The approximate modulation frequency can be determined from the frequency conversion gain curve shown in figure 5. This curve will be appropriate for signals injected into pins 4 and 5 as shown in figure 4.

EQUIVALENT SCHEMATIC



FSK Demodulation

The 564 PLL is particularly attractive for FSK demodulation since it contains an internal voltage comparator and VCO which have TTL compatible inputs and outputs, and it can operate from a single 5 volt power supply. Demodulated dc voltages associated with the mark and space frequencies are recovered with a single external capacitor in a dc retriever without utilizing extensive filtering networks. An internal comparator, acting as a Schmitt trigger with an adjustable hysteresis, shapes the demodulated voltages into compatible TTL output levels. The high frequency design of the 564 enables it to demodulate FSK at high data rates in excess of 1.0M baud.

Figure 6 shows a high-frequency FSK decoder designed for input frequency deviations of ± 1.0MHz centered around a free-running frequency of 10.8MHz. The value of the timing capacitance required was estimated from figure 8 to be approximately 40pF. A trimmer capacitor was added to fine tune f_O' to 10.8MHz.

Figure 9 indicates that the ± 1.0MHz frequency deviations will be within the lock range for input signal levels greater than approximately 50mV with zero pin 2 bias current. While strictly this figure is appropriate only for 5MHz, it can be used as a guide for lock range estimates at other f_O' frequencies.

The hysteresis was adjusted experimentally via the 10kΩ potentiometer and 2kΩ bias arrangement to give the waveshape shown in figure 7 for 20K, 500K, 2M baud rates with square wave FSK modulation. Note the magnitude and phase relationships of the phase comparators output voltages with respect to each other and to the FSK output. The high frequency sum components of the input and VCO frequency also are visible as noise on the phase comparators outputs.

SE/NE 564 TEST CIRCUIT

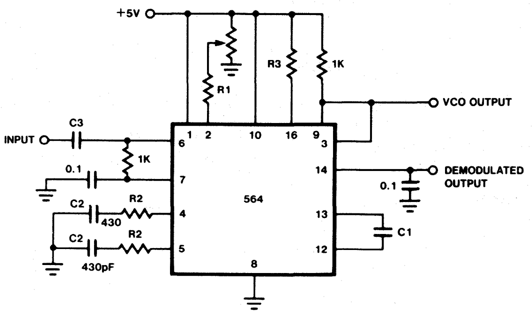


Figure 1

FM DEMODULATOR AT 5V

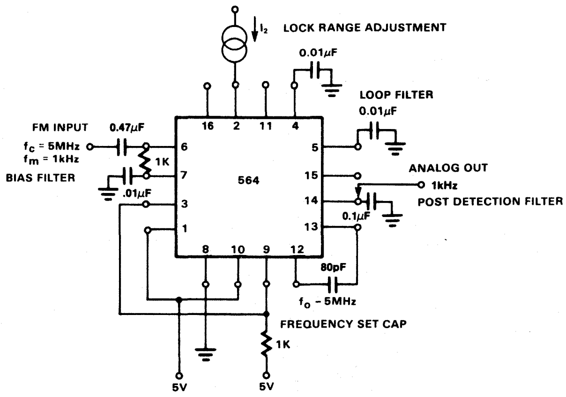


Figure 2

FM DEMODULATOR AT 12V

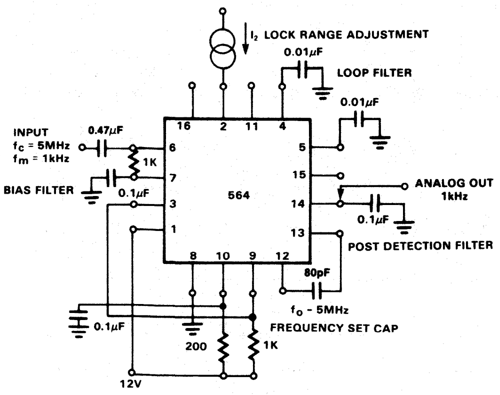


Figure 3

MODULATOR

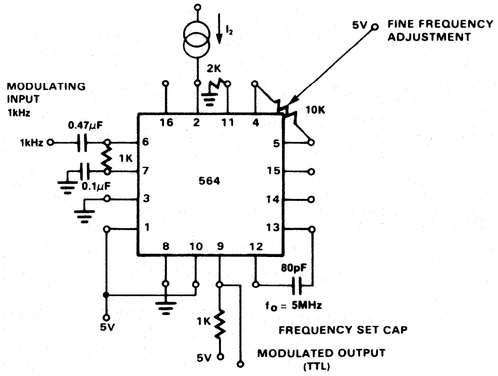
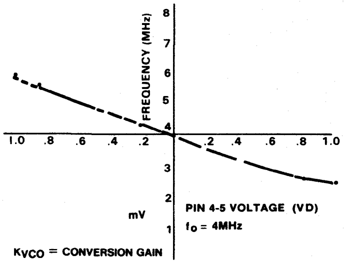


Figure 4

VCO CONVERSION GAIN



K_{VCO} = CONVERSION GAIN

$$K_{VCO} = \frac{\Delta f}{\Delta V_D} \simeq -1.8 \frac{MHz}{V}$$

FOR K_0 OF PLL MODEL

$$K_0 = \frac{(\Delta f/fo)}{VOLT} = \frac{-(1.8MHz/4MHz)}{1VOLT}$$

$$= \frac{-0.45 \text{ RADIANS}}{VOLT}$$

$$= -4.5x10^{-4} \text{ RADIANS/mV}$$

Figure 5

10.8MHz FSK DECODER USING THE 564

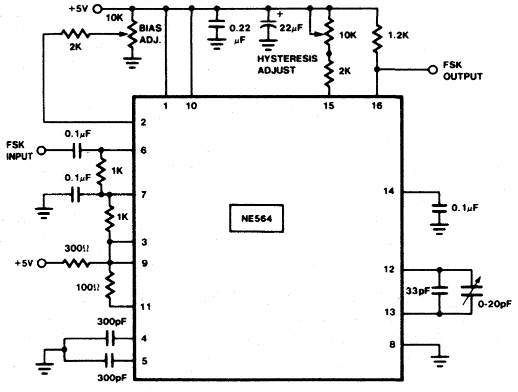
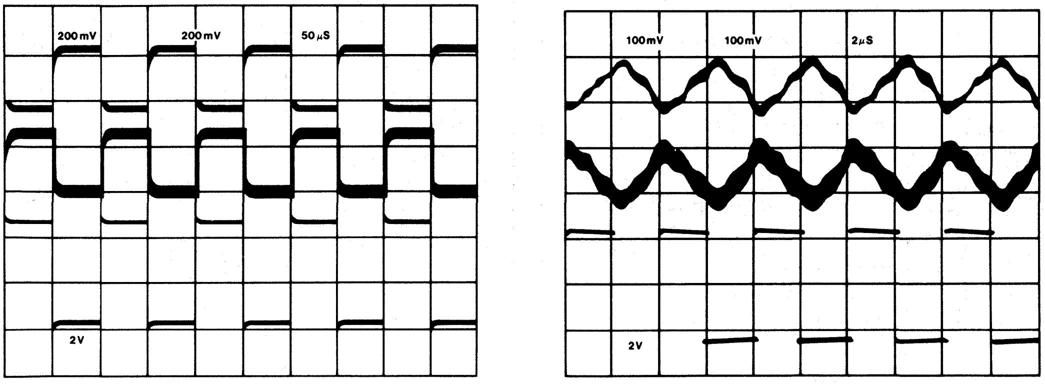


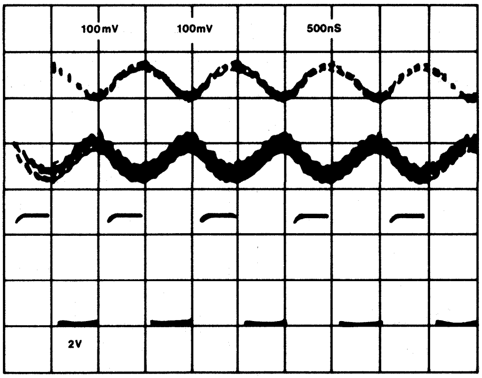
Figure 6

PHASE COMPARATOR (PINS 4 AND 5) AND FSK (PIN 16) OUTPUTS FOR DATA RATES OF



(a) 20K BAUD

(b) 500K BAUD



NOTE
Top trace-pin 4
Center trace-pin 5
Bottom trace-pin 16

(c) 2.0M BAUD

Figure 7

TYPICAL PERFORMANCE CHARACTERISTICS

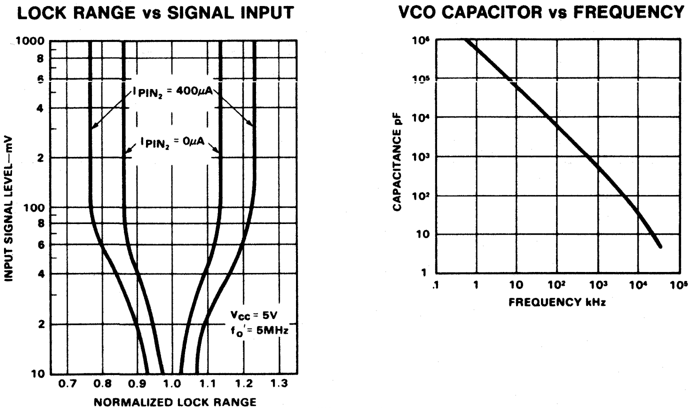
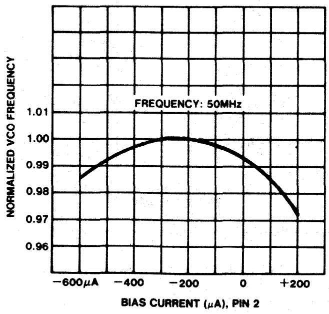
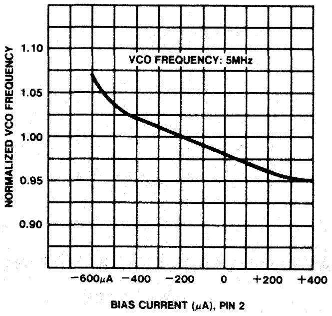


Figure 8

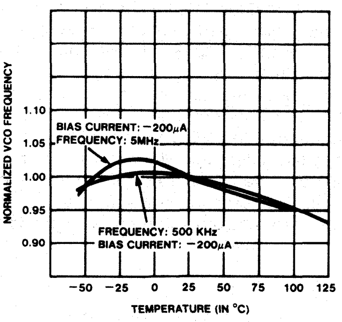
TYPICAL NORMALIZED VCO FREQUENCY AS A FUNCTION OF PIN 2 BIAS CURRENT



TYPICAL NORMALIZED VCO FREQUENCY AS A FUNCTION OF PIN 2 BIAS CURRENT



NORMALIZED VCO FREQUENCY AS A FUNCTION OF TEMPERATURE



16

PHASE LOCKED LOOP NE/SE565

DESCRIPTION

The SE/NE565 Phase-Locked Loop (PLL) is a self-contained, adaptable filter and demodulator for the frequency range from 0.001Hz to 500kHz. The circuit comprises a voltage-controlled oscillator of exceptional stability and linearity, a phase comparator, an amplifier and a low-pass filter as shown in the block diagram. The center frequency of the PLL is determined by the free-running frequency of the VCO; this frequency can be adjusted externally with a resistor or a capacitor. The low-pass filter, which determines the capture characteristics of the loop, is formed by an internal resistor and an external capacitor.

FEATURES

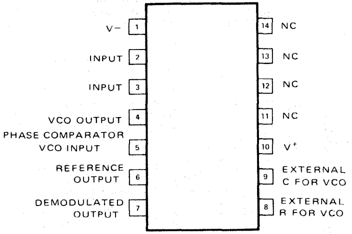
- **Highly stable center frequency (200ppm/°C typ.)**
- **Wide operating voltage range (±6 to ±12 volts)**
- **Highly linear demodulated output (0.2% typ.)**
- **Center frequency programming by means of a resistor or capacitor, voltage or current**
- **TTL and DTL compatible square-wave output; loop can be opened to insert digital frequency divider**
- **Highly linear triangle wave output**
- **Reference output for connection of comparator in frequency discriminator**
- **Bandwidth adjustable from < ±1% to > ±60%**
- **Frequency adjustable over 10 to 1 range with same capacitor**

APPLICATIONS

- **Frequency shift keying**
- **Modems**
- **Telemetry receivers**
- **Tone decoders**
- **SCA receivers**
- **Wideband FM discriminators**
- **Data synchronizers**
- **Tracking filters**
- **Signal restoration**
- **Frequency multiplication & division**

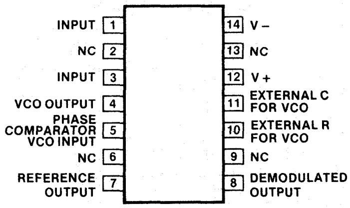
PIN CONFIGURATIONS

F,N PACKAGE



TOP VIEW
ORDER NUMBER
NE/SE565F,N

D PACKAGE

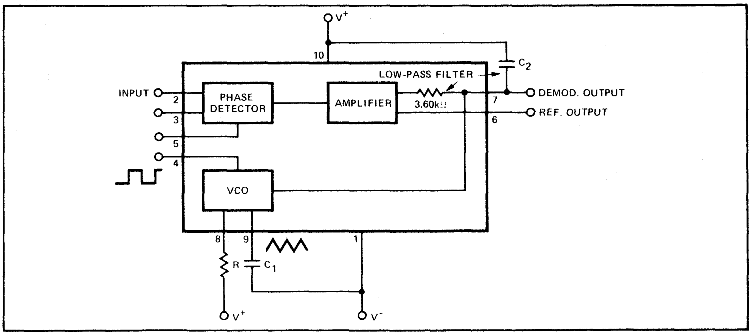


TOP VIEW
ORDER NUMBER
NE/SE565D

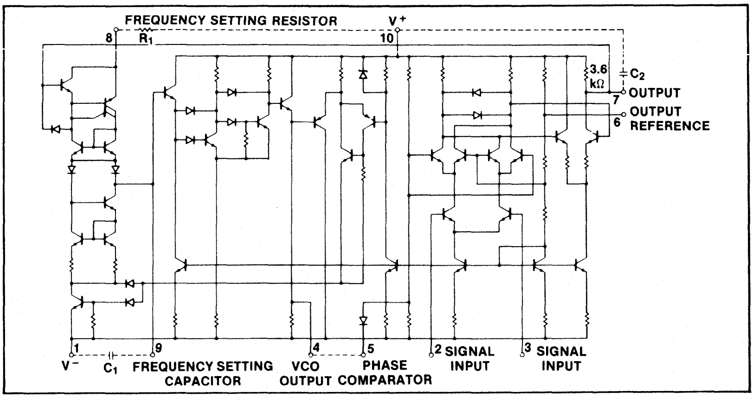
ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$ unless otherwise specified.

PARAMETER	RATING	UNIT
Maximum operating voltage	26	V
Input voltage	3	Vp-p
Storage temperature	-65 to +150	°C
Operating temperature range		
NE565	0 to +70	°C
SE565	-55 to +125	°C
Power dissipation	300	mW

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = ±6V unless otherwise specified.

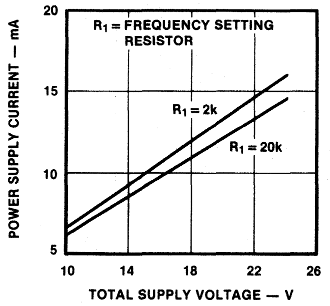
PARAMETER	TEST CONDITIONS	SE565			NE565			UNIT
		Min	Typ	Max	Min	Typ	Max	
SUPPLY REQUIREMENTS								
Supply voltage		12		±12	±6		±12	V
Supply current			8	12.5		8	12.5	mA
INPUT CHARACTERISTICS								
Input impedance[1]		7	10		5	10		kΩ
Input level required for tracking	f_o = 50kHz, ±10% frequency deviation	10	1		10	1		mVrms
VCO CHARACTERISTICS								
Center frequency								
Maximum value	C_1 = 300pF	300	500			500		kHz
Distribution[2]	Distribution taken about f_o = 50kHz, R_1 = 5.0kΩ, C_1 = 1200pF	-10	0	+10	-30	0	+30	%
Drift with temperature	f_o = 50kHz		200			300		ppm/°C
Drift with supply voltage	f_o = 50kHz, V_{CC} = ±6 to ±7 volts		0.1	1.0		0.2	1.5	%/V
Triangle wave								
Output voltage level		1.9	0		1.9	0		V
Amplitude			2.4	3		2.4	3	Vp-p
Linearity			0.2			0.5		%
Square wave								
Logical "1" output voltage	f_o = 50kHz	+4.9	+5.2		+4.9	+5.2		V
Logical "0" output voltage	f_o = 50kHz		-0.2	+0.2		-0.2	+0.2	V
Duty cycle	f_o = 50kHz	45	50	55	40	50	60	%
Rise time			20	100		20		ns
Fall time			50	200		50		ns
Output current (sink)		0.6	1		0.6	1		mA
Output current (source)		5	10		5	10		mA
DEMODULATED OUTPUT CHARACTERISTICS								
Output voltage level	Measured at pin 7	4.25	4.5	4.75	4.0	4.5	5.0	V
Maximum voltage swing[3]			2			2		Vp-p
Output voltage swing	±10% frequency deviation	250	300		200	300		mVp-p
Total harmonic distortion			0.2	0.75		0.4	1.5	%
Output impedance[4]			3.6			3.6		kΩ
Offset voltage (V6-V7)			30	100		50	200	mV
Offset voltage vs temperature (drift)			50			100		µV/°C
AM rejection		30	40			40		dB

NOTES

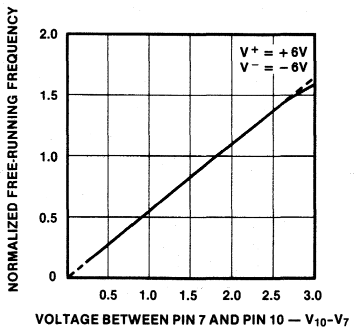
1. Both input terminals (pins 2 and 3) must receive identical dc bias. This bias may range from 0 volts to -4 volts.
2. The external resistance for frequency adjustment (R1) must have a value between 2kΩ and 20kΩ.
3. Output voltage swings negative as input frequency increases.
4. Output not buffered.

PHASE LOCKED LOOP NE/SE565

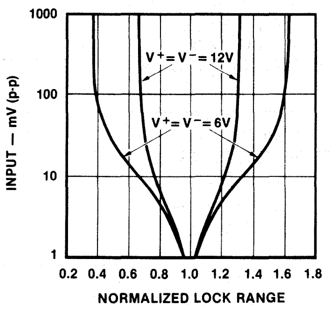
TYPICAL PERFORMANCE CHARACTERISTICS



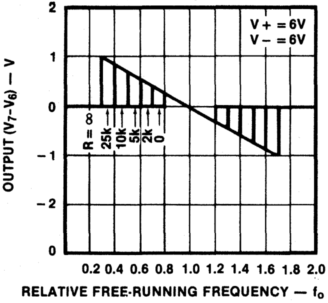
POWER SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



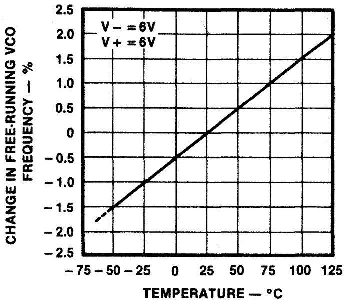
VCO CONVERSION GAIN



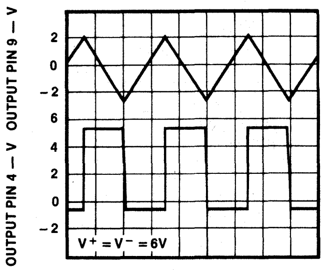
LOCK RANGE AS A FUNCTION OF INPUT VOLTAGE



LOCK RANGE AS A FUNCTION OF GAIN SETTING RESISTANCE (PIN 6-7)



CHANGE IN FREE-RNNING VCO FREQUENCY AS A FUNCTION OF TEMPERATURE



VCO OUTPUT WAVEFORM

DESIGN FORMULAS (See Figure 1)

Free-running frequency of VCO: $f_o \approx \frac{1.2}{4R_1C_1}$ in Hz

Lock-range: $f_L = \pm \frac{8f_o}{V_{CC}}$ in Hz

Capture-range: $f_C \approx \pm \frac{1}{2\pi}\sqrt{\frac{2\pi f_L}{\tau}}$

where $\tau = (3.6X10^3) X C_2$

TYPICAL APPLICATIONS

FM Demodulation

The 565 Phase Locked Loop is a general purpose circuit designed for highly linear FM demodulation. During lock, the average dc level of the phase comparator output signal is directly proportional to the frequency of the input signal. As the input frequency shifts, it is this output signal which causes the VCO to shift its frequency to match that of the input. Consequently, the linearity of the phase comparator output with frequency is determined by the voltage-to-frequency transfer function of the VCO.

Because of its unique and highly linear VCO, the 565 PLL can lock to and track an input signal over a very wide bandwidth (typically ±60%) with very high linearity (typically, within 0.5%).

A typical connection diagram is shown in Figure 1. The VCO free-running frequency is given approximately by

$f_o = \frac{1.2}{4R_1C_1}$ and should be adjusted to be at the center of the input signal frequency range. C1 can be any value, but R1 should be within the range of 2000 to 20,000 ohms with an optimum value on the order of 4000 ohms. The source can be direct coupled if the dc resistances seen from pins 2 and 3 are equal and there is no dc voltage difference between the pins. A short between pins 4 and 5 connects the VCO to the phase comparator. Pin 6 provides a dc reference voltage that is close to the dc potential of the demodulated output (pin 7). Thus, if a resistance is connected between pins 6 and 7, the gain of the output stage can be reduced with little change in the dc voltage level at the output. This allows the lock range to be decreased with little change in the free-running frequency. In this manner the lock range can be decreased from ±60% of f_o to approximately ±20% of f_o (at ±6V).

A small capacitor (typically 0.001μF) should be connected between pins 7 and 8 to eliminate possible oscillation in the control current source.

A single-pole loop filter is formed by the capacitor C2, connected between pin 7 and the positive supply, and an internal resistance of approximately 3600 ohms.

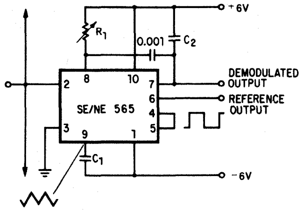


Figure 1

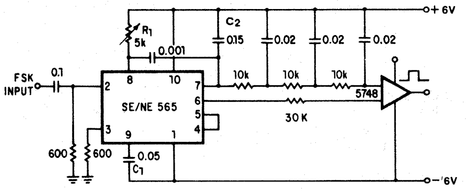


Figure 2

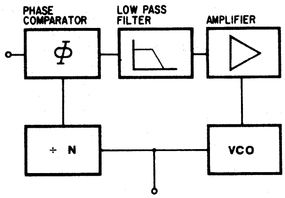


Figure 3

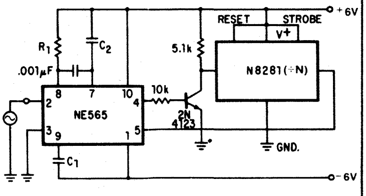


Figure 4

Frequency Shift Keying (FSK)

FSK refers to data transmission by means of a carrier which is shifted between two preset frequencies. This frequency shift is usually accomplished by driving a VCO with the binary data signal so that the two resulting frequencies correspond to the "0" and "1" states (commonly called space and mark) of the binary data signal.

A simple scheme using the 565 to receive FSK signals of 1070Hz and 1270Hz is shown in Figure 2. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding dc shift at the output.

The loop filter capacitor C2 is chosen smaller than usual to eliminate overshoot on the output pulse, and a three-stage RC ladder filter is used to remove the carrier component from the output. The band edge of the ladder filter is chosen to be approximately half way between the maximum keying rate (in this case 300 baud or 150Hz) and twice the input frequency (approximately 2200Hz). The output signal can now be made logic compatible by connecting a voltage comparator between the output and pin 6 of the loop. The free-running frequency is adjusted with R1 so as to result in a slightly-positive voltage at the output with $f_{IN} = 1070$Hz.

The input connection is typical for cases where a dc voltage is present at the source and therefore a direct connection is not desirable. Both input terminals are returned to ground with identical resistors (in this case, the values are chosen to effect a 600-ohm input impedance).

Frequency Multiplication

There are two methods by which frequency multiplication can be achieved using the 565:

1. Locking to a harmonic of the input signal.
2. Inclusion of a digital frequency divider or counter in the loop between the VCO and phase comparator.

The first method is the simplest, and can be achieved by setting the free-running frequency of the VCO to a multiple of the input frequency. A limitation of this scheme is that the lock range decreases as successively higher and weaker harmonics are used for locking. If the input frequency is to be constant with little tracking required, the loop can generally be locked to any one of the first 5 harmonics. For higher orders of multiplication, or for cases where a large lock range is desired, the second scheme is more desirable. An example of this might be a case where the input signal varies over a wide frequency range and a large multiple of the input frequency is required.

A block diagram of the second scheme is shown in Figure 3. Here the loop is broken between the VCO and the phase comparator, and a frequency divider is inserted. The fundamental of the divided VCO frequency is locked to the input frequency in this case, so that the VCO is actually running at a multiple of the input frequency. The amount of multiplication is determined by the frequency divider. A typical connection scheme is shown in Figure 4. To set up the circuit, the frequency limits of the input signal must be determined. The free-running frequency of the VCO is then adjusted by means of R1 and C1 (as discussed under FM demodulation) so that the output frequency of the divider is midway between the input frequency limits. The filter capacitor, C2, should be large enough to eliminate variations in the demodulated output voltage (at pin 7), in order to stabilize the VCO frequency. The output can now be taken as the VCO squarewave output, and its fundamental will be the desired multiple of the input frequency (f_{IN}) as long as the loop is in lock.

SCA (Background Music) Decoder

Some FM stations are authorized by the FCC to broadcast uninterrupted background music for commerical use. To do this a frequency modulated subcarrier of 67kHz is used. The frequency is chosen so as not to interfere with the normal stereo or monaural program; in addition, the level of the subcarrier is only 10% of the amplitude of the combined signal.

The SCA signal can be filtered out and demodulated with the NE565 Phase Locked Loop without the use of any resonant circuits. A connection diagram is shown in Figure 5. This circuit also serves as an example of operation from a single power supply.

A resistive voltage divider is used to establish a bias voltage for the input (pins 2 and 3). The demodulated (multiplex) FM signal is fed to the input through a two-stage high-pass filter, both to effect capacitive coupling and to attenuate the strong signal of the regular channel. A total signal amplitude, between 80mV and 300mV, is required at the input. Its source should have an impedance of less than 10,000 ohms.

The Phase Locked Loop is tuned to 67kHz with a 5000 ohm potentiometer; only approximate tuning is required, since the loop will seek the signal.

The demodulated output (pin 7) passes through a three-stage low-pass filter to provide de-emphasis and attenuate the high-frequency noise which often accompanies SCA transmission. Note that no capacitor is provided directly at pin 7; thus, the circuit is operating as a first-order loop. The demodulated output signal is in the order of 50mV and the frequency response extends to 7kHz.

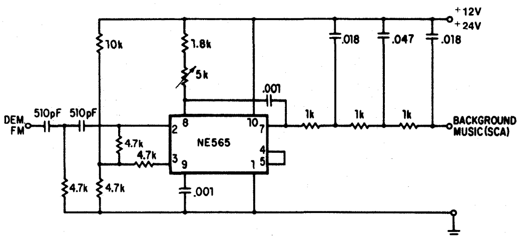

+12V
+24V
10k
1.8k
5k
.018
.047
.018
.001
DEM. FM
510pF
510pF
1k
1k
1k
BACKGROUND MUSIC (SCA)
NE565
2
8
10
7
4
5
3
9
1
4.7k
4.7k
4.7k
4.7k
.001

Figure 5

FUNCTION GENERATOR NE/SE566

DESCRIPTION

The NE/SE 566 Function Generator is a voltage controlled oscillator of exceptional linearity with buffered square wave and triangle wave outputs.The frequency of oscillation is determined by an external resistor and capacitor and the voltage applied to the control terminal. The oscillator can be programmed over a ten to one frequency range by proper selection of an external resistance and modulated over a ten to one range by the control voltage, with exceptional linearity.

FEATURES

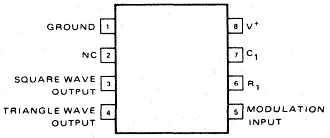
- **Wide range of operating voltage (up to 24 volts)**
- **High linearity of modulation**
- **Highly stable center frequency (200 ppm/°C typical)**
- **Highly linear triangle wave output**
- **Frequency programming by means of a resistor or capacitor, voltage or current**
- **Frequency adjustable over 10 to 1 range with same capacitor**

APPLICATIONS

- **Tone generators**
- **Frequency shift keying**
- **FM modulators**
- **Clock generators**
- **Signal generators**
- **Function generators**

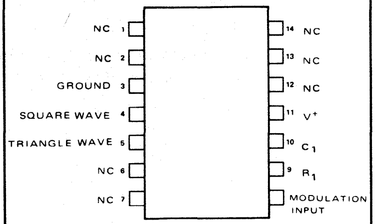
PIN CONFIGURATIONS

N PACKAGE



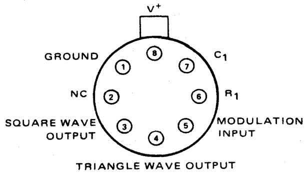
TOP VIEW
ORDER NUMBERS
NE/SE566N

F PACKAGE



TOP VIEW
ORDER NUMBERS
NE/SE566F

H PACKAGE*

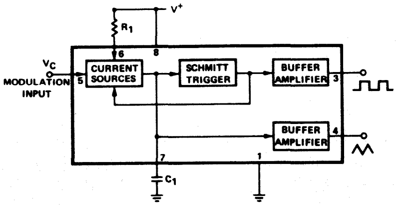


ORDER NUMBERS
NE/SE566H
*Metal cans (H) not recommended for new designs

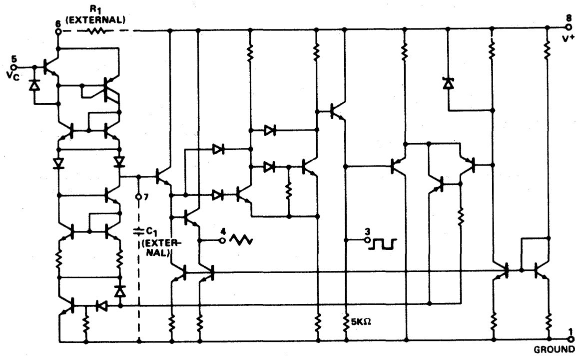
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Maximum operating voltage	26	V
Input voltage	3	V_{P-P}
Storage temperature	-65 to +150	°C
Operating temperature range		
NE566	0 to +70	°C
SE566	-55 to +125	°C
Power dissipation	300	mW

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



FUNCTION GENERATOR NE/SE566

ELECTRICAL CHARACTERISTICS $T_A = 25°C$; $V_{CC} = 12V$ unless otherwise specified.

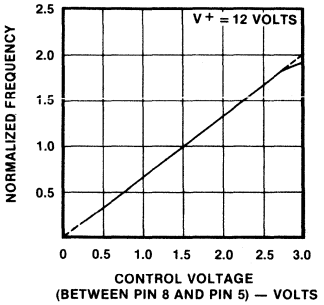
PARAMETER	SE566			NE566			UNIT
	Min	Typ	Max	Min	Typ	Max	
GENERAL							
Operating temperature range	-55		125	0		70	°C
Operating supply voltage			24			24	V
Operating supply current		7	12.5		7	12.5	mA
VCO[1]							
Maximum operating frequency		1			1		MHz
Frequency drift with temperature		200			300		ppm/°C
Frequency drift with supply voltage		1			2		%/V
Control terminal input impedance[2]		1			1		MΩ
FM distortion (±10% deviation)		0.2	0.75		0.4	1.5	%
Maximum sweep rate		1			1		MHz
Sweep range		10:1			10:1		
OUTPUT							
Triangle wave output							
Impedance		50			50		Ω
Voltage	1.9	2.4		1.9	2.4		Vpp
Linearity		0.2			0.5		%
Square wave input							
Impedance		50			50		Ω
Voltage	5	5.4		5	5.4		Vpp
Duty Cycle	45	50	55	40	50	60	%
Rise time		20			20		ns
Fall Time		50			50		ns

NOTES

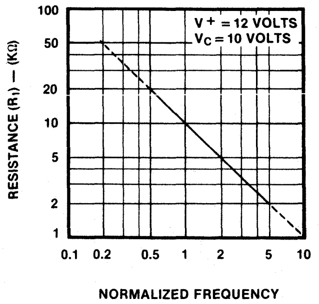
1. The external resistance for frequency adjustment (R_1) must have a value between 2kΩ and 20KΩ.
2. The bias voltage (V_C) applied to the control terminal (pin 5) should be in the range $3/4V^+ \leq V_C \leq V^+$.

TYPICAL PERFORMANCE CHARACTERISTICS

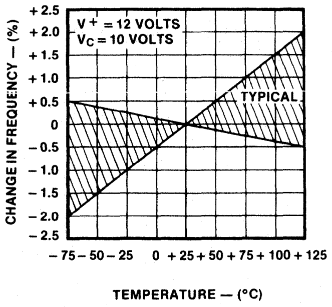
NORMALIZED FREQUENCY AS A FUNCTION OF CONTROL VOLTAGE



NORMALIZED FREQUENCY AS A FUNCTION OF RESISTANCE (R1)



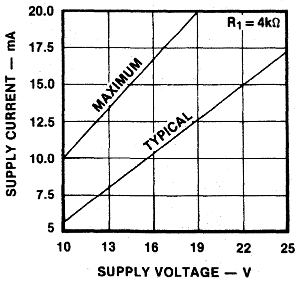
CHANGE IN FREQUENCY AS A FUNCTION OF TEMPERATURE



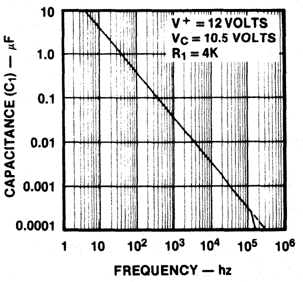
FUNCTION GENERATOR NE/SE566

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

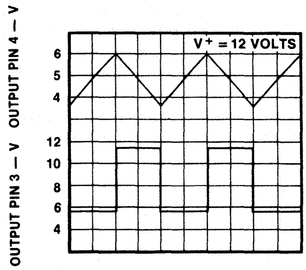
POWER SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



FREQUENCY AS A FUNCTION OF CAPACITANCE (C1)



VCO OUTPUT WAVEFORMS



OPERATING INSTRUCTIONS

The SE/NE 566 Function Generator is a general purpose voltage controlled oscillator designed for highly linear frequency modulation. The circuit provides simultaneous square wave and triangle wave outputs at frequencies up to 1MHz. A typical connection diagram is shown in Figure 1. The control terminal (pin 5) must be biased externally with a voltage (V_C) in the range

$$3/4\ V^+ \leq V_C \leq V^+$$

where V_{CC} is the total supply voltage. In Figure 1, the control voltage is set by the voltage divider formed with R_2 and R_3. The modulating signal is then ac coupled with the capacitor C_2. The modulating signal can be direct coupled as well, if the appropriate dc bias voltage is applied to the control terminal. The frequency is given approximately by

$$f_O \simeq \frac{2[(V^+) - (V_C)]}{R_1 C_1 V^+}$$

and R_1 should be in the range $2k\Omega < R_1 < 20k\Omega$.

A small capacitor (typically 0.001μf) should be connected between pins 5 and 6 to eliminate possible oscillation in the control current source.

If the VCO is to be used to drive standard logic circuitry, it may be desirable to use a dual supply of ±5 volts as shown in Figure 2. In this case the square wave output has the proper dc levels for logic circuitry. RTL can be driven directly from pin 3. For DTL or T^2L gates, which require a current sink of more than 1mA, it is usually necessary to connect a 5kΩ resistor between pin 3 and negative supply. This increases the current sinking capability to 2mA. The third type of interface shown uses a saturated transistor between the 566 and the logic circuitry. This scheme is used primarily for T^2L circuitry which requires a fast fall time (<50ns) and a large current sinking capability.

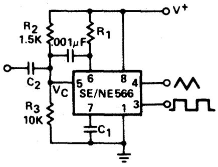


FIGURE 1

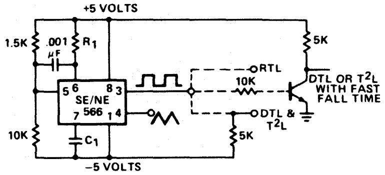


FIGURE 2

ANALOG DIVISION MARCH 1982

TONE DECODER/PHASE LOCKED LOOP NE/SE567

DESCRIPTION

The SE/NE567 tone and frequency decoder is a highly stable phase-locked loop with synchronous AM lock detection and power output circuitry. Its primary function is to drive a load whenever a sustained frequency within its detection band is present at the self-biased input. The bandwidth center frequency, and output delay are independently determined by means of four external components.

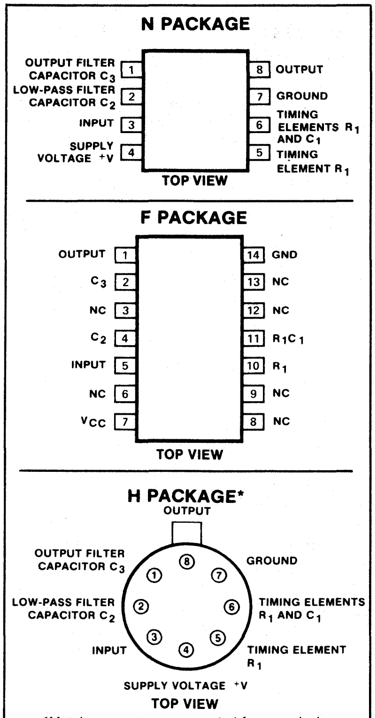
FEATURES

- **Wide frequency range (.01Hz to 500kHz)**
- **High stability of center frequency**
- **Independently controllable bandwidth (up to 14 percent)**
- **High out-band signal and noise rejection**
- **Logic-compatible output with 100mA current sinking capability**
- **Inherent immunity to false signals**
- **Frequency adjustment over a 20 to 1 range with an external resistor**
- **Military processing available**

APPLICATIONS

- **Touch Tone® decoding**
- **Carrier current remote controls**
- **Ultrasonic controls (remote TV, etc.)**
- **Communications paging**
- **Frequency monitoring and control**
- **Wireless intercom**
- **Precision oscillator**

PIN CONFIGURATIONS

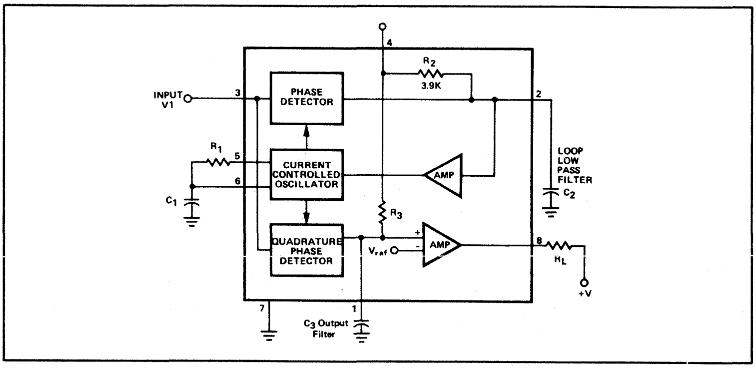


*Metal cans not recommended for new designs

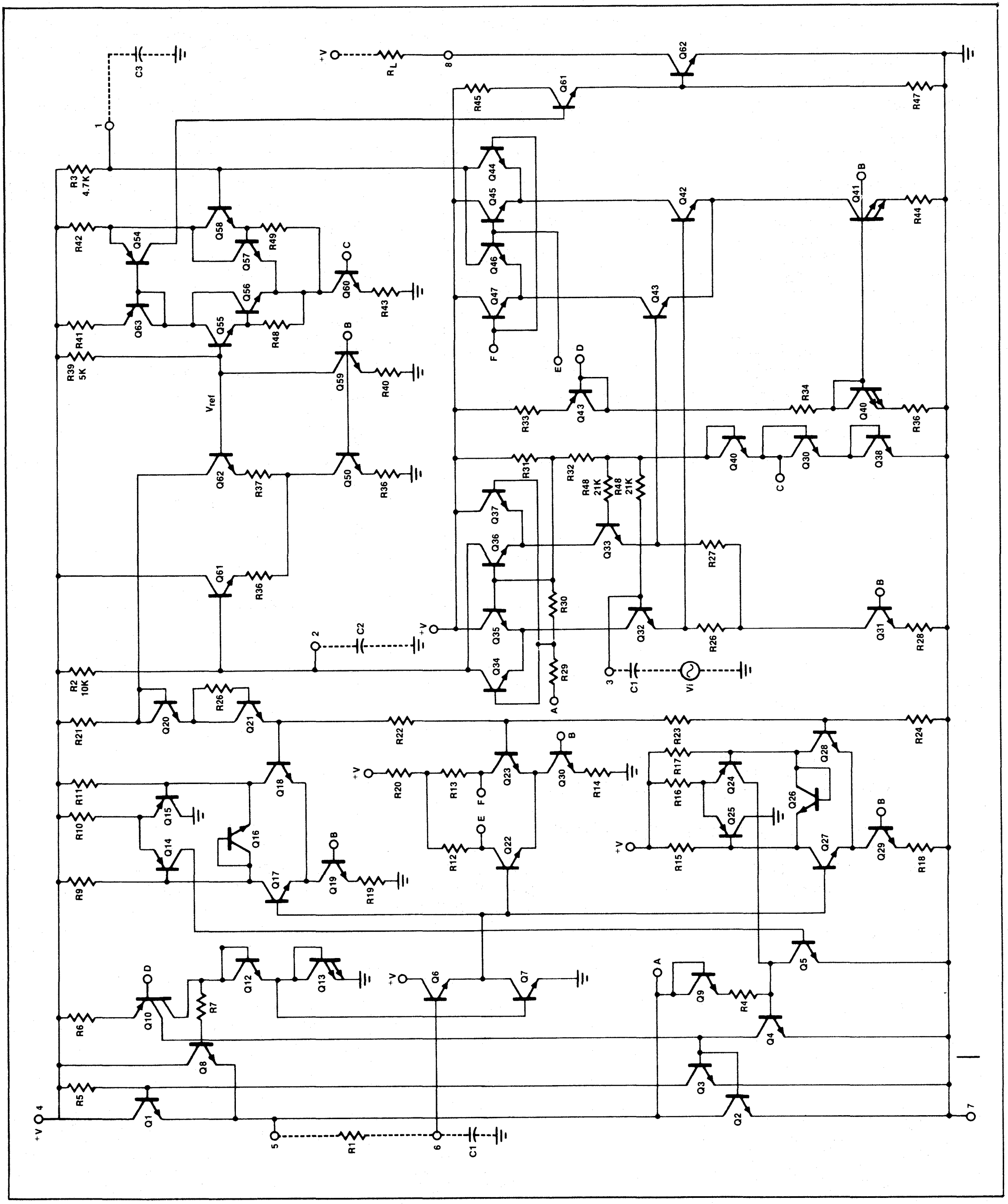
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Operating temperature		
NE567	0 to +70	°C
SE567	-55 to +125	°C
Operating voltage	10	V
Positive voltage at input	0.5 + Vs	V
Negative voltage at input	-10	Vdc
Output voltage (collector of output transistor)	15	Vdc
Storage temperature	-65 to +150	°C
Power dissipation	300	mW

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



TONE DECODER/PHASE LOCKED LOOP NE/SE567

DC ELECTRICAL CHARACTERISTICS (V+ = 5.0V; T_A = 25°C unless otherwise specified.)

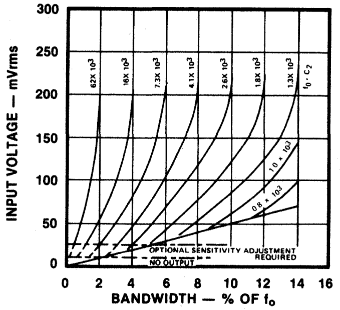
PARAMETER	TEST CONDITIONS	SE567			NE567			UNIT
		Min	Typ	Max	Min	Typ	Max	
CENTER FREQUENCY[1]								
Highest center frequency (f_o)		100	500		100	500		kHz
Center frequency stability[2]	-55 to +125°C		35±140			35±140		ppm/°C
	0 to +70°C		35±60			35±60		ppm/°C
Center frequency shift with supply voltage	f_o = 100kHz		0.5	1		0.7	2	%/V
DETECTION BANDWIDTH								
Largest detection bandwidth	f_o = 100kHz	12	14	16	10	14	18	% of f_o
Largest detection bandwidth skew			2	4		3	6	% of f_o
Largest detection bandwidth—variation with temperature	V_i = 300mVrms		±0.1			±0.1		%/°C
Largest detection bandwidth—variation with supply voltage	V_i = 300mVrms		±2			±2		%/V
INPUT								
Input resistance			20			20		kΩ
Smallest detectable input voltage (V_i)	I_L = 100mA, $f_i = f_o$		20	25		20	25	mVrms
Largest no-output input voltage	I_L = 100mA, $f_i = f_o$	10	15		10	15		mVrms
Greatest simultaneous outband signal to inband signal ratio			+6			+6		dB
Minimum input signal to wideband noise ratio	B_n = 140kHz		-6			-6		dB
OUTPUT								
Fastest on-off cycling rate			f_o/20			f_o/20		
"1" output leakage current			0.01	25		0.01	25	µA
"0" output voltage	I_L = 30mA		0.2	0.4		0.2	0.4	V
	I_L = 100mA		0.6	1.0		0.6	1.0	V
Output fall time[3]	R_L = 50Ω		30			30		ns
Output rise time[3]	R_L = 50Ω		150			150		ns
GENERAL								
Operating voltage range		4.75		9.0	4.75		9.0	V
Supply current quiescent			6	8		7	10	mA
Supply current—activated	R_L = 20kΩ		11	13		12	15	mA
Quiescent power dissipation			30			35		mW

NOTES

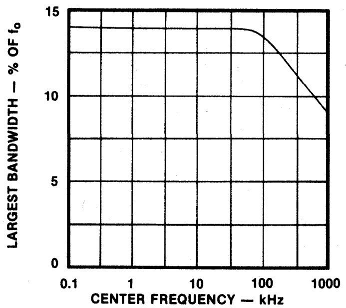
1. Frequency determining resistor R_1 should be between 1 and 20kΩ.
2. Applicable over 4.75 to 5.75 volts. See graphs for more detailed information.
3. Pin 8 to Pin 1 feedback R_L network selected to eliminate pulsing during turn-on and turn-off.

TYPICAL PERFORMANCE CHARACTERISTICS

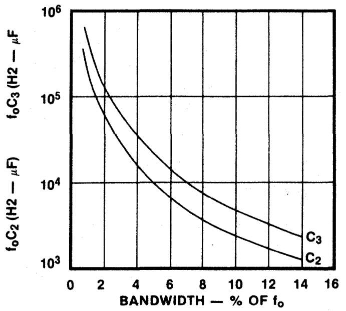
BANDWIDTH vs INPUT SIGNAL AMPLITUDE



LARGEST DETECTION BANDWIDTH vs OPERATING FREQUENCY

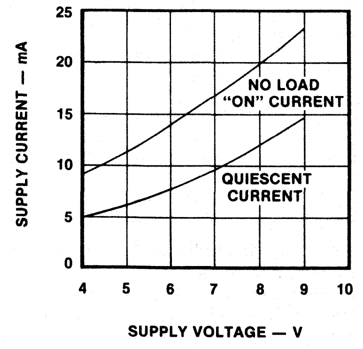


DETECTION BANDWIDTH AS A FUNCTION OF C2 and C3

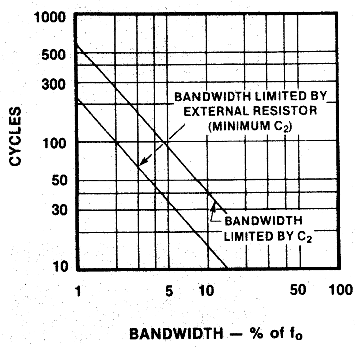


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

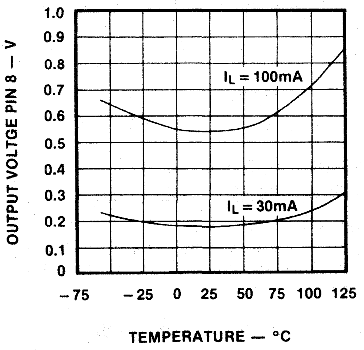
TYPICAL SUPPLY CURRENT vs SUPPLY VOLTAGE



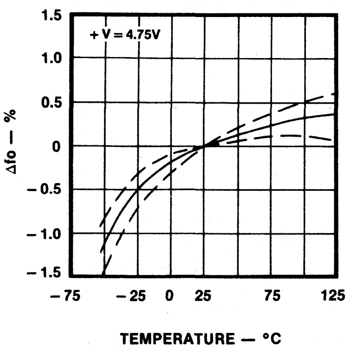
GREATEST NUMBER OF CYCLES BEFORE OUTPUT



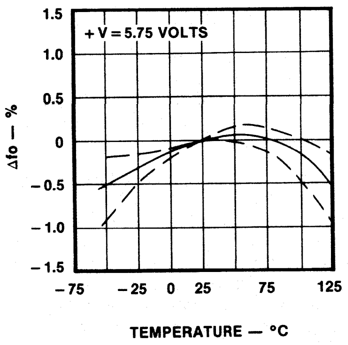
TYPICAL OUTPUT VOLTAGE vs TEMPERATURE



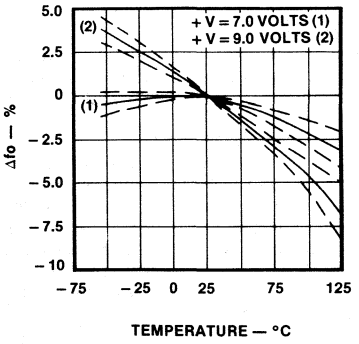
TYPICAL FREQUENCY DRIFT WITH TEMPERATURE (MEAN AND S.D.)



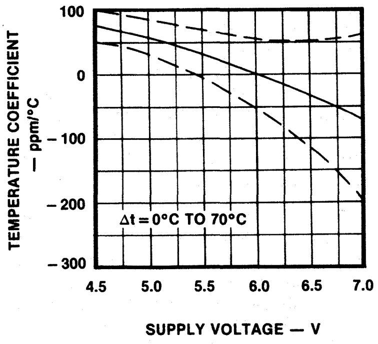
TYPICAL FREQUENCY DRIFT WITH TEMPERATURE (MEAN AND S.D.)



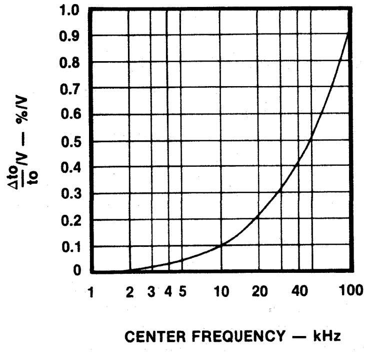
TYPICAL FREQUENCY DRIFT WITH TEMPERATURE (MEAN AND S.D.)



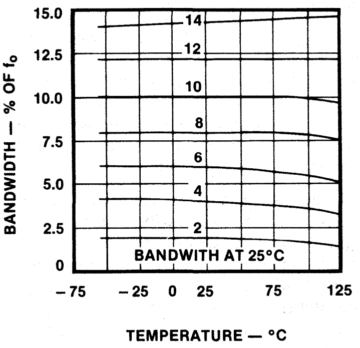
CENTER FREQUENCY TEMPERATURE COEFFICIENT (MEAN AND S.D.)



CENTER FREQUENCY SHIFT WITH SUPPLY VOLTAGE CHANGE vs OPERATING FREQUENCY



TYPICAL BANDWIDTH VARIATION WITH TEMPERATURE



TONE DECODER/PHASE LOCKED LOOP NE/SE567

DESIGN FORMULAS

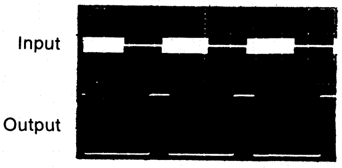
$$f_0 \simeq \frac{1.1}{R_1C_1}$$

$$BW \simeq 1070\sqrt{\frac{V_I}{f_0C_2}} \text{ in \% of } f_0,\ V_i \leq 200\text{mVrms}$$

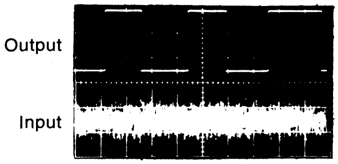
Where

V_i = Input Voltage (Vrms)
C_2 = Low-Pass Filter Capacitor (μF)

TYPICAL RESPONSE



Response to 100mVrms tone burst.
R_L = 100 ohms.



Response to same input tone burst with wideband noise.
$\frac{S}{N}$ = -6db R_L = 100 ohms
Noise Bandwidth = 140Hz

PHASE LOCKED LOOP TERMINOLOGY CENTER FREQUENCY (fo)

The free-running frequency of the current controlled oscillator (CCO) in the absence of an input signal.

Detection Bandwidth (BW)

The frequency range, centered about f_o, within which an input signal above the threshold voltage (typically 20mVrms) will cause a logical zero state on the output. The detection bandwidth corresponds to the loop capture range.

Lock Range

The largest frequency range within which an input signal above the threshold voltage will hold a logical zero state on the output.

Detection Band Skew

A measure of how well the detection band is centered about the center frequency, f_0. The skew is defined as $(f_{max} + f_{min} - 2f_o)/2f_o$ where fmax and fmin are the frequencies corresponding to the edges of the detection band. The skew can be reduced to zero if necessary by means of an optional centering adjustment.

OPERATING INSTRUCTIONS

Figure 1 shows a typical connection diagram for the 567. For most applications, the following three-step procedure will be sufficient for choosing the external components R_1, C_1, C_2 and C_3.

1. Select R_1 and C_1 for the desired center frequency. For best temperature stability, R_1 should be between 2K and 20K ohm, and the combined temperature coefficient of the R_1C_1 product should have sufficient stability over the projected temperature range to meet the necessary requirements.

2. Select the low pass capacitor, C_2, by referring to the Bandwidth versus Input Signal Amplitude graph. If the input amplitude variation is known, the appropriate value of f_oC_2 necessary to give the desired bandwidth may be found. Conversely, an area of operation may be selected on this graph and the input level and C_2 may be adjusted accordingly. For example, constant bandwidth operation requires that input amplitude be above 200mVrms. The bandwidth, as noted on the graph, is then controlled solely by the f_oC_2 product (f_o (Hz), C_2 (μ fd)).

3. The value of C_3 is generally non-critical. C_3 sets the band edge of a low pass filter which attenuates frequencies outside the detection band to elminate spurious outputs. If C_3 is too small, frequencies just outside the detection band will switch the output stage on and off at the beat frequency, or the output may pulse on and off during the turn-on transient. If C_3 is too large, turn-on and turn-off of the output stage will be delayed until the voltage on C_3 passes the threshold voltage. (Such delay may be desirable to avoid spurious outputs due to translent frequencies.) A typical minimum value for C_3 is $2C_2$.

AVAILABLE OUTPUTS (Figure 2)

The primary output is the uncommitted output transistor collector, pin 8. When an in-band input signal is present, this transistor saturates; its collector voltage being less than 1.0 volt (typically 0.6V) at full output current (100mA). The voltage at pin 2 is the phase detector output which is a linear function of frequency over the range of 0.95 to 1.05 f_o with a slope of about 20mV per percent of frequency deviation. The average voltage at pin 1 is, during lock, a function of the inband input amplitude in accordance with the transfer characteristic given. Pin 5 is the controlled oscillator square wave output of magnitude $(+V - 2V_{be}) \approx (+V - 1.4V)$ having a dc average of +V/2. A 1kΩ load may be driven from pin 5. Pin 6 is an exponential triangle of 1 volt peak-to-peak with an average dc level of +V/2. Only high impedance loads may be connected to pin 6 without affecting the CCO duty cycle or temperature stability.

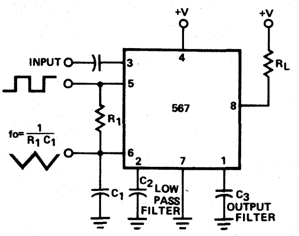


Figure 1

OPERATING PRECAUTIONS

A brief review of the following precautions will help the user achieve the high level of performance of which the 567 is capable.

1. Operation in the high input level mode (above 200mV) will free the user from bandwidth variations due to changes in the in-band signal amplitude. The input stage is now limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the in-band signal is suppressed. Also, the limiting action will create in-band components from sub-harmonic signals, so the 567 becomes sensitive to signals at $f_o/3$, $f_o/5$, etc.

2. The 567 will lock onto signals near $(2n + 1) f_o$, and will give an output for signals near $(4n + 1) f_o$ where n = 0, 1, 2, etc. Thus, signals at $5f_o$ and $9f_o$ can cause an unwanted output. If such signals are anticipated, they should be attenuated before reaching the 567 input.

3. Maximum immunity from noise and out-band signals is afforded in the low input level (below 200mVrms) and reduced bandwidth operating mode. However, decreased loop damping causes the worse-case lock-up time to increase, as shown by the Greatest Number of Cycles Before Output vs Bandwidth graph.

4. Due to the high switching speeds (20ns) associated with 567 operation, care should be taken in lead routing. Lead lengths should be kept to a minimum. The power supply should be adequately bypassed close to the 567 with a 0.01μF or greater capacitor; grounding paths should be carefully chosen to avoid ground loops and

unwanted voltage variations. Another factor which must be considered is the effect of load energization on the power supply. For example, an incandescent lamp typically draws 10 times rated current at turn-on. This can cause supply voltage fluctuations which could, for example, shift the detection band of narrow-band systems sufficiently to cause momentary loss of lock. The result is a low-frequency oscillation into and out of lock. Such effects can be prevented by supplying heavy load currents from a separate supply or increasing the supply filter capacitor.

SPEED OF OPERATION

Minimum lock-up time is related to the natural frequency of the loop. The lower it is, the longer becomes the turn-on transient. Thus, maximum operating speed is obtained when C_2 is at a minimum. When the signal is first applied, the phase may be such as to initially drive the controlled oscillator away form the incoming frequency rather than toward it. Under this condition, which is of course unpredictable, the lock-up transient is at its worst and the theoretical minimum lock-up time is not achievable. We must simply wait for the transient to die out.

The following expressions give the values of C_2 and C_3 which allow highest operating speeds for various band center frequencies. The minimum rate at which digital information may be detected without information loss due to the turn-on transient or output chatter is about 10 cycles per bit, corresponding to an information transfer rate of $f_o/10$ baud.

$$C_2 = \frac{130}{f_o} \mu F$$

$$C_3 = \frac{260}{f_o} \mu F$$

In cases where turn-off time can be sacrificed to achieve fast turn-on, the optional sensitivity adjustment circuit can be used to move the quiescent C_3 voltage lower (closer to the threshold voltage). However, sensitivity to beat frequencies, noise and extraneous signals will be increased.

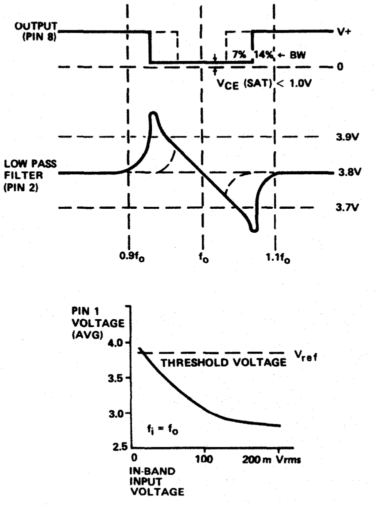


Figure 2

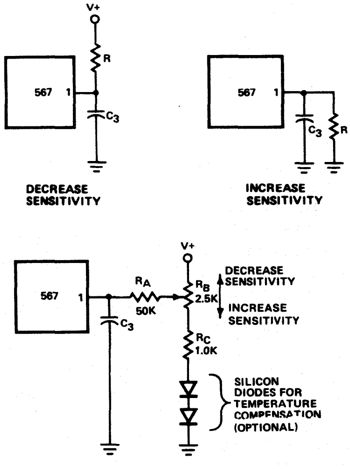


Figure 3

OPTIONAL CONTROLS (Figure 3)

The 567 has been designed so that, for most applications, no external adjustments are required. Certain applications, however, will be greatly facilitated if full advantage is taken of the added control possibilities available through the use of additional external components. In the diagrams given, typical values are suggested where applicable. For best results the resistors used, except where noted, should have the same temperature coefficient. Ideally, silicon diodes would be low-resistivity types, such as forward-biased transistor base-emmiter junctions. However, ordinary low-voltage diodes should be adequate for most applications.

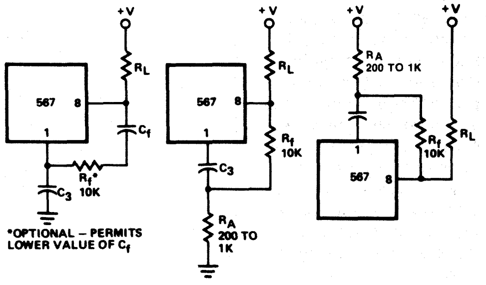


Figure 4

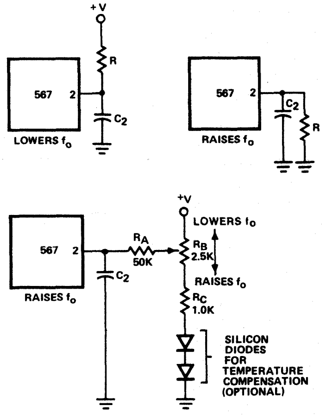


Figure 5

SENSITIVITY ADJUSTMENT

(Figure 3)

When operated as a very narrow band detector (less than 8 percent), both C_2 and C_3 are made quite large in order to improve noise and outband signal rejection. This will inevitably slow the response time. If, however, the output stage is biased closer to the threshold level, the turn-on time can be improved. This is accomplished by drawing additional current to terminal 1. Under this condition, the 567 will also give an output for lower-level signals (10mV or lower).

By adding current to terminal 1, the output stage is biased further away from the threshold voltage. This is most useful when, to obtain maximum operating speed, C_2 and C_3 are made very small. Normally, frequencies just outside the detection band could cause false outputs under this condition. By desensitizing the output stage, the outband beat notes do not feed through to the output stage. Since the input level must be somewhat greater when the output stage is made less sensitive, rejection of third harmonics or in-band harmonics (of lower frequency signals) is also improved.

CHATTER PREVENTION (Figure 4)

Chatter occurs in the output stage when C_3 is relatively small, so that the lock transient and the AC components at the quadrature phase detector (lock detector) output cause the output stage to move through its threshold more than once. Many loads, for example lamps and relays, will not respond to the chatter. However, logic may recognize the chatter as a series of outputs. By feeding the output stage output back to its input (pin 1) the chatter can be eliminated. Three schemes for doing this are given in Figure 4. All operate by feeding the first output step (either on or off) back to the input, pushing the input past the threshold until the transient conditions are over. It is only necessary to assure that the feedback time constant is not so large as to prevent operation at the highest anticipated speed. Although chatter can always be eliminated by making C_3 large, the feedback circuit will enable faster operation of the 567 by allowing C_3 to be kept small. Note that if the feedback time constant is made quite large, a short burst at the input frequency can be stretched into a long output pulse. This may be useful to drive, for example, stepping relays.

DETECTION BAND CENTERING (OR SKEW) ADJUSTMENT

(Figure 5)

When it is desired to alter the location of the detection band (corresponding to the loop capture range) within the lock range, the circuits shown above can be used. By moving the detection band to one edge of the range, for example, input signal variations will expand the detection band in only one direction. This may prove useful when a strong but undesirable signal is expected on one side or the other of the center frequency. Since R_B also alters the duty cycle slightly, this method may be used to obtain a precise duty cycle when the 567 is used as an oscillator.

ALTERNATE METHOD OF BANDWIDTH REDUCTION

(Figure 6)

Although a large value of C_2 will reduce the bandwidth, it also reduces the loop damping so as to slow the circuit response time. This may be undesirable. Bandwidth can be reduced by reducing the loop gain. This scheme will improve damping and permit faster operation under narrow-band conditions. Note that the reduced impedance level at terminal 2 will require that a larger value of C_2 be used for a given filter cutoff frequency. If more than three 567s are to be used, the network of R_B and R_C can be eliminated and the R_A resistors connected together. A capacitor between this junction and ground may be required to shunt high frequency components.

OUTPUT LATCHING (Figure 7)

To latch the output on after a signal is received, it is necessary to provide a feedback resistor around the output stage (between pins 8 and 1). Pin 1 is pulled up to unlatch the output stage.

REDUCTION OF C1 VALUE

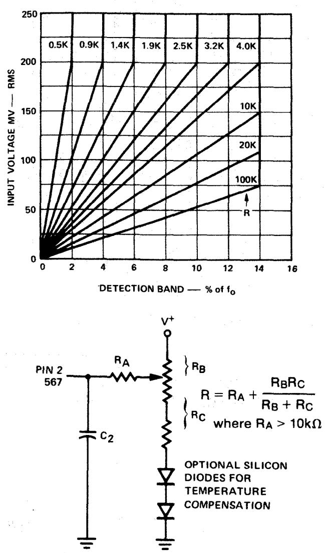
(Figure 8)

For precision very low-frequency applications, where the value of C_1 becomes large, an overall cost savings may be achieved by inserting a voltage follower between the R_1 C_1 junction and pin 6, so as to allow a higher value of R_1 and a lower value of C_1 for a given frequency.

TONE DECODER/PHASE LOCKED LOOP NE/SE567

PROGRAMMING

To change the center frequency, the value of R_1 can be changed with a mechanical or solid state switch, or additional C_1 capacitors may be added by grounding them through saturating npn transistors.



$$\frac{130}{f_o}\left(\frac{10K + R}{R}\right) < C_2 < \frac{1300}{f_o}\left(\frac{10K + R}{R}\right)$$

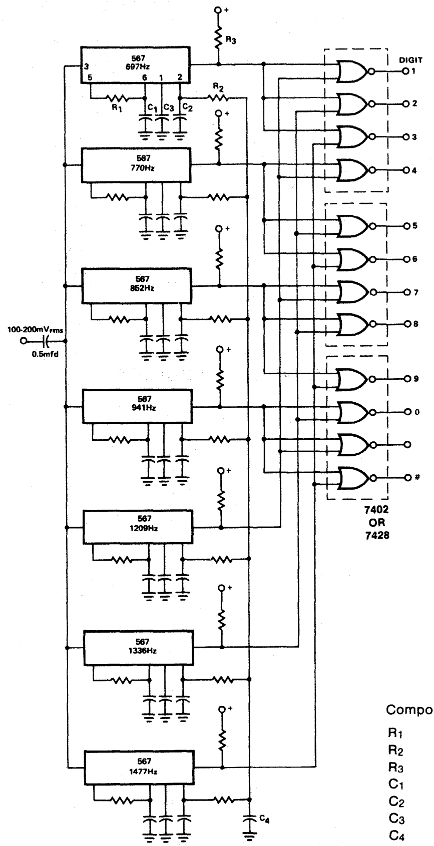
NOTE

Adjust control for symmetry of detection band edges about f_o.

Figure 6

TYPICAL APPLICATIONS

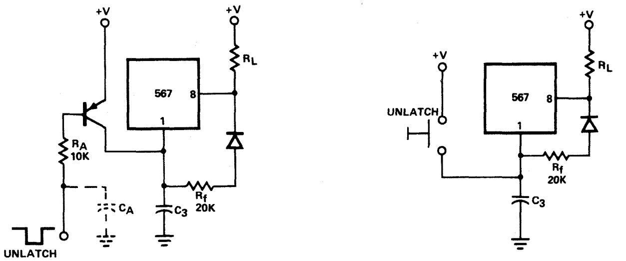
TOUCH-TONE® DECODER



Component values (Typical)

R_1	6.8 to 15K ohm
R_2	4.7K ohm
R_3	20K ohm
C_1	0.10mfd
C_2	1.0mfd 5V
C_3	2.2mfd 6V
C_4	250 μF 6V

OUTPUT LATCHING



C_A prevents latch-up when power supply is turned on.

Figure 7

PRECISION VLF

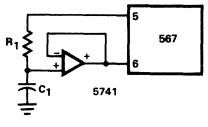
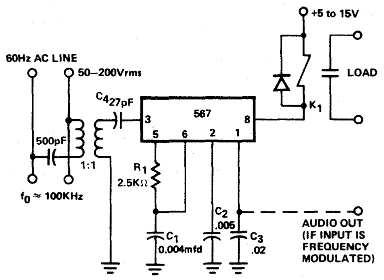


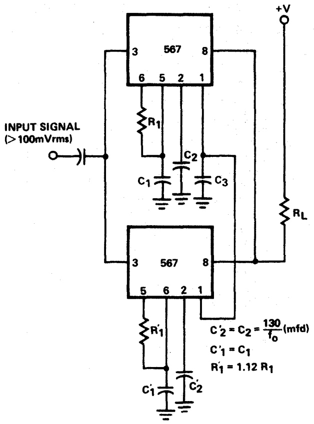
Figure 8

TYPICAL APPLICATIONS (Cont'd)

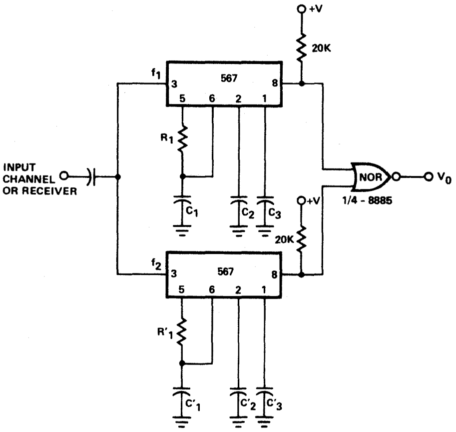
CARRIER-CURRENT REMOTE CONTROL OR INTERCOM



24% BANDWIDTH TONE DECODER

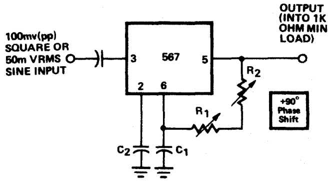


DUAL-TONE DECODER



1. Resistor and capacitor values chosen for desired frequencies and bandwidth.
2. If C_3 is made large so as to delay turn-on of the top 567, decoding of sequential (f_1 f_2) tones is possible.

0° to 180° PHASE SHIFTER

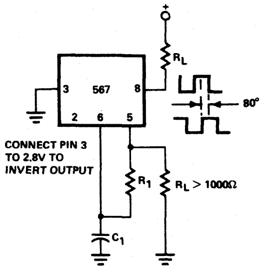


$R_2 \approx R_1/5$

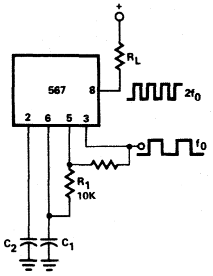
Adjust R_1 so that $\phi = 90°$ with control midway

TYPICAL APPLICATIONS (Cont'd)

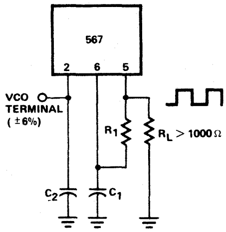
OSCILLATOR WITH QUADRATURE OUTPUT



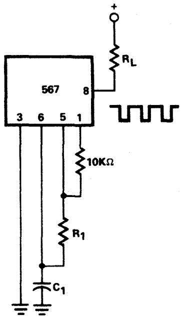
OSCILLATOR WITH DOUBLE FREQUENCY OUTPUT



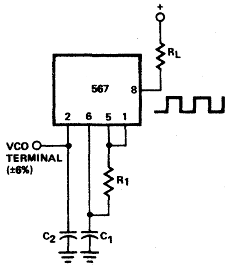
PRECISION OSCILLATOR WITH 20ns SWITCHING



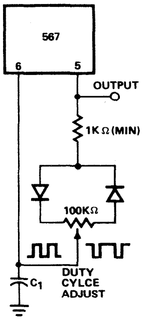
PULSE GENERATOR WITH 25% DUTY CYCLE



PRECISION OSCILLATOR TO SWITCH 100ma LOADS



PULSE GENERATOR



NOTE

Application information available on request.

Section 17
Military

INDEX

Section 17 — Military

MILITARY PRODUCTS/PROCESS LEVELS

The Signetics MIL 38510/883 Program is organized to provide a broad selection of processing options, structured around the most commonly requested customer flows. The program is designed to provide our customers:

- Fully compliant 883 flows on all products.
- Standard processing flows to help minimize the need for custom specs.
- Cost savings realized by using standard processing flows in lieu of custom flows.
- Better delivery lead times by minimizing spec negotiation time, plus allows customer to buy product off-the-shelf or in various stages of production rather than waiting for devices started specifically to custom specs.

The following explains the different processing options available to you. Special device marking clearly distinguishes the type of screening performed. Refer to Tables 2, 3, 4 and 5.

JAN QUALIFIED (JB)

JAN Qualified product is designed to give you the optimum in quality and reliability. The JAN processing level is offered as the result of the government's product standardization programs, and is monitored by the Defense Electronic Supply Center (DESC), through the use of industry-wide procedures and specifications.

JAN Qualified products are manufactured, processed and tested in a government certified facility to Mil-M 38510, and appropriate device slash sheet specifications. Design documentation, lot sampling plans, electrical test data and qualification data for each specific part type ~~has~~ been approved by the Defense Electronic Supply Center (DESC) and products appear on the DESC Qualified Products List (QPL-38510).

Group B testing, per Mil-Std-883 Method 5005, is performed on each six weeks of production on each slash sheet for each package type. Group C, per Mil-Std-883 Method 5005, is performed every ninety days for each microcircuit group. Group D testing, per Mil-Std-883 Method 5005, is performed every six months for each package type.

In addition to the common specs used throughout the industry for processing and testing, JAN Qualified products also possess a requirement for a standard marking used throughout the IC industry.

JAN CASE OUTLINE AND LEAD FINISH	SIGNETICS MILITARY PACKAGE TYPES						
	CAN		DUAL-IN-LINE				
	8-PIN	10-PIN	8-PIN	14-PIN	16-PIN	18-PIN	24-PIN
PB	—	—	FE	—	—	—	—
CB	—	—	—	F	—	—	—
EB	—	—	—	—	F	—	—
JB	—	—	—	—	—	—	F
DB	—	—	—	W	—	—	—
FB	—	—	—	—	W	—	—
ZC	—	—	—	—	—	—	Q
GC	H	—	—	—	—	—	—
IC	—	H	—	—	—	—	—
VB	—	—	—	—	—	I	—

All products listed are also available in Die form

Table 1 MILITARY PACKAGE AVAILABILITY

	JB	RB	RC
	Jan Qualified	883B	883C
54	X	X	X
54LS	X	X	X
54S	X	X	X
82	X	X	X
8T	—	X	X
93XX	X	X	X
96XX	—	X	X
Analog	X	X	X
Bipolar Memory	X	X	X
Microprocessor	—	X	X

Table 2 MILITARY SUMMARY

MIL-STD-883, LEVEL B

Processing to this option is ideal when no JAN slash sheets are released on devices required. Product is processed to Mil-Std-883 Method 5004, and is 100% electrically tested to industry data sheets. Devices are selectively available as custom processed parts with electricals screened to the JAN Slash Sheets.

MIL-STD-883, LEVEL C

If you need a Military temp, range device, but do not require burn in screening performed, our 883C product is ideal. 883C parts are the standard full Mil-Temperature range product to the Signetics data sheet parameters and screened to MIL-STD-883, Class C.

MILITARY GENERIC DATA

Signetics has a new program for those customers who require quality conformance data on their products. This program allows our customers to obtain reliability information without the necessity or running Groups B, C and D inspections for their particular purchase order. It provides for the customer something that has not been readily available before in the semiconductor industry in that all Military Generic Data is controlled and audited by both Government Inspection in the case of JAN data and Signetics Quality Assurance.

Signetics Military Generic Data is compiled by the Military Products Division based on data from 1) JAN quality conformance lots, and 2) Data generated by quality conformance lots run for other reliability programs. Refer to Table 4.

A Military Generic family is defined as consisting of die function and package type families.

Military Generic Data

- Allows our customers to qualify Signetics products based on existing quality conformance data performed at Signetics.
- Allows our customers to reduce costs and improve deliveries.
- Provides assurance that all Signetics die function families and packages meet Mil-M-38510 and customer reliability requirements.
- Provides an attributes summary to the customer backed by lot identity and traceability.

MILITARY PRODUCTS/PROCESS LEVELS

PROCESS LEVEL AND MARKETING	PRE-CAP VISUAL	BURN IN	FUNCTIONAL TEST	DC/AC @25°C	DC/AC @TEMP	QPL	OFFSHORE
JB JM38510XXXXX	2010, Cond. B	Yes	100%	100%	100%	Yes	No
RB SXXXX883B	2010, Cond.B	Yes	100%	100%	100%	No	Yes
RC SXXXX883C	2010, Cond. B	No	100%	100% dc Sample ac	Sample dc only	No	Yes

Table 3 MILITARY PRODUCTS PROCESSING MATRIX

QUALIFIED	QUALIFIES	OPTION 1	OPTION 2
SUB-GROUPS			
A*	Electrical Test		
B	Package—Same package construction and lead finish.	Data selected from devices manufactured within 6 weeks of the manufacturing period on the same production line through final seal.	Data selected from devices manufactured within 24 weeks of manufacturing period.
C	Die/Process—Devices representing the same process families.	Data selected from representative devices from the same microcircuit group and sealed within 12 weeks of the manufacturing period.	Data selected from the representative devices from the same microcircuit group and sealed within 48 weeks of the manufacturing period.
D	Package—Same package construction and lead finish.	Data selected from the devices representing the same package construction and lead finish manufactured within the 24 weeks of manufacturing period. If specific data not available, Option 2 will be supplied	Data selected from the devices representing the same package construction and lead finish manufactured within the 52 weeks of manufacturing period.

NOTE*
Group A is performed on each lot or sublot of Signetics devices.

Table 4 DEFINITION AND QUALIFYING MANUFACTURING PERIODS FOR GENERIC DATA

MILITARY PRODUCTS/PROCESS LEVELS

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 AND MIL-STD-883 REQUIREMENTS, METHDS AND TEST CONDITIONS	REQUIREMENT	PROCESSING LEVELS			
			CLASS S	JAN QUALIFIED (JB)	883B (RB)	883C (RC)
General Mil-M-38510 1. Pre-Certification A. Product Assurance Program Plan B. Manufacturer's Certification	The Manufacturer shall establish and implement a Products Assurance Program Plan and provide for a manufacturer survey by the qualifying activity, Para. 3.4.1.1	—	X	X	N/A	N/A
2. Certification	Received after manufacturer has completed a successful survey, Para. 3.4.1.2	—	X	X	N/A	N/A
3. Device Qualification	Device qualification shall consist of subjecting the desired device to groups A, B, C & D of method 5005 to tightened LTPD, Para. 3.4.1.2	—	X	X	N/A	N/A
4. Traceability	Traceability maintained back to a production lot Para. 3.4.6	—	X	X	X	X
5. Country of Origin	Devices must be manufactured, assembled, and tested within the U.S. or its territories, Para. 3.2.1	—	X	X	N/A	N/A
Screening Per Method 5004 of Mil-Std-883						
6. Internal Visual (Precap)	2010, Cond. A or B	100%	XA	XB	XB	XB
7. Stabilization Bake	1008, Cond. C Min; (24 Hrs @ 150°C)	100%	X	X	X	X
8. Temperature Cycling* *For Class B and C devices thermal shock may be substituted, 1011, Cond. A; (15 cycles, 0° to +100°C)	1010, Cond. C; (10 cycles, −65°C to +150°C)	100%	X	X	X	X
9. Constant Acceleration	2001, Cond. E; (30kg in Yl Plane)	100%	X	X	X	X
10. Visual Inspection	There is no test method for this screen; it is intended only for the removal of "Catastrophic Failures" defined as "Missing Leads, Broken Packages or Lids Off."	100%	X	X	X	X
11. Seal (Hermeticity)	1014					
A. Fine	Cond. A or B (5.0 X 10^{-8}CC/Sec)	100%	X	X	X	X
B. Gross	Cond. C2 Min.	100%	X	X	X	X
12. Interim Electricals (Pre Burn-In)	Per applicable device specification	100% Optional	100% Read & Record	Slash Sheet	Data Sheet	N/A
13. Burn-In	1015, Cond. as specified (160 hrs. Min. at 125°C)	100%	100% 240 hrs.	X	X	N/A
14. Final Electricals	Per applicable Device Specification	100%	100% Read & Record	Slash Sheet	Data Sheet	Data Sheet
A. Static Tests @ 25°C	Sub Group 1		X	X	X	X
B. Static Tests @ +125°C	Sub Group 2		X	X	X	N/A
C. Static Tests @ −55°C	Sub Group 3		X	X	X	N/A

Table 5 REQUIREMENTS AND SCREENING FLOWS FOR STANDARD PRODUCTS

MILITARY PRODUCTS/PROCESS LEVELS

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 AND MIL-STD-883 REQUIREMENTS, METHODS AND TEST CONDITIONS	REQUIREMENT	PROCESSING LEVELS			
			CLASS S	JAN QUALIFIED (JB)	883B (RB)	883C (RC)
D. Dynamic Test @25°C	Sub Group 4 (for Linear Product Mainly)		X	X	X	X
E. Functional Test @25°C	Sub Group 7		X	X	X	X
F. Switching Test @25°C	Sub Group 9		X	X	X	N/A
15. Percent Defective allowable (PDA)	A PDA of 10% is a normal requirement applied against the static tests @25°C (A-1). This is controlled by the slash sheets for JB products. For RB 10% is standard	10%	10% 3% Funct"l	X	X	N/A
16. Marking	Fungus Inhibiting Paint	100%	As Req'd	JM38510/XXXX Slash Sheet #	SXXXX 883B	SXXXX 883C
17. X-Ray	2012		100%	N/A	N/A	N/A
18. External Visual	2009	100%	X	X	X	X
Quality Conformance Inspection per Method 5005 of Mil-Std 883						
19. Group A	Electrical Tests-Final Electricals (#14 above) repeated on a sample basis. (Sub Groups 1 thru 12 as specified.)	Each Lot	X	X	X	X
20. Group B	Package functional and constructional related test I.E. package dimensions, resistance to solvents, internal visual & mechanical, bond strength & solderability.	Every 6 week per pkg. group	X	X	Generic Data Available	
21. Group C	Die related tests I.E. 1,000 hr. operating life, temperature cycling, & constand acceleration.	Every 3 months per μcircuit type	X	X	Generic Data Available	
22. Group D	Package related tests I.E. physical dimensions, lead fatigue, thermal shock, temperature cycle, moisture resistance, mechanical shock, vibration variable frequency constant acceleration, & salt atmosphere.	Every 6 months per package type	X	X	Generic Data Available	

Table 5 REQUIREMENTS AND SCREENING FLOWS FOR STANDARD PRODUCTS (Cont'd)

MILITARY SELECTION GUIDE

DEVICE	DESCRIPTION	PACKAGE		AVAILABILITY			QUAL STATUS
		DIP	CAN	883C	883B	83510/SHEET	
OPERATIONAL AMPLIFIERS							
LF155	Bi-FET Op Amp		H	X	X		
LF156	Bi-FET Op Amp		H	X	X		
LF156A	Bi-FET Op Amp		H		X		
LF198	Sample and Hold Amp		H		X		
LH2101A	Hybrid Dual Op Amp	F		X	X	10105	QPL1
LM101A	High Performance Op Amp	F, FE	H	X	X	10103	QPL1
LM124	Quad Op Amp	F		X	X		
LM158	Dual Op Amp		H	X	X		
MC1556	High Performance	F	H	X	X		
SE532	Dual Op Amp		H		X		
SE538	High Slew Rate Op Amp	F	H	X	X		
SE5512	Dual High Performance Op Amp	F			X		
SE5532	Dual Low Noise Op Amp	FE		X	X		
SE5532A	Dual Low Noise Op Amp	FE		X	X		
SE5534	Low Noise Op Amp	FE	H	X	X		
SE5534A	Low Noise Op Amp	FE	H	X	X		
SE5539	Very High Slew Rate Op Amp	F		X	X		
μA741	General Purpose Op Amp		H			10101	QPL1
μA747	Dual Op Amp	F	H	X	X	10102	QPL1
VIDEO AMPS							
μA733	Differential Video Amplifier	F	H	X	X		
SE511	Dual Differential Amplifier	F			X		
INTERFACE							
DS7820/A	Dual Line Receiver	F		X	X		
DATA CONVERSION							
DAC-08/A	8-Bit D/A Converter	F			X		
MC1508-8	8-Bit D/A Converter	F		X	X		
SE5008	8-Bit D/A Converter	F			X		
SE5009	8-Bit D/A Converter	F			X		
SE5018	8-Bit μP-Compatible D/A Converter	F			X		
SE5019	8-Bit μP-Compatible D/A Converter	F			X		
SE5118	8-Bit DAC Current Output	F		X	X		
SE5119	8-Bit DAC Current Output	F		X	X		
SAMPLE AND HOLD CIRCUITS							
SE5537	Precision Sample and Hold Amplifier		H	X	X		
LF198	Sample and Hold Amplifier		H		X		
PHASE-LOCKED LOOPS							
SE567	Phase-Locked Loop Tone Decoder	F	H	X	X		

MILITARY SELECTION GUIDE

DEVICE	DESCRIPTION	PACKAGE		AVAILABILITY			QUAL STATUS
		DIP	CAN	883C	883B	83510/SHEET	
	POWER CONTROLLERS						
SE5560	SMPS Control Circuit	F			X		
SG1524	SMPS Control Circuit	F			X		
SE5551	Dual Polarity Regulator	F			X		
SE5552	Dual Polarity Regulator	F			X		
SE5553	Dual Polarity Regulator	F			X		
SE5554	Dual Polairty Regulator	F			X		
SE5555	Dual Polarity Regulator	F			X		
	TIMERS						
SE555	Timer	F, FE	H	X	X	10901	QPL1
SE556-1	Dual Timer	F		X	X	10902	QPL1
SE558	Quad Timer	F			X		
	COMPARATORS						
SE521	High-Speed Dual Differential Comparator	F		X	X		
SE522	High-Speed Dual Differential Comparator	F		X	X		
SE527	Voltage Comparator	F	H	X	X		
SE529	Voltage Comparator	F	H	X	X		
LH2111	Hybrid Dual Comparator	F		X	X		
LM111	Voltage Comparator	F	H	X	X		
LM139/A	Quad Comparator	F			X		
LM193/A	Dual Comparator	F			X		
LM119	Dual Voltage Comparator	F	H		X		

MILITARY CROSS REFERENCE

FAIRCHILD	SIGNETICS
μA111	LM111
μA139	LM139
μA733	μA733
μAF155/156	LF155/156
μA101	LM101
μA101A	LM101A
MC1556	MC1556
μA1558	MC1558
μA747	μA747
MC1555	SE555
μA556	SE556
μA723	μA723

MOTOROLA	SIGNETICS
MLM111	LM111
MC1733	μA733
LF155/56	LF155/156
MLM101	LM101
MLM101A	LM101A
MC1558	MC1558
MC1747	μA747
MC3556	SE556
MC1723	μA723
MC1508	MC1508-8

NATIONAL	SIGNETICS
LM161	SE527
LH2111	LH2111
LM111	LM111
LM119	LM119
LM139	LM139
LM193	LM193/193A
LM733	μA733
LF155/56	LF155/156
LH2101A	LH2101A
LH2108A	LH2108A
LM101A	LM101
LM101	LM101A
LM124	LM124
LM158	LM158
LM1558	MC1558
LM1581	SE532
LM747	μA747
LM567	SE567
DM7820	DM7820
DM7830	DM7830
LM555	SE555
LM723	μA723

PMI	SIGNETICS
SSS1508	MC1508-8
DAC-08	SE5008

RAYTHEON	SIGNETICS
LM111	LM111
LM139	LM139
RM733	μA733
LF155/56/57	LF155/156
LM101	LM101
LM101A	LM101A
LM124	LM124
RM1556	MC1556
RM1558	MC1558
RM747	μA747
RM555	SE555
RM723	μA723

T.I.	SIGNETICS
LM111	LM111
SN52733	μA733
LF155/56	LF155/156
SN52101A	LM101A
SN55182	DM7820
SN55183	DM7830
SN52555	SE555
SE556	SE556
SN52723	μA723

Section 18
Appendices

INDEX

PACKAGE OUTLINES

INTRODUCTION

The following information applies to all packages unless otherwise specified on individual package outline drawings.

General

1. Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).
2. Lead spacing shall be measured within this zone.
   a. Shoulder and lead tip dimensions are to centerline of leads.
3. Tolerances non-cumulative.
4. Thermal resistance values are determined by utilizing the linear temperature dependence of the forward voltage drop across the substrate diode in a digital device to monitor the junction temperature rise during known power application across V_{CC} and ground. The values are based upon 120 mils square die for plastic packages and a 90 mils square die in the smallest available cavity for hermetic packages. All units were solder mounted to P.C. boards, with standard stand-off, for measurement.

PLASTIC ONLY

5. Lead material: Alloy 42 (Nickel/Iron Alloy) Olin 194 (Copper Alloy) or equivalents, solder dipped.
6. Body material: Plastic (Epoxy)
7. Round hole in top corner denotes lead No. 1.
8. Body dimensions do not include molding flash.
9. SO Packages-microminiature packages.
   a. Lead material: Alloy-42.
   b. Body material: Plastic (Epoxy).

HERMETIC ONLY

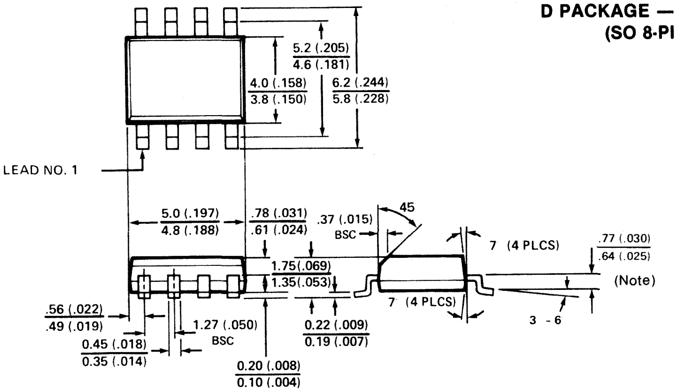
10. Lead material
    a. ASTM alloy F-15 (KOVAR) or equivalent—gold plated, tin plated, or solder dipped.
    b. ASTM alloy F-30 (Alloy 42) or equivalent—tin plated, gold plated or solder dipped.
    c. ASTM alloy F-15 (KOVAR) or equivalent—gold plated.
11. Body Material
    a. Eyelet, ASTM alloy F-15 or equivalent—gold or tin plated, glass body.
    b. Ceramic with glass seal at leads.
    c. BeO ceramic with glass seal at leads.
    d. Ceramic with ASTM alloy F-30 or equivalent.
12. Lid Material
    a. Nickel or tin plated nickel, weld seal.
    b. Ceramic, glass seal.
    c. ASTM alloy F-15 or equivalent, gold plated, alloy seal.
    d. BeO Ceramic with glass seal.
13. Signetics symbol, angle cut, or lead tab denotes Lead No. 1.
14. Recommended minimum offset before lead bend.
15. Maximum glass climb .010 inches.
16. Maximum glass climb or lid skew is .010 inches.
17. Typical four places.
18. Dimension also applies to seating plane.

PACKAGE OUTLINES

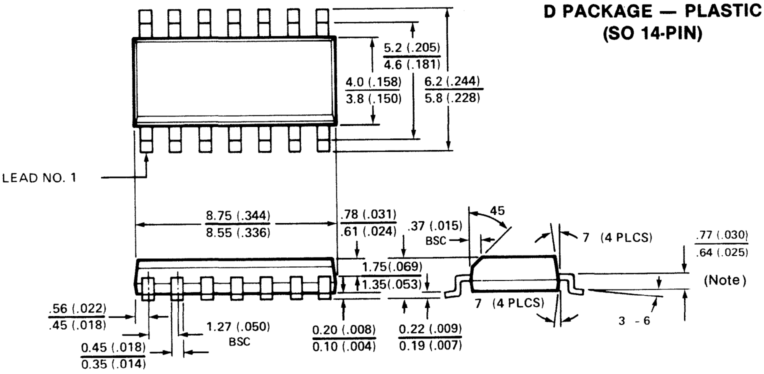
PLASTIC PACKAGES			
	PACKAGE CODE	Θ_{ja}/Θ_{jc}(°C/W)	DESCRIPTION
SO Packages			
8-Pin	D	110	SO-8
14-Pin	D	100	SO-14
16-Pin	D	100	SO-16
Standard Dual-In-Line			
8-Pin	N	162/65	
14-Pin	N	150/65	TO-116/MO-001
16-Pin	N	137/53	MO-001
18-Pin	N	135/53	
20-Pin	N	135/53	
22-Pin	N	120/53	
24-Pin	N	116/53	MO-015
28-Pin	N	116/53	MO-015
Power Dual-In-Line			
14-Pin	N	95/33	Butterfly
16-Pin	N	95/33	Butterfly
18-Pin	N	90/26	Butterfly
20-Pin	N	90/26	Butterfly
24-Pin	N	60/23	Heatsink
28-Pin	N	56/21	Heatsink
Metal Headers			
3-Pin	H	100/20	TO-5 Header
4-Pin	E	100/20	TO-46 Header
4-Pin	E	150/25	TO-72 Header
8-Pin	H	150/25	TO-5 Header
10-Pin	H	150/25	TO 5/TO-100 Header, Short Can
10-Pin	H	150/25	TO-5/TO-100 Header, Tall Can
Flat Packs			
10-Pin	W	240/50	Flat Ceramic
16-Pin	W	200/50	Flat Ceramic
Cerdip Family			
8-Pin	FE	110/30	Dual-in-Line Ceramic
14-Pin	F	110/30	Dual-in-Line Ceramic
16-Pin	F	100/30	Dual-in-Line Ceramic
18-Pin	F	93/27	Dual-in-Line Ceramic
20-Pin	F	90/25	Dual-in-Line Ceramic
22-Pin	F	75/27	Dual-in-Line Ceramic
24-Pin	F	60/26	Dual-in-Line Ceramic
28-Pin	F	57/27	Dual-in-Line Ceramic
Laminated Ceramic, Side Brazed Lead			
14-Pin	I	95/25	Dip Laminate
16-Pin	I	90/25	Dip Laminate
28-Pin	I	60/25	Dip Laminate

PACKAGE OUTLINES

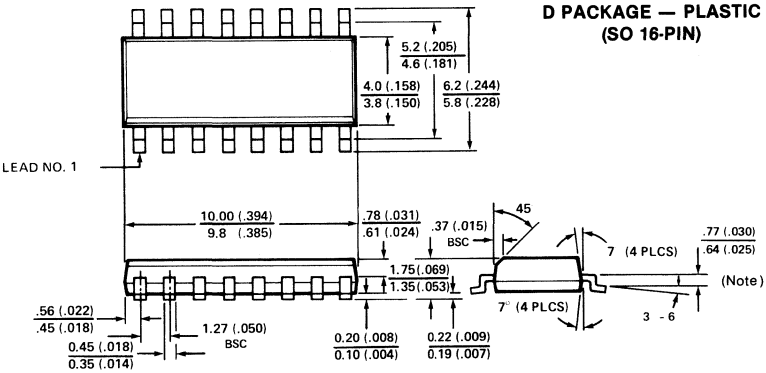
D PACKAGE — PLASTIC (SO 8-PIN)



D PACKAGE — PLASTIC (SO 14-PIN)

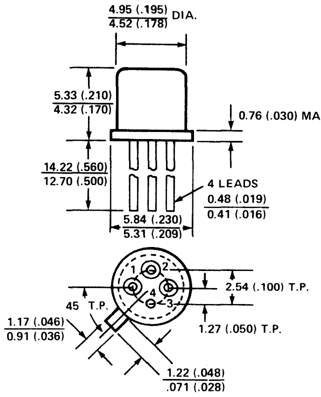


D PACKAGE — PLASTIC (SO 16-PIN)

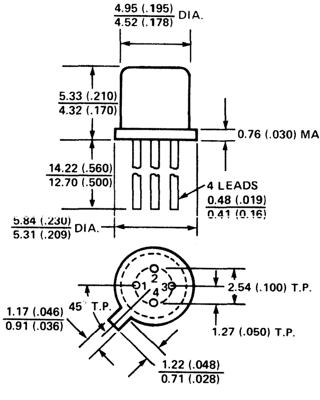


PACKAGE OUTLINES

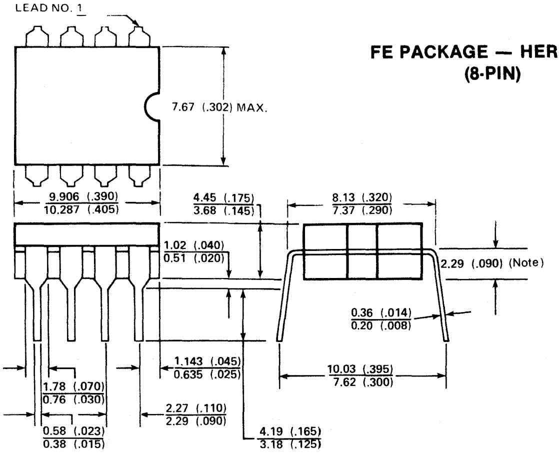
E PACKAGE — HERMETIC (TO-46 HEADER)



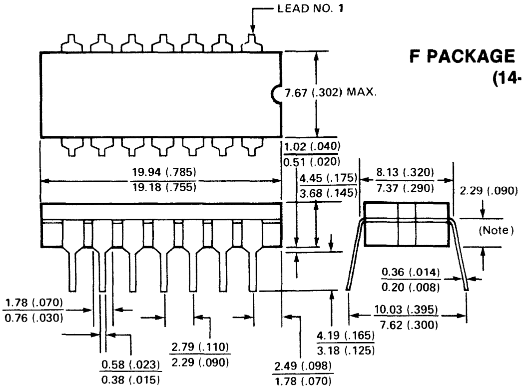
E PACKAGE — HERMETIC (TO-72 HEADER)



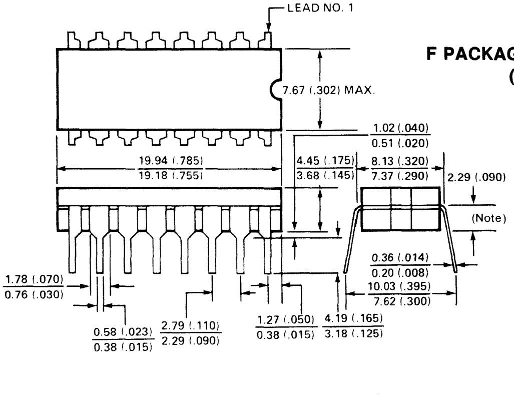
PACKAGE OUTLINES



FE PACKAGE — HERMETIC (8-PIN)



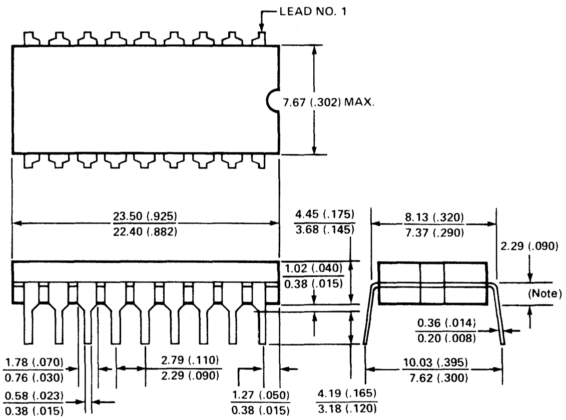
F PACKAGE — HERMETIC (14-PIN)



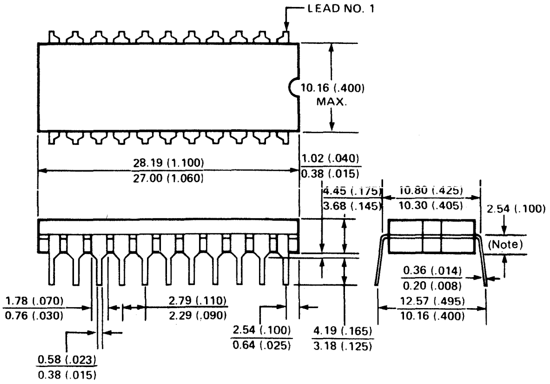
F PACKAGE — HERMETIC (16-PIN)

PACKAGE OUTLINES

F PACKAGE — HERMETIC
(18-PIN)

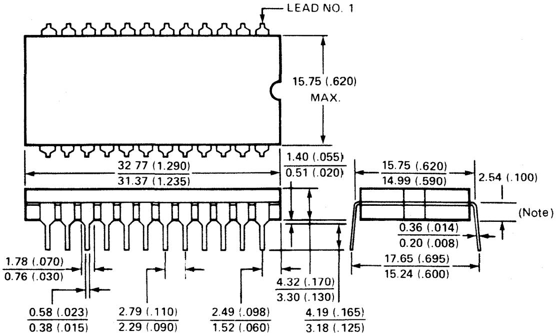


F PACKAGE — HERMETIC
(22-PIN)

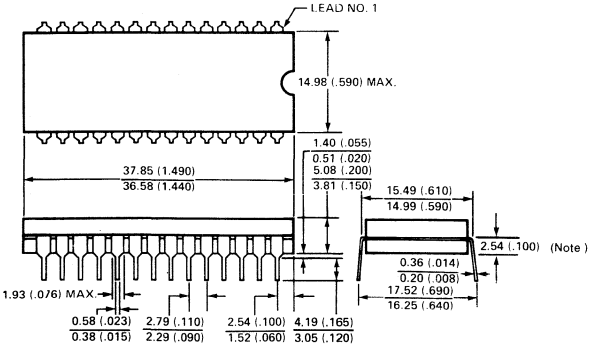


PACKAGE OUTLINES

F PACKAGE — HERMETIC
(24-PIN)

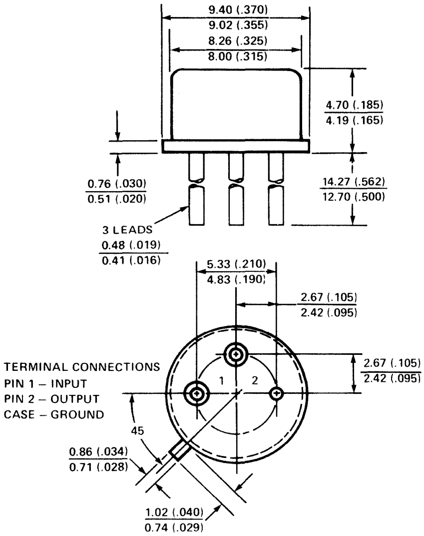


F PACKAGE — HERMETIC
(28-PIN)

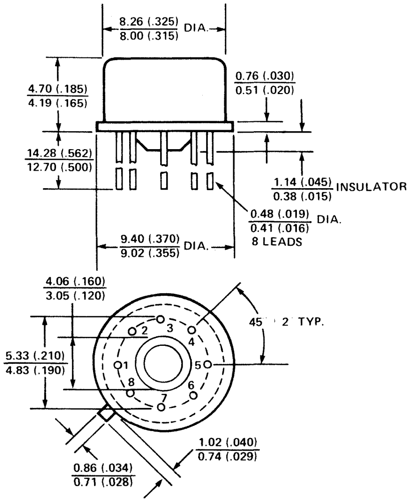


PACKAGE OUTLINES

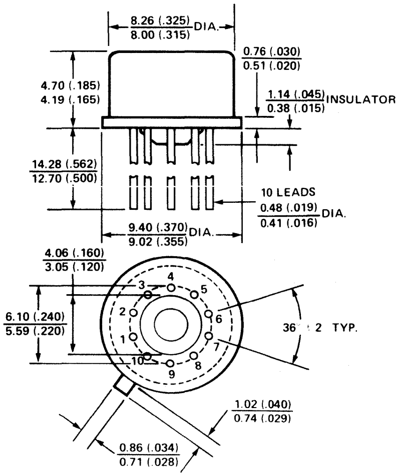
H PACKAGE — HERMETIC
3-PIN
(TO-5 HEADER)



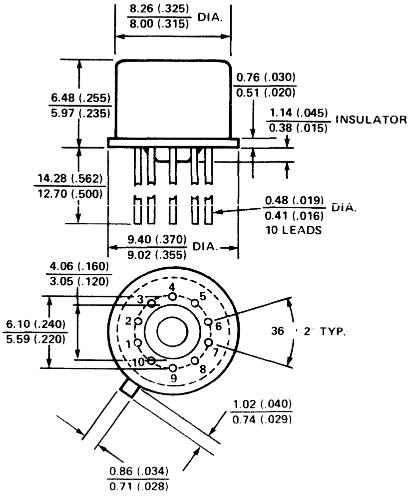
H PACKAGE — HERMETIC
8-PIN
(TO-5 HEADER)



H PACKAGE — HERMETIC
10-PIN
(TO-5/100 HEADER
SHORT CAN)

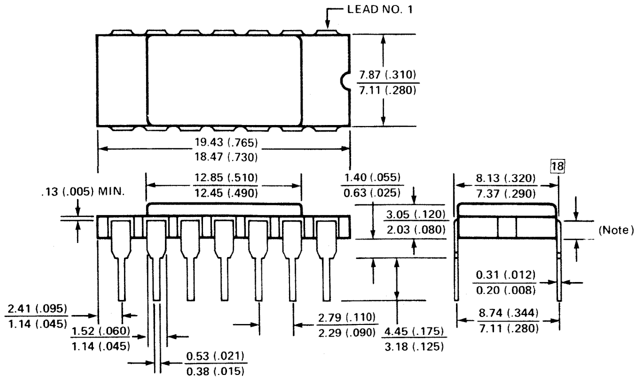


H PACKAGE HERMETIC
10-PIN
(TO-5/100 HEADER
TALL CAN)

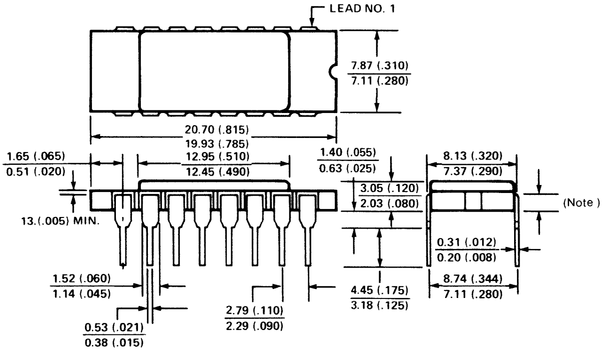


PACKAGE OUTLINES

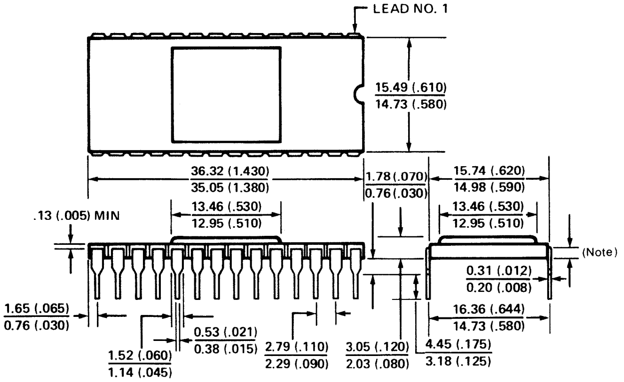
I PACKAGE — HERMETIC (14-PIN)



I PACKAGE — HERMETIC (16-PIN)

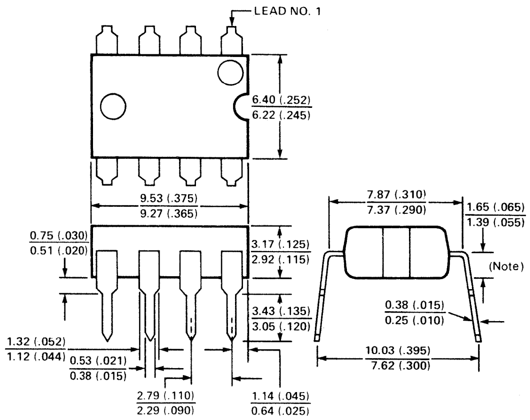


I PACKAGE — HERMETIC (28-PIN)

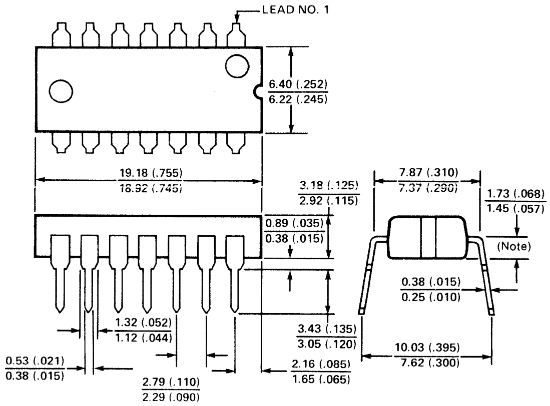


PACKAGE OUTLINES

N PACKAGE — PLASTIC
(8-PIN)

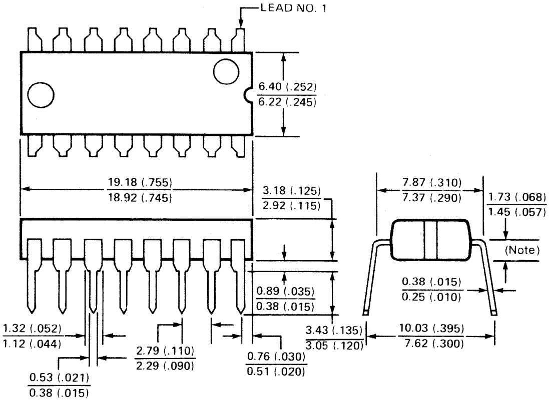


N PACKAGE — PLASTIC
(14-PIN)

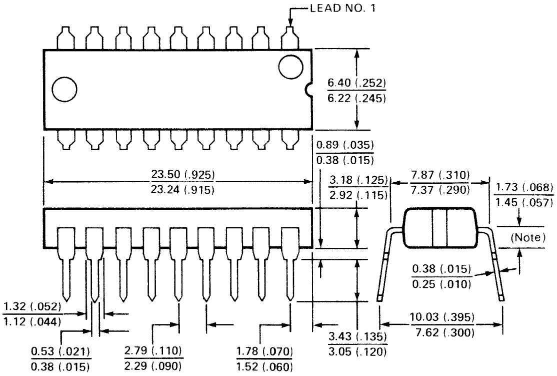


PACKAGE OUTLINES

N PACKAGE — PLASTIC (16-PIN)

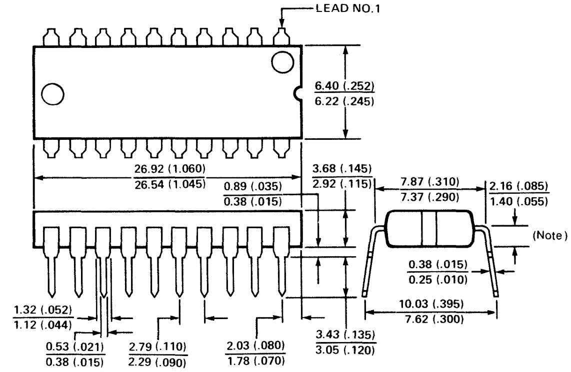


N PACKAGE — PLASTIC (18-PIN)

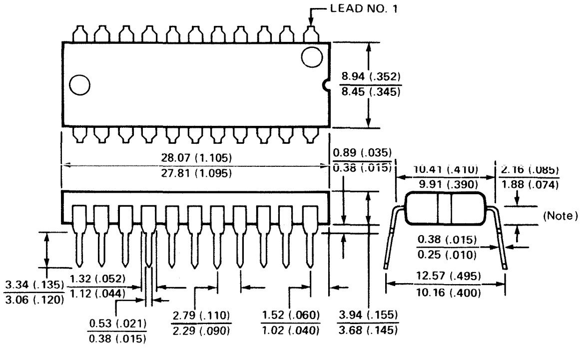


PACKAGE OUTLINES

N PACKAGE — PLASTIC (20-PIN)

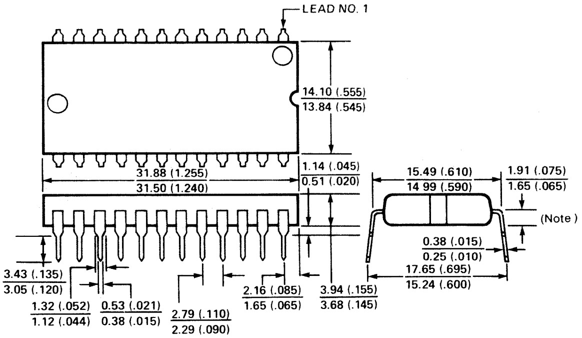


N PACKAGE — PLASTIC (22-PIN)

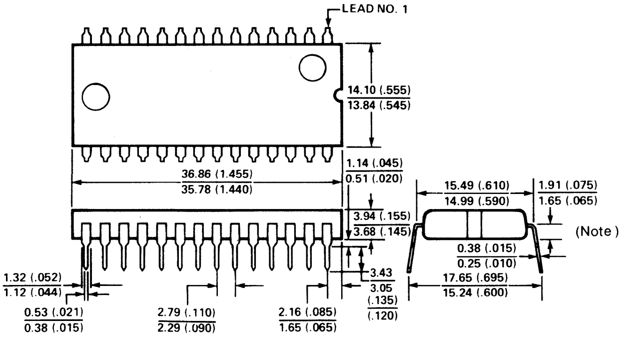


PACKAGE OUTLINES

N PACKAGE — PLASTIC (24-PIN)

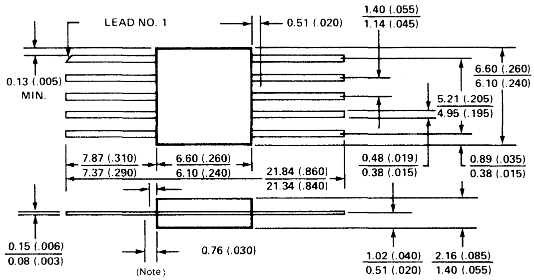


N PACKAGE — PLASTIC (28-PIN)

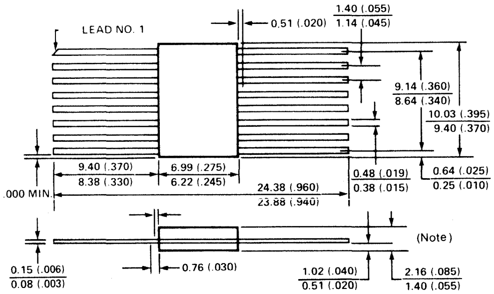


PACKAGE OUTLINES

W PACKAGE — HERMETIC
(10-PIN)



W PACKAGE — HERMETIC
(16-PIN)



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